High-Frequency Small Signal AC and Noise Modeling of MOSFETs for RF IC Design

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***Abstract*—In this paper, high-frequency (HF) AC and noise modeling of MOSFETs for radio frequency (RF) integrated circuit (IC) design is discussed. A subcircuit RF model incorporating the HF effects of parasitics is presented. This model is compared with the measured data for both y parameter and f_T characteristics. Good model accuracy is achieved against measurements for a 0.25 μm RF CMOS technology. The HF noise predictivity of the model is also examined with measured data. Furthermore, a methodology to extract the channel thermal noise of MOSFETs from HF noise measurements is presented. By using the extracted channel thermal noise, any thermal noise models can be verified directly. Several noise models including the RF model discussed in this paper have been examined, and the results show that the RF model can predict the channel thermal noise better than the other models.**

***Index Terms*—Circuit simulation, high-frequency noise modeling, radio frequency (RF) integrated circuit (IC) design, RF MOSFET modeling.**

I. Introduction

WITH the fast growth of radio frequency (RF) wireless communications market, RF designers have begun to explore the use of CMOS devices in RF circuits. Accurate and efficient RF MOSFET models are required. It has been known that a device model emphasizing on low frequency applications cannot be used directly in RF [1]. Compared with the MOSFET modeling at low frequency, compact RF models are difficult to develop. Many microwave circuit designers use a table-look-up approach based on measurements. However, this approach requires a large database obtained from numerous device measurements, and becomes questionable when used to simulate the statistical behavior of the RF circuits or to perform predictive simulations for those circuits before having "silicon."

Recently, work has been reported to model the RF performance of submicron MOS devices [1]–[5]. Most of them are focused on the discussion of the HF equivalent circuit and the fitting of the s- or y-parameters. Some of them discussed the HF noise characteristics [6]. But the results of the noise parameters are from direct calculations of the equivalent circuits instead of from simulations of the compact model in a circuit simulator, so it is difficult to judge its validity of the noise model after implementing it in a circuit simulator. In this paper, we discuss the details of the modeling of the parasitic components, and present a simple subcircuit MOSFET model for RF applications. The model is accurate in y-parameters (up to the $1/2f_T$ frequency range) and f_T characteristics in the device geometry range for RF ICs. The Nonquasistatic (NQS) behavior of the model has also been verified with measurements. Further, we examine the HF noise performance of the subcircuit RF model with measured data and present a methodology to extract the channel thermal noise from the measured data, which is very important in HF noise modeling as it provides a way to check the validity and accuracy of a noise model. With the extracted channel thermal noise data, the noise characteristics of several noise models including the RF model discussed in this paper are examined.

Manuscript received June 15, 2001; revised November 20, 2001. The review of this paper was arranged by Editor C. McAndrew.

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Publisher Item Identifier S 0018-9383(02)01560-5.

II. AC Small Signal Modeling at RF

A. Equivalent Circuit of the AC Model and the Components

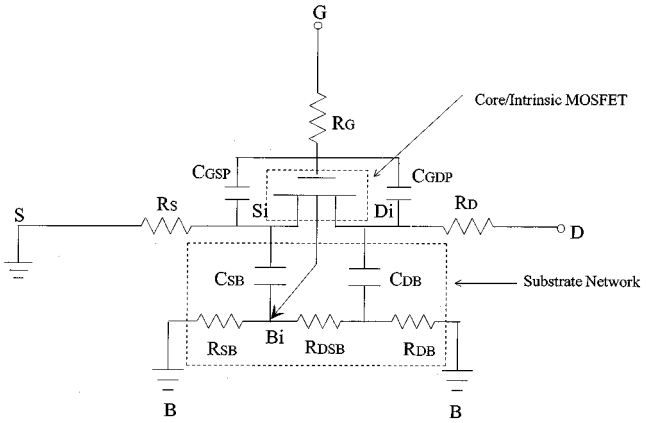
With the parasitic components at the gate, source, drain and substrate, an RF model based on the subcircuit approach is given in Fig. 1(a). The core intrinsic model can be any MOSFET model that is suitable for analog applications, and in this paper, it is BSIM3v3 [7]. The equivalent circuit (EC) of the RF model is shown in Fig. 1(b). Even though it is not very precise to represent the subcircuit model in Fig. 1(a) by the EC in Fig. 1(b), it can approximately describe the HF characteristics of the subcircuit model in saturation region and simplify the model analysis to facilitate the model parameter extraction.

At dc and low frequency, the gate resistance R_G consists mainly of the polysilicon sheet resistance. At HF, however, two additional physical effects will affect the effective gate resistance. One is the gate-distributed effect (GDE), and another one is the nonquasistatic effect (NQS) in the channel [6], [8].

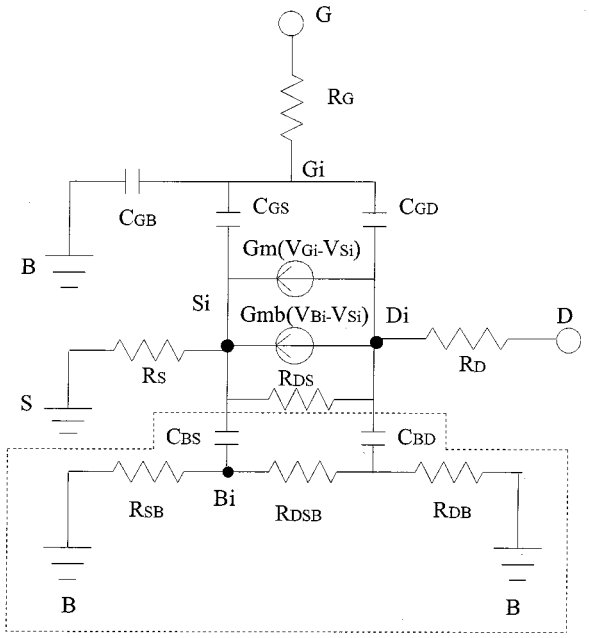
A simple expression of gate resistance R_G has been used to calculate gate resistance with the influence of GDE

$$R_{G,\mathrm{poly}} = \frac{R_{\mathrm{Gsh}}}{N_f L_f}\left(W_{\mathrm{ext}} + \frac{W_f}{\alpha}\right) \tag{1}$$

where R_{Gsh} is the gate sheet resistance, W_f is the channel width per finger, L_f is the channel length, and N_f is the number of fingers, W_{ext} is the extension of the polysilicon gate over the active region, α is a fitting parameter, typically three or 12 depending on whether the gate fingers are connected to one side or to both sides to account for the GDE.



(a)



(b)

Fig. 1. (a) Schematic of the subcircuit model for a RF MOSEFT and (b) an equivalent circuit of the subcircuit RF model in saturation regime. $C_{\rm GD} = C_{\rm GDP} + C_{\rm GDi}$ and $C_{\rm GS} = C_{\rm GSP} + C_{\rm GSi}$, where $C_{\rm GDP} = C_{\rm GD\,total\_extracted} - C_{\rm GD\,intrinsic\_simulated}$ and $C_{\rm GSP} = C_{\rm GS\,total\_extracted} - C_{\rm GS\,intrinsic\_simulated}$.

For the devices with NQS effects, gate resistance and inductance with additional bias and geometry dependences are introduced [6], [7], [9]. However, we do not discuss the influence of the gate inductance in this paper since the frequency range is much lower than that at which the influence of the gate inductance becomes significant.

It has been proposed that an additional resistive component in the gate should be added to represent the channel distributed RC effect [6]. When a MOSFET operates at high frequencies, the contribution to the effective gate resistance is not only from the physical gate electrode resistance but also from the distributed channel resistance, which can be "seen" by the signal applied to the gate. Thus, the effective R_G consists of two parts

$$R_G = R_{G,\rm poly} + R_{G,\rm nqs} \tag{2}$$

where $R_{G,\rm poly}$ is the distributed gate electrode resistance from the polysilicon gate material and is given by (1), and $R_{G,\rm nqs}$ is the NQS distributed channel resistance seen from the gate and is a function of both biases and geometry [6], [8].

A R_G model with the consideration of NQS effect has been reported [6]. However, the following expression can be used to obtain the $R_{G,\rm nqs}$ approximately in strong inversion regime

$$R_{G,\rm nqs} \cong \frac{\beta}{G_m} \tag{3}$$

where G_m is the device transconductance, and β is a fitting parameter with a typical value around 0.2.

The source/drain resistances R_D and R_S without including any bias dependence can be described by

$$R_D \cong R_{D0} + \frac{r_{\rm dw}}{N_f W_f} \tag{4a}$$

$$R_s \cong R_{s0} + \frac{r_{\rm sw}}{N_f W_f} \tag{4b}$$

where $r_{\rm dw}$ and $r_{\rm sw}$ are the parasitic drain and source resistances where unit width R_{D0} and R_{S0} are to account for the part of the series resistances without the width dependence.

It has been known that the source/drain resistances are bias dependent. However, (4) can work reasonably well in RF MOSFETs, because the LDD region in devices (for example, in a 0.18 μm or even more advanced technology) has a high doping concentration. Thus, the bias dependence of R_D and R_S becomes weaker compared with an older technology with lighter LDD doping.

The influence of the substrate resistance is usually ignored in compact models for low frequency application. However, at HF, the signal at the drain couples to the source and bulk terminals through the source/drain junction capacitances and the substrate resistance. The substrate resistance influences mainly the output characteristics, and can contribute as much as 20% or more of the total output admittance [10].

It has been known that the substrate components become distributed at HF [1]. Although it is always desirable to have a detailed distributed RC network to account for the contribution of the substrate components, it is too complex to be implemented in a compact model. A good compromise is to use a lumped RC network, accurate in the required operation frequency range, to simulate the contribution of the substrate components.

A simple equivalent circuit for the substrate network shown in Fig. 1 has been used to analyze the HF substrate-coupling-effect (SCE) and the characteristics of substrate resistance at HF [11]. Even though a simpler substrate network has been reported, it is found that the three-resistor substrate network can ensure better model accuracy in a frequency range up to 10 GHz.

Generally, assuming the device is symmetric between source and drain and there is no difference between the outer and inner source/drain regions in a multifinger device, we have

$$R_{\rm DSB} = \frac{r_{\rm dsb} L_f}{N_f W_f} \tag{5}$$

where $r_{\rm dsb}$ is the sheet resistance in the substrate between the source and drain.

According to the device layout used in this paper, $R_{\rm SB}$ and $R_{\rm DB}$ are functions of channel width of the device, as described approximately by the following equations:

$$R_{\rm DB} \approx \frac{r_{\rm dbw}}{W_f} \tag{6a}$$

$$R_{\rm SB} \approx \frac{r_{\rm sbw}}{W_f} \tag{6b}$$

where $r_{\rm dbw}$ and $r_{\rm sbw}$ are the substrate resistances per unit-channel-width.

Some bias dependence of the substrate resistances had been expected based on the fact that the depletion regions below the gate and surrounding the source and drain diffusions may vary at different gate and drain bias conditions [10]. However, it has been found that the bias dependence of the substrate resistances is actually very weak in the devices studied in this paper, and the above simple substrate resistance network is accurate up to 10 GHz [10], [11].

The parasitic capacitances in a MOSFET contain different components at the gate, the source, the drain and the substrate. The core model has contained most of these capacitive components. However, additional components, such as $C_{\rm GDP}$ and $C_{\rm GSP}$ obtained from the difference between the capacitances extracted from the measured s-parameters and the intrinsic capacitances simulated with the model can be added as shown in Fig. 1 in case the RF model cannot meet the accuracy requirements. According to the definition of $C_{\rm GDP}$ and $C_{\rm GSP}$, we can consider these capacitances as overlap capacitances if the intrinsic capacitance model is accurate enough. However in some cases, $C_{\rm GDP}$ and $C_{\rm GSP}$ should not be called as overlap capacitances since they may contain part of the intrinsic capacitances if the intrinsic capacitances are not properly modeled.

The substrate capacitance $C_{\rm sub}$, existing at high frequencies to describe the capacitive effect in the substrate material, is another extrinsic capacitance that should be considered in an RF model. We do not include this substrate capacitance in the above substrate RC network. It does not influence the model accuracy significantly to describe the device HF behavior up to 10 GHz. However, $C_{\rm sub}$ is important in a RF model when the device operates at frequencies much higher than 10 GHz.

B. Model Parameter Extraction and Simulations

Based on the equivalent circuit in Fig. 1(b), the following approximate equations can be obtained from a detailed y-parameter analyses:

$$y_{11} \approx \omega^2 \left(C_{\rm GG}^2 R_G + C_{\rm GS}^2 R_S + C_{\rm GD}^2 R_D\right) + j\omega C_{\rm GG} \tag{7a}$$

$$y_{12} \approx -\omega^2 C_{\rm GG} C_{\rm GD} R_G - j\omega C_{\rm GD} \tag{7b}$$

$$y_{21} \approx G_m - \omega^2 C_{\rm GG} C_{\rm GD} R_G - j\omega (C_{\rm GD} + G_m R_G C_{\rm GG}) \tag{7c}$$

$$y'_{22} \approx \frac{R_{\rm DB}(R_{\rm SB} + R_{\rm DSB})}{R_{\rm DB} + R_{\rm SB} + R_{\rm DSB}} (\omega C_{\rm BD})^2 + R_G (\omega C_{\rm GD})^2 + \frac{1}{R_{\rm DS}} + j\omega (C_{\rm GD} + C_{\rm BD}) \tag{7d}$$

where y'_{22} is the y_{22} without the influence of R_D. The assumptions of $\omega^2 (C_{\rm GS} + C_{\rm GB})^2 R_G^2 \ll 1$ and $(\omega C_{\rm GD})^2 R_G^2 \ll 1$ are used in the derivation, which are generally valid up to 10 GHz [4], [10].

The parameters for the components in the RF model can be extracted directly from the measured HF data according to the previous equations [4], [10], [11]. For devices with short channel lengths, a R_G component without additional bias and geometry dependence as given in (1) can be used to simulate the HF characteristics with sufficient accuracy. Since the core model has included the overlap capacitance with bias dependence, we do not include $C_{\rm GSP}/C_{\rm GDP}$ in the RF model.

The model has been examined with the devices of different geometries at different bias conditions. The devices are fabricated with a 0.25 μm RF CMOS technology. Multifinger devices with lengths L_f from 0.36 μm to 1.36 μm and width per finger (W_f) from 2.5 μm to 12 μm are characterized with a HF measurement system consisting of a HP8510 vector network analyzer and a HP4142 I-V tester. S-parameters are measured and are then converted to Y-parameters to facilitate the parameter extraction. The measured raw data are de-embedded with a two-step (open and short) procedure to remove the influence of the parasitics from the pads [12]. The model parameters for the intrinsic devices as well as for the series source/drain resistances are extracted from the measured dc data. Other parameters for the components such as $R_G, R_{\rm DB}, R_{\rm SB}$ etc. and some parameters for the capacitances are extracted from the measured HF and AC data.

The simulations with the RF model show satisfactory agreement to experiments. As examples, Fig. 2 shows the comparison of the y-parameter characteristics between measurements and the model for devices with different geometries at $V_G = V_D = 1$ V. A good match between the model and data demonstrates that the RF model is accurate up to 10 GHz. Fig. 3 gives the comparison of f_T-I_D characteristics between the model and measurements for several devices. Together with the plots in Fig. 2, it demonstrates that the RF model can predict the HF characteristics of the devices with different geometries at different biases.

C. Modeling of NQS Effects

It has been known that NQS effect should be included in a RF model to accurately describe the HF characteristics of devices at HF. Most MOSFET models available in circuit simulators use the quasistatic (QS) approximation. In a QS model, the channel charge is assumed to be a unique function of the instantaneous biases, i.e., the charge has to respond to a change in voltages with infinite speed. Thus, the finite charging time of the carriers in the inversion layer is ignored. In reality, the carriers in the channel do not respond to the signal immediately, and hence, the channel charge is not a unique function of the instantaneous terminal voltages (quasistatic) but a function of the history of the voltages (non-quasistatic). This problem may become pronounced in RF applications, where the input signals may have rise or fall times comparable to, or even smaller than, the channel transit time. Because the carriers in these devices cannot follow the changes of the applied signal, the QS models may give inaccurate simulation results that cannot guide circuit design.

The NQS effect can be modeled with different approaches for RF applications: (a) $R_G$approach in which a bias-dependent gate resistance is introduced to account for the distributed ef-

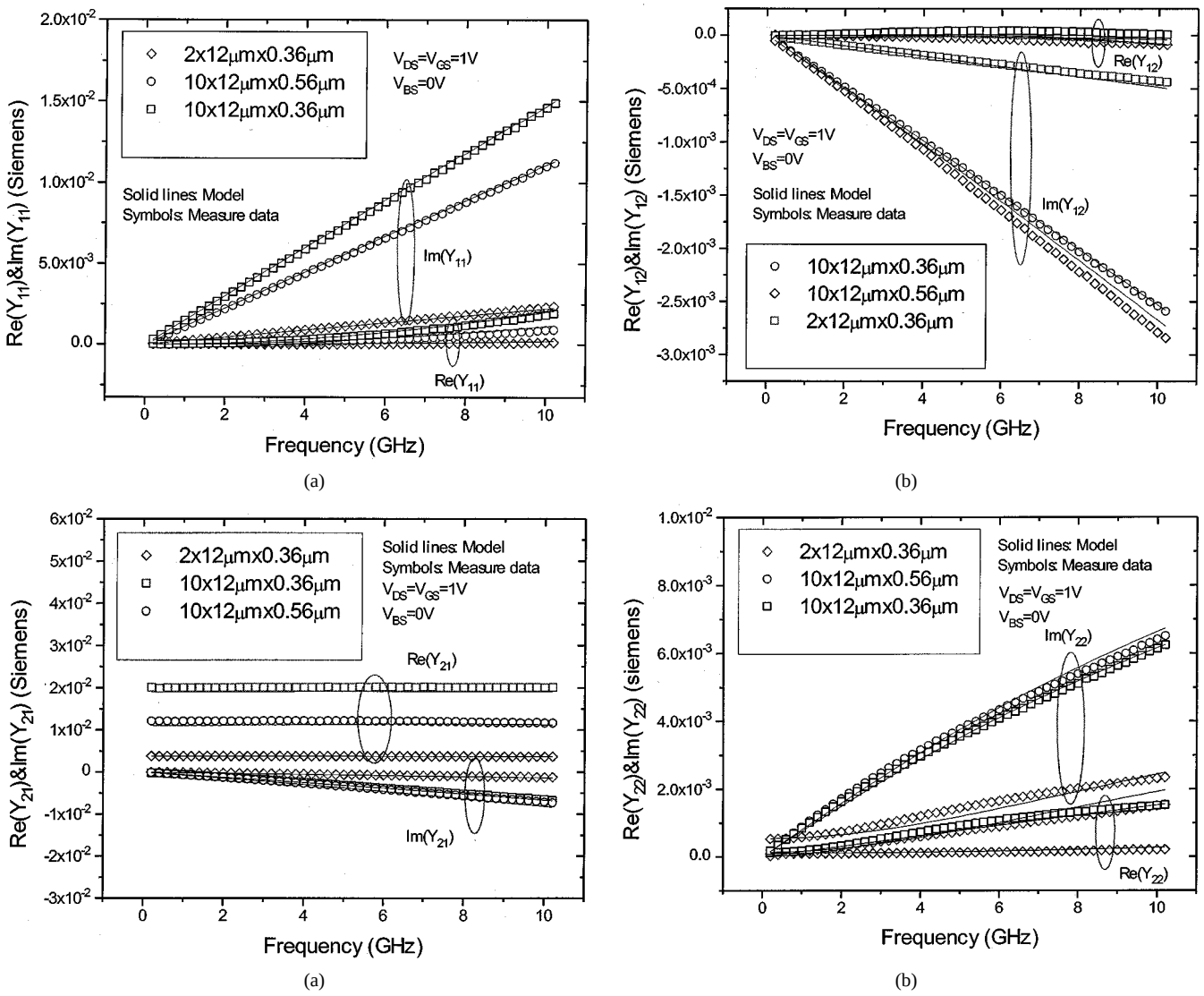


Fig. 2. Comparison of simulated and measured y-parameters (a) y_{11}; (b) y_{12}; (c) y_{21}; and (d) y_{22} (both real part and imaginary part) versus frequency at $V_{\rm GS} = V_{\rm DS} = 1$ V for several devices.

fects from the channel resistance as discussed earlier [6], (b) R_i approach in which a resistance R_i (as used in modeling a MESFET or HEMT) is introduced [13], (c) transadmittance approach in which a voltage-control-current-source (VCCS) is connected in parallel to the intrinsic capacitances and transconductances to model the NQS effect [10], [14], and (d) core model approach in which the NQS effect can be modeled in the core intrinsic model [7]. It should be pointed out that all of these approaches would have to deal with complex implementation issues.

Both R_G and R_i approaches will introduce additional resistance components in the model besides the existing physical gate and channel resistances, so the noise characteristics of the model using either R_G or R_i approach need to be examined. Ideally, the NQS effect should be included in the core intrinsic model if the model can predict both NQS and noise characteristics without a large penalty in the model implementation and simulation efficiency.

In this paper, the NQS model is contained in the core model. The NQS model utilized a Elmore's approach, in which the RF distributed channel has been represented approximately by a simple RC network that retains the lowest frequency pole of the original RC network [7]. In Fig. 4, simulation results of the RF model with and without NQS effects are shown with a comparison to the measured data. Without including the NQS effect, the model cannot predict the measured y_{21} at higher frequencies, while the model with NQS effect can simulate the measured data very well. The inclusion of the NQS effect would be a desirable feature for a RF model even though it remains a question whether the devices in RF circuits for small-signal applications will operate in the frequency region at which the devices show significant NQS effects.

III. HF Noise Modeling

In this section, we study thermal noise characteristics of the earlier subcircuit RF model that uses the built-in noise models in the core model [7]. And also, we discuss a methodology of extracting the channel thermal noise from measured data and use the extracted thermal noise to validate different noise models.

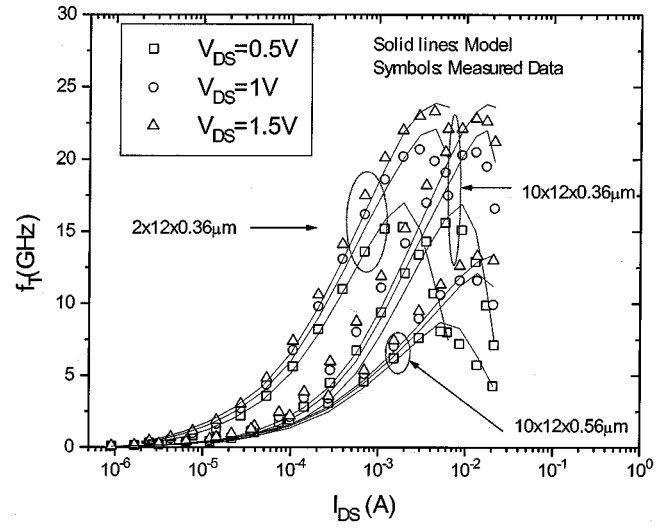


Fig. 3. Comparison of f_T–I_D characteristics between the model and measurements for different devices.

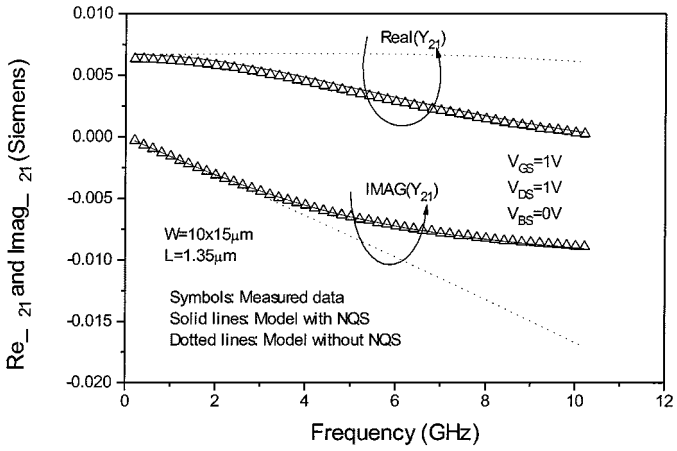


Fig. 4. y_{21} comparison of models with and without NQS effect and measured data for a NMOSFET with strong NQS effect.

A. Experimental Verification of Noise Predictivity of the RF Model

The HF noise sources in the RF model discussed above include the contributions from the terminal resistances. Fig. 5 shows a complete EC of the RF model with HF noise contributions. With the extracted parameters from the measured data for a 0.25 μm RF CMOS technology, we verify the noise characteristics of the RF model discussed above. The four noise parameters calculated by the correlation matrix technique (CMT) [15] from the simulated noise characteristics are given in Fig. 6 against the measured data for a 0.36 μm device at different bias conditions. In Fig. 6, the solid lines represent the simulation results of the RF model, and the symbols with solid squares and open circles are the measured data for $V_{\rm GS} = 1$ V and $V_{\rm DS} = 1$ V and for $V_{\rm GS} = 2$ V and $V_{\rm DS} = 1$ V, respectively. While the RF model with extracted parameters fits accurately the measured y-parameters data as shown in previous section, it can also predict the HF noise characteristics of the device as given in Fig. 6. It has been found that the transconductance and trancapacitances are the key components determining the HF noise characteristics besides the resistive components. For a model to predict well the HF noise characteristics, the accuracy in both dc and AC fittings has to be ensured while the noise model itself is developed with the inclusion of important physical effects such as velocity saturation (VS) and hot carrier effects (HCE). In this RF model, the influence of the VS effect has been included in the core model; however, the contribution of the HCE to thermal noise is not considered even though the influence of impact ionization (and hence HCE) to the channel conductance has been incorporated in the dc model [7].

In Fig. 6, a discrepancy in R_n characteristics between the model and the measured data at $V_{\rm GS} = 2$ V has been found. Further investigations in both noise model and parameter extraction are needed to explore the reason. The inaccuracy in either dc or AC models can result in this discrepancy. However obvious disagreement in the simulated and measured imaginary part of y_{12} has been found at that bias condition so the discrepancy in R_n characteristics may be caused by the inaccuracy of the capacitance model in that operation regime since the contribution from the capacitive components to R_n becomes comparable to that from the transconductance at HF [15].

B. Direct Extraction of Channel Thermal Noise From Measured Data

As shown in Fig. 5, different noise sources associated with terminal resistances and channel resistance exist in a MOSFET. However, the noise generated from the channel resistance will play an increasingly important rule in the overall noise performance of the circuits at RF. Therefore, an accurate model for the channel thermal noise in a MOSFET is crucial for RF CMOS IC design. As we demonstrated in Fig. 6, models of the channel thermal noise are confirmed by the minimum noise figure $(\mathrm{NF}_{\min})$ of devices, which is calculated based on the measured thermal noise and the other simulated noise parameters with a help of a small signal model including all the noise sources in the circuit simulator. However, the accuracy of the small-signal model, the values of model parameters used in the simulation and the noise model itself will affect the simulated noise parameters. These factors make the verification of a noise model more difficult, even when accurate noise parameters are measured. Therefore, obtaining the channel thermal noise of MOSFETs directly from RF noise measurements and using it to verify the noise model are desirable in noise modeling.

It has been known that a noisy two-port may be represented by a noise-free two-port and two noise current sources, one at the input port (i_1) and the other at the output port (i_2). From the noisy two-port network theory, the power spectral density of i_2 can be obtained from [16]

$$\frac{\overline{|i_2|^2}}{\Delta f} = \overline{|u|}^2 \cdot |y_{21}|^2 = 4kTR_n|y_{21}|^2 \tag{8}$$

where k is the Boltzmann's constant, T is the absolute temperature, y_{21} is the transadmittance from port 1 to port 2 of the noise-free two-port, and R_n is the equivalent noise resistance, which is a resistance cascaded at the input port that will produce the same amount of noise power spectral density as i_2 does at the output port.

It is too complex to obtain any analytical solutions for the noise sources in the equivalent circuit shown in Fig. 5. How-

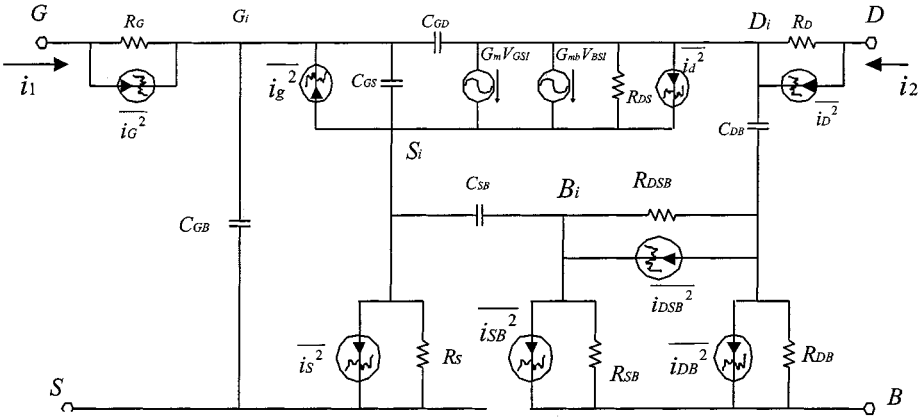
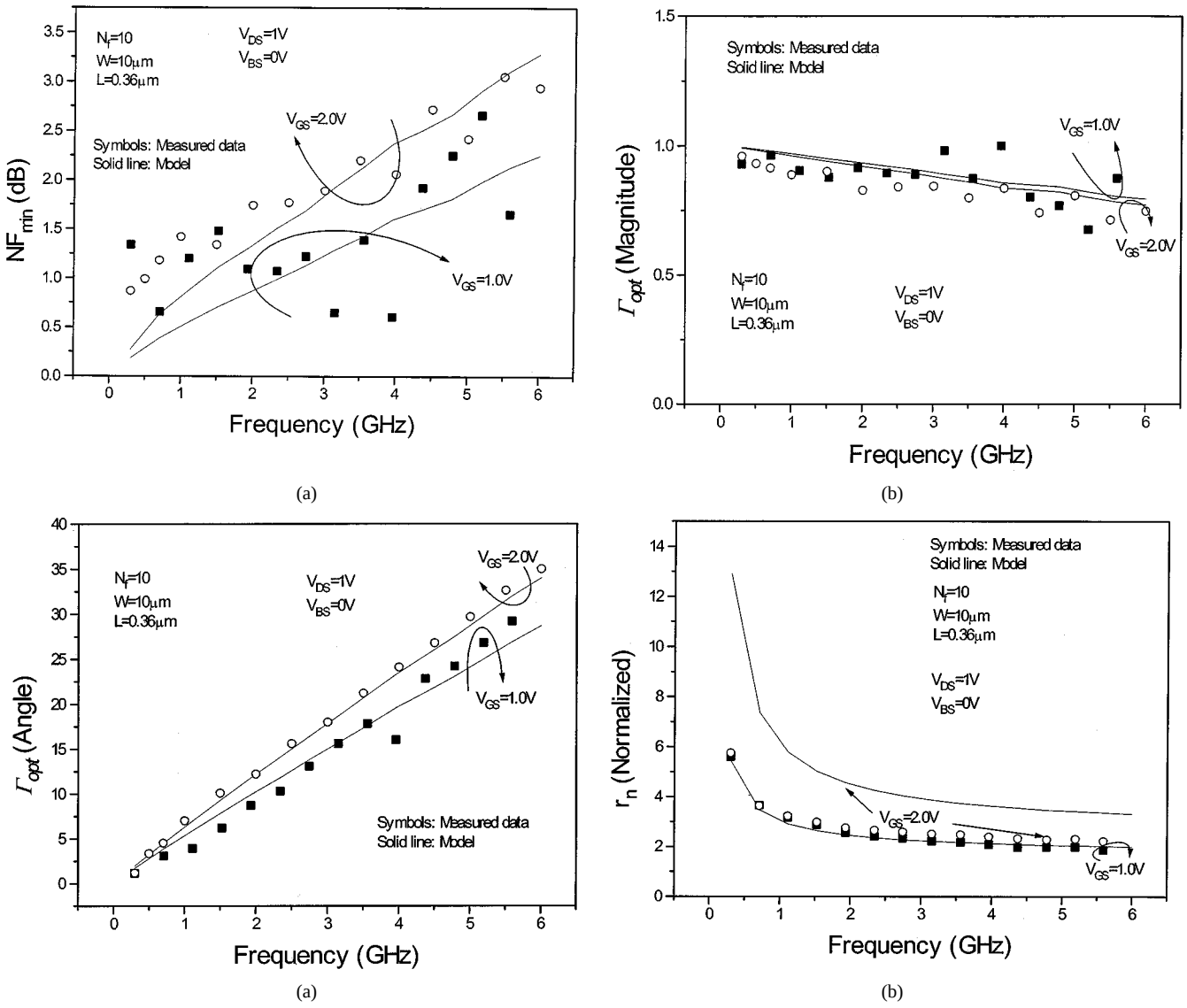


Fig. 5. An equivalent circuit to illustrate the noise sources in a MOSFET.



(a) (b)

(a) (b)

Fig. 6. (a) Comparisons of measured data for minimum noise figure $\mathrm{NF}_{\min}$ with simulations at different bias conditions. The N_f is the finger number of each device. The channel width per finger is 10 μm and channel length is 0.36 μm; (b) comparisons of measured data for the magnitude of the optimized source reflection coefficient G_{opt} with simulations at different bias conditions; (c) comparisons of measured data for the phase of the optimized source reflection coefficient Γ_{opt} with simulations at different bias conditions; and (d) comparisons of measured data for the noise resistance normalized to 50 Ω, r_n, with simulations at different bias conditions.

ever, assuming that all the capacitors in Fig. 5 are open-circuited, that is, all the admittances of the capacitors are approximately zero at low frequencies (above the corner frequency of the flicker noise), the equivalent noise model can be sim-

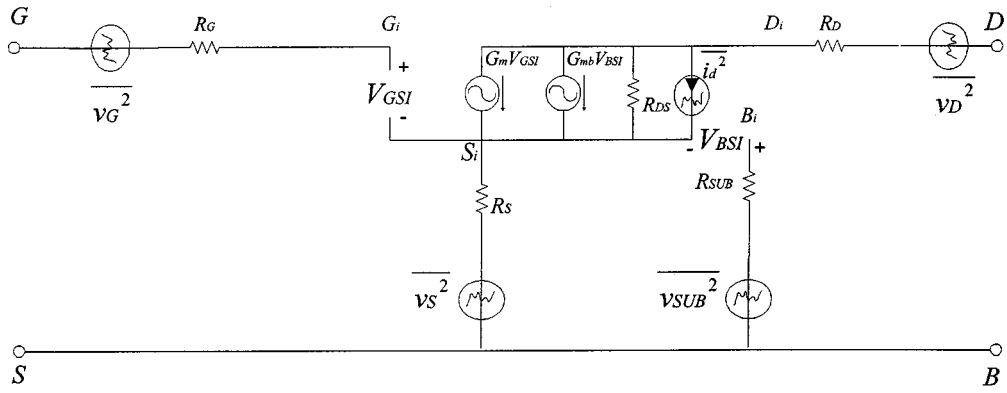


Fig. 7. Simplified equivalent circuit with noise sources at dc or lower frequency.

plified to that shown in Fig. 7 by converting the noise current sources associated with the parasitic resistances to noise voltage sources. The power spectral density of the noise current source i_2 defined in Fig. 5 can be given by

$$\frac{\overline{|i_2|^2}}{\Delta f} = \frac{\overline{|i_{G\,\mathrm{out}}|^2}}{\Delta f} + \frac{|i_{S\,\mathrm{out}}|^2}{\Delta f} + \frac{|i_{D\,\mathrm{out}}|^2}{\Delta f} + \frac{|i_{\mathrm{Subout}}|^2}{\Delta f} + \frac{|i_{d\,\mathrm{out}}|^2}{\Delta f} \quad (9)$$

where $i_{G\,\mathrm{out}}, i_{S\,\mathrm{out}}, i_{D\,\mathrm{out}}$ i_{Subout}, and $i_{d\,\mathrm{out}}$ are the noise currents contributed at the output port by gate resistance (R_G), source and drain resistances (R_S and R_D), the substrate resistance (R_{sub}), and the channel thermal noise (i_d), respectively.

By calculating the noise contribution from each noise source analytically according to (8), we have the following expressions for $i_{G\,\mathrm{out}}, i_{S\,\mathrm{out}}$, $i_{D\,\mathrm{out}}$, and $i_{d\,\mathrm{out}}$

$$\frac{\overline{|i_{G\,\mathrm{out}}|^2}}{\Delta f} = 4kTR_G\left(\frac{G_mR_{\mathrm{DS}}}{G_mR_SR_{\mathrm{DS}} + R_D + R_S + R_{\mathrm{DS}}}\right)^2 \quad (10a)$$

$$\frac{\overline{|i_{D\,\mathrm{out}}|^2}}{\Delta f} = 4kTR_D\left(\frac{1}{G_mR_SR_{\mathrm{DS}} + R_D + R_S + R_{\mathrm{DS}}}\right)^2 \quad (10b)$$

$$\frac{\overline{|i_{S\,\mathrm{out}}|^2}}{\Delta f} = 4kTR_S\left(\frac{1+G_mR_{\mathrm{DS}}}{G_mR_SR_{\mathrm{DS}} + R_D + R_S + R_{\mathrm{DS}}}\right)^2 \quad (10c)$$

$$\frac{\overline{|i_{d\,\mathrm{out}}|^2}}{\Delta f} = \overline{|i_d|^2}\left(\frac{R_{\mathrm{DS}}}{G_mR_SR_{\mathrm{DS}} + R_D + R_S + R_{\mathrm{DS}}}\right)^2 \quad (10d)$$

Substituting $i_{G\,\mathrm{out}}, i_{S\,\mathrm{out}}, i_{D\,\mathrm{out}}$, and $i_{d\,\mathrm{out}}$ in (9), the power spectral density of the channel thermal noise in MOSFETs can be extracted according to the following equation:

$$\overline{|i_d|^2} = 4kT\left[(R_{n0} - R_G - R_S)G_m^2 - \frac{2G_mR_S}{R_{\mathrm{DS}}} - \frac{R_D + R_S}{R_{\mathrm{DS}}^2}\right] \quad (11)$$

where R_{no} is the equivalent noise resistance extrapolated at dc or low frequencies from the measured equivalent noise resistance R_n versus frequency characteristics. To facilitate the derivation earlier, the noise contribution from the substrate resistances is ignored, which is acceptable because of the "open-like" junction capacitances at dc or low frequency and much lower bulk transconductance G_{mb} compared with the transconductance G_m. Also, the induced gate noise (i_g) and its correlation with the channel thermal noise are negligible at low frequencies and are therefore neglected in above derivations.

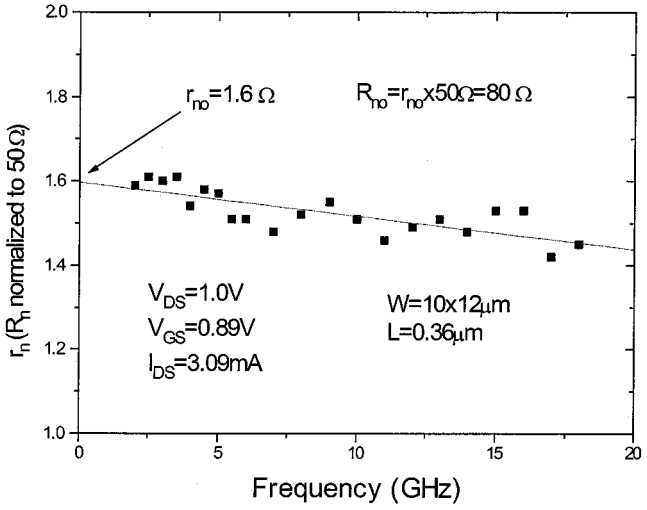


Fig. 8. Extraction of R_{no} from the measured characteristics of equivalent noise resistance versus frequency.

In order to obtain the model element values in (11), values of parameters R_G, R_S, R_D, G_m and R_{DS} are extracted from the measured S-parameters. Furthermore, R_{no} in (11) can be extracted by extrapolating the R_n versus frequency characteristics shown in Fig. 8 at low frequency. In Fig. 8, it shows that $R_{\mathrm{no}} = 80\,\Omega$ for this bias condition. Based on these extracted parameters and (11), the channel thermal noise can be calculated from the measured HF noise characteristics. Together with the extracted HF AC noise parameters, it can be used to verify the noise predictive capability of models available in circuit simulation.

C. Verification of Different Noise Models

The noise characteristics of several noise models including the subcircuit RF model discussed above are verified with the extracted channel thermal noise with the discussed methodology to explore the physical nature and accuracy of

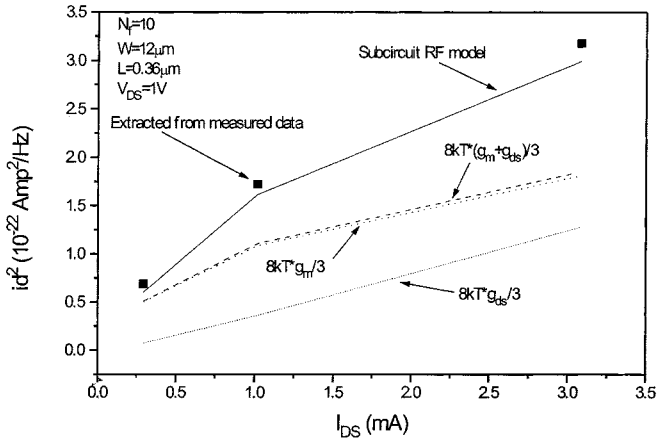


Fig. 9. Power spectral densities of channel thermal noise versus bias current of a 0.36 μm n-channel MOSFET. They are extracted from the measured data and calculated from different channel thermal noise models.

the models. Fig. 9 shows the curves of the channel thermal noise versus bias current, from the measured data, and simulations of the RF model and several other noise models. It shows that the calculated channel thermal noise based on the equation $i_d^2 = 8kTG_m/3, i_d^2 = 8kTG_{\rm ds}/3$, and $i_d^2 = 8kT(G_m + G_{\rm ds})/3$, where $G_{\rm ds}$ is the channel conductance, cannot predict the channel thermal noise extracted from measured data. The noise prediction of this subcircuit RF model has much better accuracy at the given bias conditions.

D. Induced Gate Noise

The concept of the induced gate noise has been introduced for three decades [17], [18]. This noise current can be modeled by a noisy current source connected in parallel to the intrinsic gate-to-source capacitance $C_{\rm GSi}$ [10]. Since the physical origin of the induced gate noise is the same as for the channel thermal noise at the drain, the two noise sources are partially correlated with a correlation factor [20]. Currently, the induced gate noise and moreover its correlation to the thermal noise at the drain is not yet implemented completely in compact models yet. One reason is due to the difficulty of modeling the induced-gate noise and implementing it in circuit simulators. Another reason is that it is not very critical at frequencies much smaller than the f_T of the device, since at that frequency range two more important contributors to the total noise are the substrate and the gate resistances, instead of the induced gate noise, besides the channel thermal noise. The methodology to extract the induced gate noise has also been developed [20], [21], however, further detailed investigations are needed to understand the induced gate noise issue and model it correctly. The RF model discussed in this paper does not include the contribution of the induced gate noise.

IV. Summary

In this paper, we have discussed both AC and noise modeling of MOSFETs for RF applications. The modeling of parasitic components in MOSFETs is crucial to describe the HF behavior of MOS devices operated at GHz frequency. An accurate RF MOSFET model with a simple substrate network is presented. The model has been verified by high frequency measurements. Good model accuracy at different bias conditions has been found for devices with different channel lengths, widths and fingers. The modeling approaches of NQS effects have been discussed. The discussed RF model can predict the y_{21} characteristics of devices with significant NQS effect.

The HF noise modeling is also discussed. The predictivity of HF noise characteristics of the RF model has been examined with the measured data. It shows that the model can predict the HF noise characteristics while the model with extracted parameters can simulate accurately the HF AC parameters. A methodology of extracting the channel thermal noise parameters is introduced, with which the validity of channel thermal noise model in a RF model can be examined. The results of several noise models are shown with the comparisons to the measured data. The subcircuit RF model gives better prediction of HF channel noise characteristics. The concept of the induced gate noise is briefly introduced without further theoretical analysis and experimental investigation. It is still an issue to model the induced gate noise, the correlation with channel thermal noise and its influence to the circuits at RF.

References

[1] W. Liu, R. Gharpurey, M. C. Chang, U. Erdogan, R. Aggarwal, and J. P. Mattia, "R. F. MOSFET modeling ac-counting for distributed substrate and channel resistances with emphasis on the BSIM3v3 SPICE model," in *IEDM Tech. Dig.*, Dec. 1997, pp. 309–312.

[2] D. R. Pehlke, M. Schroter, A. Burstein, M. Matloubian, and M. F. Chang, "High-frequency application of MOS compact models and their development for scalable RF MOS libraries," *Proc. IEEE Custom Integrated Circuits Conf.*, pp. 219–222, 1998.

[3] J.-J. Ou, X. Jin, I. Ma, C. Hu, and P. Gray, "CMOS RF modeling for GHz communication IC's," in *Proc. VLSI Symp. Technology*, Honolulu, HI, June 1998.

[4] S. H. Jen, C. Enz, D. R. Pehlke, M. Schroter, and B. J. Sheu, "Accurate MOS transistor modeling and parameter extraction valid up to 10-GHz," in *Proc. European Solid-State Device Research Conf.*, Bordeaux, France, Sept. 1998, pp. 484–487.

[5] Y. Cheng, M. Schroter, C. Enz, M. Matloubian, and D. Pehlke, "RF modeling issues of deep-submicron MOS-FET's for circuit design," *Proc. IEEE Int. Conf. Solid-State and Integrated Circuit Technology*, pp. 416–419, Oct. 1998.

[6] X. Jin, J.-J. Ou, C.-H. Chen, W. Liu, M. J. Deen, P. R. Gray, and C. Hu, "An effective gate resistance model for CMOS RF and noise modeling," in *IEDM Tech. Dig.*, Dec. 1998, pp. 961–964.

[7] Y. Cheng, M. Chan, K. Hui, M. Jeng, Z. Liu, J. Huang, K. Chen, P. Ko, and C. Hu, BSIM3v3.1 User's Manual, Univ. California, Berkeley, 1997. Memo. UCB/ERL M97/2.

[8] Y. Cheng and M. Matloubian, "High frequency characterization of gate resistance in MOSFETs," *IEEE Electron Device Lett.*, vol. 22, pp. 98–100, Feb. 2001.

[9] P. H. Ladbrooke, *MMIC design: GaAs FET's and HEMTs*. Norwood, MA: Artech House, 1989, ch. 6.

[10] C. Enz and Y. Cheng, "MOS transistor modeling for RF IC design," *IEEE J. Solid-State Circuits*, vol. 35, pp. 186–201, Feb. 2000.

[11] Y. Cheng and M. Matloubian, "On the high frequency charateristics of substrate resistance in RF MOSFETs," *IEEE Electron Device Lett.*, vol. 21, pp. 604–606, Dec. 2000.

[12] M. C. A. M. Koolen, J. A. M. Geelen, and M. P. J. G. Verleijen, "An improved de-embedding technique for on-wafer high-frequency characterization," in *IEEE Proc. Bipolar Circuit and Technology Meeting*, Minneapolis, MN, 1991, pp. 188–191.

[13] C. H. Chen and M. J. Deen, "High frequency noise of MOSFET's I: Modeling," *Solid-State Electron.*, vol. 42, pp. 2069–2081, Nov. 1998.

[14] Y. Tsividis, *Operation and Modeling of the MOS Transistor*, 2nd ed. New York: McGraw–Hill, 1999.

[15] G. D. Vendelin *et al.*, *Microwave Circuit Design Using Linear and Nonlinear Techniques*. New York: Wiley, 1990.

[16] C. H. Chen, M. J. Deen, M. Matloubian, and Y. Cheng, "Extraction of channel thermal noise of MOSFETs," in *Int. Conf. Microelectrics Test Structures (ICMTS)*, 2000, pp. 42–47.
[17] H. E. Halladay and A. Van der Ziel, "On the high frequency excess noise and equivalent circuit representation of the MOSFET with n-type channel," *Solid-State Electron.*, vol. 12, pp. 161–176, 1969.
[18] D. P. Triantis, A. N. Birbas, and S. E. Plevridis, "Induced gate noise in MOSFET's revisited: The submicron case," *Solid-State Electron.*, vol. 41, no. 12, pp. 1937–1942, 1997.
[19] D. K. Shaeffer and T. H. Lee, "A 1.5-V, 1.5-GHz CMOS low-noise amplifier," *IEEE J. Solid-State Circuits*, vol. 32, pp. 745–759, May 1997.
[20] C. H. Chen, M. J. Deen, M. Matloubian, and Y. Cheng, "Extraction of the induced gate noise, channel thermal noise and their correlation in sub-micron MOSFET's from RF noise measurements," *Proc. IEEE Int. Conf. Microelectronic Test Structures*, Mar. 2001.
[21] C. H. Chen, M. J. Deen, Y. Cheng, and M. Matloubian, "Extraction of the induced gate noise, channel noise and their correlation in sub-micron MOSFET's from RF noise measurements," *IEEE Trans. Electron Devices*, vol. 48, pp. 2884–2892, Dec. 2001.

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