EE2CI5 LAB 3b

Square wave oscillator circuit

Objective

The objective of this lab is to use a 555 integrated circuit, a capacitor and some resistors to design a periodic square wave oscillator with period 1ms and a duty cycle of 2/3; i.e., the oscillator output voltage is "high" for 2/3ms and is then "low" for 1/3ms.

Equipment:

1) Function generator
2) Digital oscilloscope

Components:

1) Resistors: one each of 330 Ω, 680 Ω, 4.7kΩ, 1kΩ, 10kΩ and 20kΩ
2) Capacitors: one 0.1 μF,
3) 555 timer chip

1. 555 Timer

The "555 Timer" is an integrated circuit that can be used to construct circuits that implement a variety of different timing functions. Several different manufacturers make 555 chips, and each has a slightly different implementation. However, the external configuration remains the same. The 555 chip comes in an 8-pin Dual Inline Package (DIP). The dot on the top of the package marks pin 1. The remaining pins are numbered sequentially in a counterclockwise direction from pin one. In Figure 1 the pins have been labeled with their functions.

Figure 1: The pins of a 555 chip.
(Figure sourced from www.wikipedia.org/wiki/555_timer_IC)

Pins 1, 4, 5 and 8 are typically used to establish the operation of the chip, where as Pins 2 and 6 are the operational inputs and Pins 3 and 7 are the operational outputs. Here are some brief descriptions of their characteristics.

- Pin 1 (GND): to be connected to ground. This is the "low" voltage level.
- Pin 8 (VCC): to be connected to a positive DC voltage source, typically between 3 and 15 volts. The value of the voltage at this pin establishes the "high" voltage level.
- Pin 4 (RESET-bar): When set to "low" this turns off the chip. When set to "high" the chip is turned on.
- Pin 5 (CTRL): Used to control the comparison signal for the threshold input.
- Pin 7 (DIS): This is one of the controlled outputs. One way to picture the operation of Pin 7 is to think of there being a switch between this pin and the ground. (The switch is implemented using a transistor.) When the operation of the timer (see the table below) is such that this switch is turned on, there is a low-resistance path from Pin 7 to the ground. In effect Pin 7 is connected to the ground. When this switch is off, the path from Pin 7 to the ground has a very high resistance, and essentially no current will flow into or out of this pin.
- Pin 3 (OUT): This is the main output of the chip. The voltage on this pin is either the "high" voltage or the "low" voltage, and the goal of circuit design using the 555 timer is to manipulate this output to obtain the desired effects.
- Pin 2 (TRIG) and Pin 6 (THR): The inputs to these two pins control the operation of the circuit (when the input at Pin 4 is "high" so that the chip is turned on). As will be seen in the functional circuit diagram below, these inputs are connected to the inputs of comparator circuits. Since comparators have high input resistance, the current drawn by these two input pins is usually negligible.

The functional operation of the 555 timer can be succinctly captured in the Table 1. As you can see from this table, when the chip is switched on, the voltage level of the output and the state of the discharge switch depend on the voltages applied to the TRIG and THR pins.

Table 1: Functional operation of a 555 chip.
(Source: Texas Instruments Data Sheet for NA555, NE555, SA555, SE555. Revised June 2010.)

RESET-bar (4)	TRIG (2)	THR (6)	OUT (3)	DIS (7)
Low	Irrelevant	Irrelevant	Low	On
High	< VCC/3	Irrelevant	High	Off
High	> VCC/3	> 2VCC/3	Low	On
High	> VCC/3	< 2VCC/3	As previously established	As previously established

To give you some idea of how this functionality is realized in a circuit, the functional circuit layout of one implementation of the 555 chip is given in Figure 2.

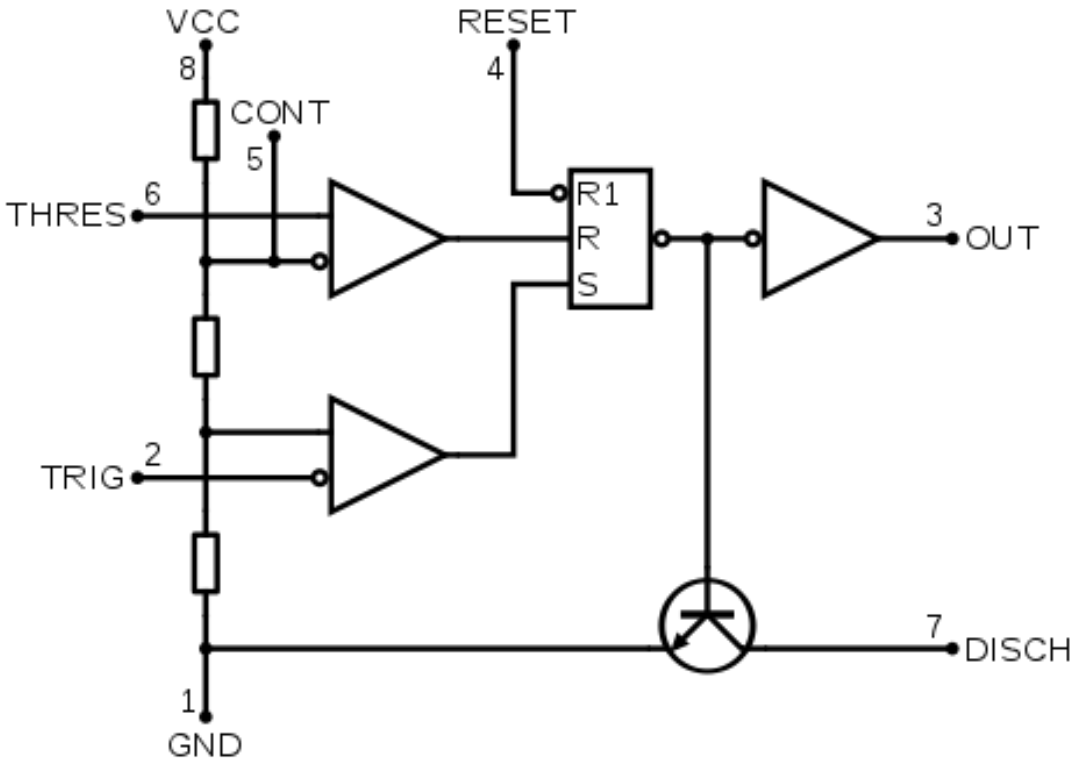


Figure 2: Functional circuit layout of a 555 chip.
Note the slightly different labels for Pins 6 and 7.
In order to be consistent with Figure 1, the label of Pin 4 ought to be RESET-bar.
(Figure sourced from www.wikipedia.org/wiki/555_timer_IC)

Some of the features of this layout are as follows:

- The three rectangles on the VCC to GND path represent resistors of (nominally) equal value. Therefore, it is quite straightforward to calculate the (nominal) voltages at the nodes at which these resistors are connected. (*Hint:* use voltage division.)
- The two triangles just to the right of these resistors are comparators. The circled input can be considered as the reference voltage. When the voltage at the other input is below the reference voltage, the comparator output is low. When the voltage at the other input is above the reference voltage, the comparator output is high.
- The block with inputs labeled R1, R and S is an RS flip-flop, and the output is the complement of the state of the flip-flop. In this circuit, the flip-flop is use to store some the important transient outputs from the comparators. The operation of the flip-flop is described Table 2.
- The element in the path from the flip-flop to the output is an inverter. When the input is low, the output is high, and vice versa.
- The transistor in the path between the DISCH pin (7) and the ground is turned on if the output of the flip-flop is high, and is turned off when the output of the flip-flop is low.

Table 2: Functional operation of an enabled RS flip-flop, with the output being the complement of the state. [The (High,High) input pair gives rise to an undesirable race condition, and is to be avoided.]

Voltage at S	Voltage at R	Output, Q-bar
Low	Low	Retain the current output
Low	High	Set Q-bar to high
High	Low	Set Q-bar to low

2. Pre-lab Part I: Understanding 555 chip in Astable mode (3 marks)

We will use the 555 chip in the Astable mode, which is illustrated in Figure 3.

The first part of your prelab is to sketch the waveforms of the important signals in the circuit, including some of those inside the 555 chip. Your sketches should all have the same time scale and should be aligned underneath each other. That way you can follow how events in one part of the circuit trigger events in the other parts. You should sketch

- the capacitor voltage in volts,
- the "R" input to the flip-flop, in terms of "low" or "high" voltage levels. Note that it will only be "high" for a short period of time.
- the "S" input to the flip-flop; "low" or "high". Note that with the exception of the initial charge up period, it will only be "high" for a short period of time.
- the output of the flip-flop "Q-bar"; "low" or "high"
- the state of the discharge "switch"; "on" or "off"
- the voltage at the output (pin 3); "low" or "high"

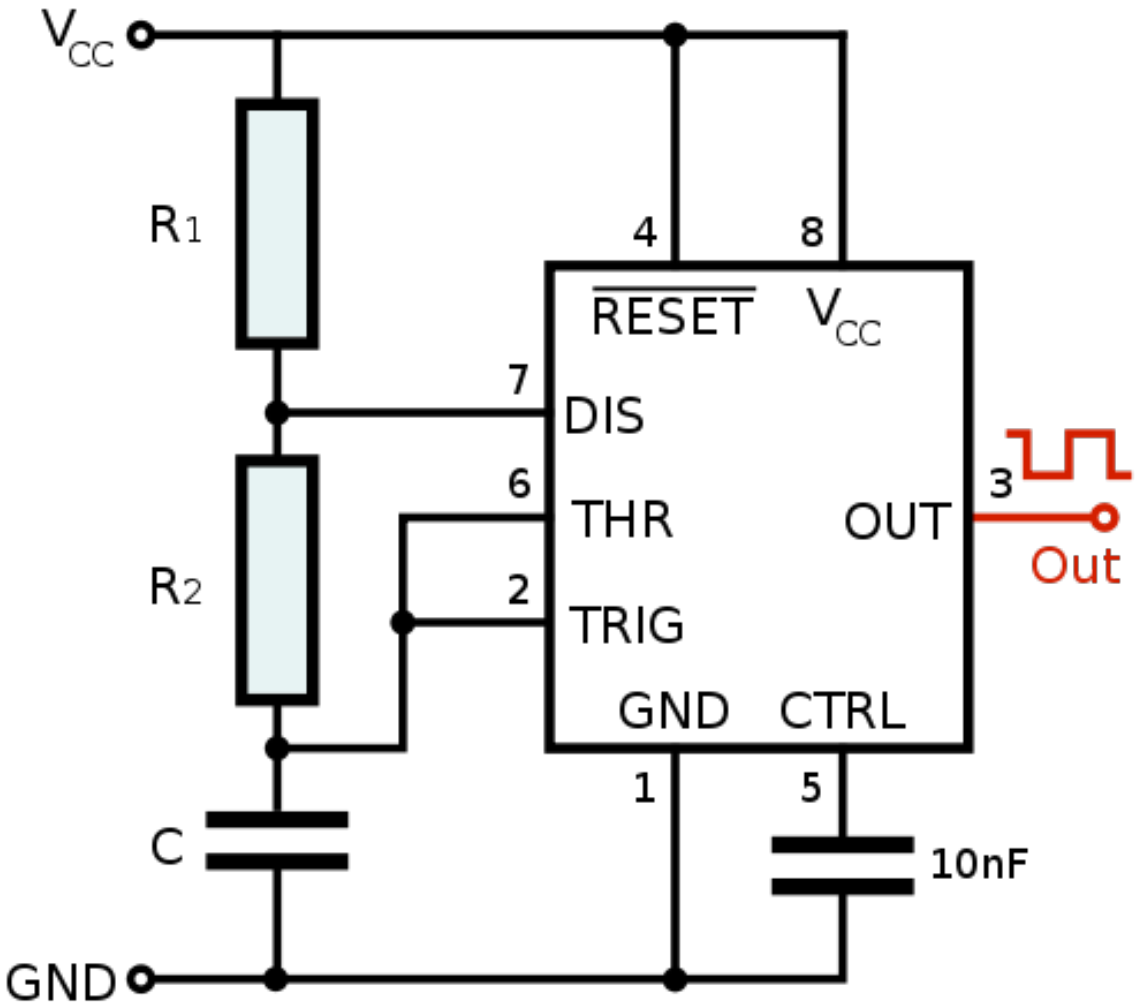
To help you make these sketches, consider the following description of the circuit.

- When the power supply is first turned on, the capacitor voltage is zero and the power supply (VCC) charges up the capacitor through R1 and R2. Since the comparator inputs draw very little current, the circuit looks like a single loop with a voltage source VCC, a resistor of value R1+R2, and the capacitor C. Be sure to consider the time constant of the charging of the capacitor.
- The capacitor continues to charge until the "THRES" comparator is turned on. That changes the flip-flop output so that Q-bar is high, and hence the discharge "switch" is turned on. At that point, the equivalent circuit "seen" by the capacitor is simply a resistor of value R2 connected to the ground. Therefore, the capacitor will begin to discharge. When sketching the capacitor voltage waveform, think carefully about the

time constant relative to the time constant of the circuit in the previous phase. Also, think carefully about the length of time that the "THRES" comparator is turned on, and how long the flip-flop output Q-bar remains high.

- The capacitor continues to discharge until the "TRIG" comparator is turned on. That changes the flip-flop output so that Q-bar is low, and hence the discharge switch is turned off. Therefore, the capacitor begins to charge again through a circuit consisting of a voltage source VCC and an equivalent resistor of value R1+R2. Again, think carefully about the time constants, and the length of time that the "TRIG" comparator is turned on, and how long the flip-flop output Q-bar remains low.

Figure 3: 555 timer configured in Astable mode.
Note, in our experiments we will not connect the 10nF capacitor to pin 5.



3. Pre-lab Part II: Circuit Design (3 marks)

Design an Astable circuit using the 555 chip so that the waveform on output pin 3 is a periodic square wave that is high for 0.667ms and low for 0.333ms.

Carefully explain your design procedure, using your waveform sketches and time constant computations.

Note: Ideally, the timing values are independent of the supply voltage. However, in practice this is not necessarily so. The use of a 9V power supply is recommended.

4. Experiment (2 marks)

Build your circuit and compare your predicted theoretical response with your measured response.

5. Report (2 marks)

Summarize the outcomes of your design and experiment, and suggest an application for the circuit te up your