ELEC ENG 4CL4:

Control System Design

Notes for Lecture #31

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Minimum Time Dead-Beat Control

The basic idea in dead-beat control design is similar to that in the minimal prototype case: to achieve zero error at the sample points in a finite number of sampling periods for step references and step output disturbances (*and with zero initial conditions*). However, in this case we add the requirement that, for this sort of reference and disturbance, the controller output $u[k]$ also reach its steady state value in the same number of intervals.

The design involves cancelling the open loop poles in the controller. Thus, the system is (*for the moment*) assumed to be stable. We see that the result is achieved by the following control law

$$C_q(z) = \frac{\alpha A_{0q}(z)}{z^n - \alpha B_{0q}(z)}; \quad \alpha = \frac{1}{B_{0q}(1)}$$

The resulting closed loop complementary sensitivity function is

$$T(z) = \frac{C_q(z) G_{0q}(z)}{1 + C_q(z) G_{0q}(z)} = \frac{\alpha B_{0q}(z)}{z^n}$$

Example

Consider the servo system

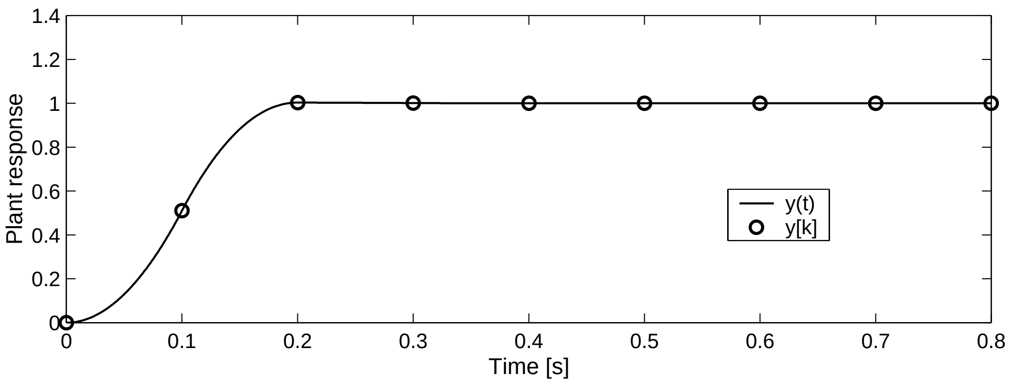
$$G_o(s) = \frac{1}{s(s+1)}$$

Synthesize a minimum time dead-beat control with sampling period $\Delta = 0.1[s]$.

$$C_q(z) = \frac{\alpha A_{0q}(z)}{z^n - \alpha B_{0q}(z)} = \frac{105.49z - 95.47}{z + 0.4910}$$

The next slide shows the simulated response.

Figure 13.7: *Minimum time dead-beat control for a second order plant*



From the above result we see that the intersample problem has been solved by the dead-beat control law.

Note, however, that this is still a very wide-bandwidth control law and thus the other problems discussed in the slides for Chapter 12 (*i.e. noise, input saturation and timing jitter issues*) will still be a problem for the dead-beat controller.

The controller presented above has been derived for stable plants or plants with at most one pole at the origin. Thus cancellation of $A_{0q}(z)$ was allowed. However, the dead-beat philosophy can also be applied to unstable plants, provided that dead-beat is attained in more than n sampling periods. To do this we simply use pole assignment and place all of the closed loop poles at the origin.

Indeed, dead-beat control is then seen to be simply a special case of general pole-assignment. We study the general case below.

Digital Control Design by Pole Assignment

Minimal prototype and dead-beat approaches are particular applications of pole assignment. Indeed, all can be derived by solving the usual pole assignment equation:

$$A(q)L(q)+B(q)P(q)=A_{cl}(q)$$

for particular values of $A_{cl}(q)$.

The general pole assignment problem is illustrated below.

Example

Consider a continuous time plant having a nominal model given by

$$G_o(s) = \frac{1}{(s+1)(s+2)}$$

Design a digital controller, $C_q(z)$, which achieves a loop bandwidth of approximately 3[rad/s]. The loop must also yield zero steady state error for constant references.

We first use the MATLAB program ***c2del.m*** to obtain the discrete transfer function in delta form representing the combination of the continuous time plant and the zero order hold mechanism. This yields

$$\mathcal{D}\left\{G_{ho}(s)G_o(s)\right\} = \frac{0.0453\gamma + 0.863}{\gamma^2 + 2.764\gamma + 1.725}$$

We next choose the closed loop polynomial $A_{cl\delta}(\gamma)$ to be equal to

$$A_{cl\delta}(\gamma) = (\gamma + 2.5)^2(\gamma + 3)(\gamma + 4)$$

The resulting pole assignment equation has the form

$$(\gamma^2 + 2.764\gamma + 1.725)\gamma\overline{L}_\delta(\gamma) + (0.0453\gamma + 0.863)P_\delta(\gamma) = (\gamma + 2.5)^2(\gamma + 3)(\gamma + 4)$$

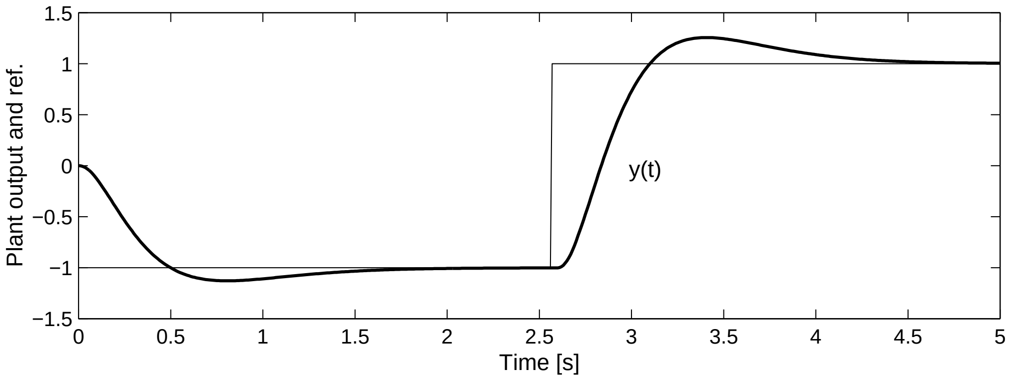
The MATLAB program ***paq.m*** is then used to solve this equation, leading to $C_\delta(\gamma)$, which is finally transformed into $C_q(z)$. The delta and shift controllers are given by

$$C_\delta(\gamma) = \frac{29.1\gamma^2 + 100.0\gamma + 87.0}{\gamma^2 + 7.9\gamma} = \frac{P_\delta(\gamma)}{\gamma \overline{L}_\delta(\gamma)} \qquad \text{and}$$

$$C_q(z) = \frac{29.1z^2 - 48.3z + 20.0}{(z-1)(z-0.21)}$$

Finally, the closed loop response is as shown on the next slide.

Figure 13.8: *Performance of digital control loop*



Summary

- There are a number of ways of designing digital control systems:
  - design in continuous time and discretize the controller prior to implementation;
  - model the process by a digital model and carry out the design in discrete time.
- Continuous time design which is discretized for implementation:
  - Continuous time signals and models are utilized for the design;
  - Prior to implementation, the controller is rep0laced by an equivalent discrete time version;
  - Equivalent means to simply map s to δ (where δ is the delta operator);

- Caution must be exercised since the analysis was carried out in continuous time and the expected results are therefore based on the assumption that the sampling rate is high enough to mask sampling effects;
- If the sampling period is chosen carefully, in particular with respect to the open and closed loop dynamics, then the results should be acceptable.

❖ Discrete design based on a discretized process model:

- First the model of the continuous process is discretized;
- Then, based on the discrete process, a discrete controller is designed and implemented;
- Caution must be exercised with so called intersample behavior: the analysis is based entirely on the behavior as observed at discrete points in time, but the process has a continuous behavior also between sampling instances;

- Problems can be avoided by refraining from designing solutions which appear feasible in a discrete time analysis, but are known to be unachievable in a continuous time analysis (such as removing non-minimum phase zeros from the closed loop!).

❖ The following rules of thumb will help avoid intersample problems if a purely digital design is carried out:

- Sample 10 times the desired closed loop bandwidth;
- Use simple anti-aliasing filters to avoid excessive phase shift;
- Never try to cancel or otherwise compensate for discrete sampling zeros;
- always check the intersample response.