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Wafer Level Surface Activated Bonding Tool for MEMS Packaging

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A wafer level surface activated bonding (SAB) tool has been developed for microelectromechanical systems (MEMS) packaging at low temperature. The tool accommodates 8 in. diam wafers. The principle features of the tool are the automatic parallel adjustment for 8 in. wafers to a margin of error within ± 1 μm and the *X*, *Y*, and θ axis alignments with an accuracy of ± 0.5 μm. We have approached a new integration technique for the integration of ionic crystals with transparent and nontransparent thin intermediate layers using this tool. Various sizes of patterned and bare silicon, Al silicate glass, and quartz wafers cleaned by a low energy argon ion source in a vacuum have been successfully bonded by this technique at low temperature. Radioisotope fine leak and vacuum seal tests of sealed silicon cavities show leak rates of 1.0×10^{-9} and 2.6×10^{-16} Pa/m^3 s, respectively, which are lower than the American military standard encapsulation requirements for MEMS devices in harsh environments. Void-free interfaces with bonding strengths comparable to bulk materials are found. Low adhesion between SAB-processed ionic crystals without adhesive layers is believed to be due to radiation-induced discontinuous polarization.
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The surface activated bonding (SAB) process is a solid-state bonding process in which two or more smooth surfaces are cleaned by using either an argon fast atom beam (Ar-FAB), an Ar ion beam, or a radio frequency (rf) plasma in an ultrahigh vacuum (UHV) followed by contact, which results in strong adhesion between the mated surfaces.[1] The driving forces of the SAB process are the integration potential at room or low temperature, which eliminates thermal mismatch problems, and the production of electrically and microstructurally useful interfaces with bonding strengths comparable to bulk materials. Therefore, the SAB process can be a packaging solution for three-dimensional (3D) integration of multifunctional materials to achieve high density and multifunctional devices at low total packaging costs. Generally, direct-bonded wafers need to be annealed in order to increase bonding strength, and the interfaces have voids for specific activation treatments unless annealed at high temperatures (~1000 K).[2,3] Voids may degrade device performance and reliability. In fact, microelectromechanical systems (MEMS) may contain temperature-sensitive active and passive devices, therefore a low-temperature integration technique is highly desirable. In addition, as devices shrink, high precision aligned bonding is necessary for 3D integration. Furthermore, in order to protect MEMS devices from mechanical damage and harsh environmental affects, hermetic sealing of the devices is required.[4] However, gas formation due to high-temperature anneals in the cavities fabricated by direct wafer bonding techniques is a major concern.[5] Therefore, a high precision tool has been developed which eliminates these problems for MEMS applications.

The SAB approach has been found to be applicable in chip size and wafer level optoelectronic[6] and MEMS[7] packaging. This technique has already been successfully used to integrate various combinations of metals (Al, Cu, Ag, Au, Sn, and their alloys), semiconductors (Si, GaAs, InP, GaP, InAs, etc), and insulators (SiC, Al_2O_3, AlN, etc.). However, we have found low adhesion between ionic crystals like quartz, glass wafers, and other materials. In order to improve interfacial strength between Si, quartz, and Al silicate glass wafers, thin adhesive layers termed as transparent (a few nanometers) and nontransparent (a few hundred nanometers) layers, were prepared on glass and quartz wafers by depositing Fe and Au/Ti. Nevertheless for certain applications, it is very important to maintain the ultraviolet (UV) transparency behavior of quartz after bonding. This article reports on the development of a wafer level bonding tool with submicrometer alignment accuracy for MEMS packaging including bonding results of Si, and ionic crystalline Al silicate glass, and quartz wafers using UV and non-UV transparent intermediate layers. The bonding results include the interfacial strength measurements by tensile pulling tests, vacuum sealing behavior of cavities, and the microstructure of the interfaces.

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Development of the SAB Tool

Structure and features.—Figure 1 shows the schematic diagram of a wafer level robot controlled SAB tool. It consists of a transfer chamber surrounded by processing, analyzing, heating, turning over/preliminary alignment (prealignment), alignment/preliminary bonding (prebonding), and bonding chambers.[8] A robot capable of handling 8 in. wafers is positioned in the transfer chamber, which has access to all chambers except the load lock. An Ar-FAB consists of two cells and a hollow cathode low energy Ar-ion beam source located in the processing chamber capable of etching at incidence angles of 25° and 90°, respectively. Both sources can etch over a surface area of 200 mm diam while the wafers are rotated to achieve homogeneous etching during sputtering. Highly efficient rotary pumps, turbomolecular pumps, as well as ion pumps used in the vacuum system are capable of decreasing the pressure to a high vacuum pressure ranging from 10^{-6} to 10^{-7} Pa. Baking heaters positioned inside and around all chambers can decrease the pressure from a high vacuum to an UHV pressure of 10^{-8} Pa. The processes

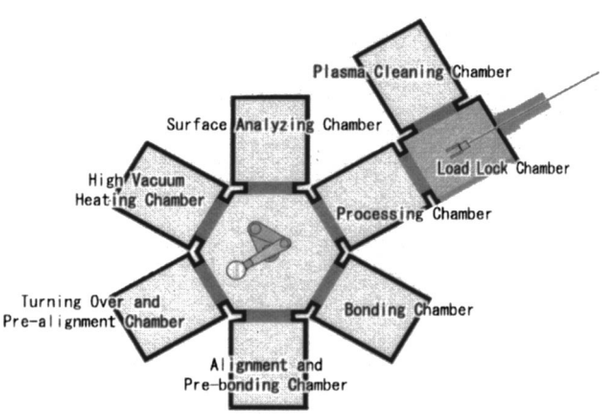

Figure 1. Schematic diagram of a robot controlled 8 in. wafer level SAB tool.[8]

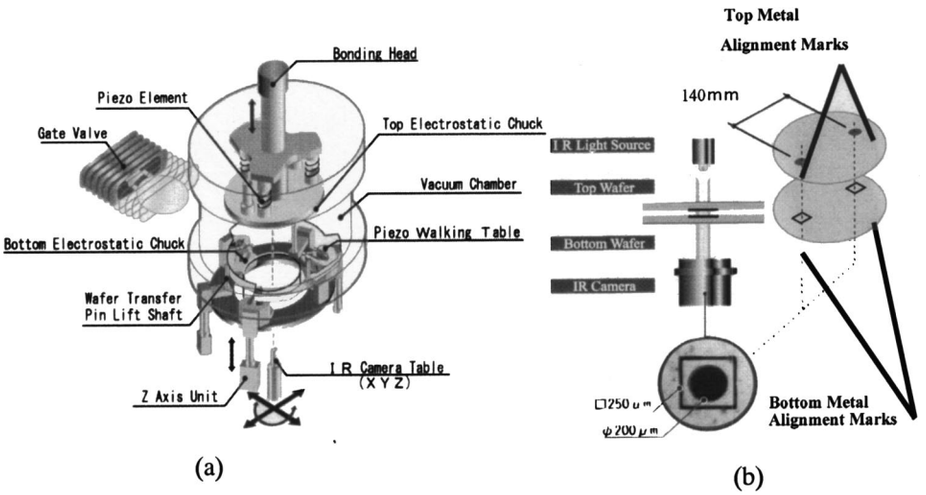

Figure 2. Schematic diagrams for (a) wafer alignment system and (b) infrared detection system.

from wafer activation to surface analysis to wafer alignment and bonding are accomplished without breaking UHV pressure.

The load lock chamber is connected to both the processing chamber and a plasma cleaning chamber in which Ar, N_2, CF_4, O_2, and H_2 plasma treatments are possible. A wafer is transferred from the load lock chamber to the processing chamber by mechanical insertion only. On the other hand, the wafer can be transferred automatically to each and all chambers by the robot. In fact, all controls such as the opening of gate valves, the leaking of chambers, and the turning over of wafers are controlled by pressing on a soft touch computer. The surface analyzing chamber is equipped with Auger electron spectroscopy (AES) and reflection high energy electron diffraction (RHEED). In addition, a charge-coupled device (CCD) camera is positioned across the window of each chamber for detecting the position of the wafer. A magnetron Cu sputtering deposition source of 1 kW power is equipped in the heating chamber. Wafers can either be annealed and/or sputter-deposited up to 800 K in an UHV.

In the turning over and prealignment chamber, wafer turn over and alignment can be performed with an accuracy of ± 0.2 mm. After analyzing the removal of native oxides or contaminants of the sputtered wafer surface, the wafer is first transferred from the transfer chamber to the turning over and prealignment chamber then placed on the table in the chamber and finally turned over by the mechanical chuck. Two pairs of glass windows on the upper and lower sides of the chamber are located on the top and bottom of the table. Two pairs of CCD cameras are vertically positioned to face each other on the glass windows to the upper and lower sides of the chamber in order to align the position of the wafer. Prealigned wafers are separately transferred to the alignment and prebonding chamber.

Alignment and position detection process.—High precision alignment with prebonding is performed in the alignment and prebonding chamber. The chamber is composed of electrostatic chucks that hold the top and bottom wafers, a piezo walking table that serves as the alignment table, a wafer transfer pin lift shaft, an infrared (IR) camera/table for the detection of alignment marks, and a bonding head as shown in Fig. 2. Three piezo elements attached to the bonding head and three *Z* axis units attached to the piezo walking table are used to perform the parallel adjustment function of the top and bottom wafers.

In this chamber, first the wafer carried by the robot is delivered on the wafer transfer pin, then the bonding head is lowered to the position of the pins on which the top wafer is placed, and finally the top wafer is held by activating the top electrostatic chuck. For the bottom wafer, the transfer pins are lowered together with the wafer, and the wafer is placed on the bottom electrostatic chuck, then this chuck is activated to hold the wafer. Next, the alignments of the top and bottom wafers are accomplished, which include three step-parallel adjustment, position detection, and alignment systems. As stated previously, three piezo elements installed on the bonding head serve as actuators for the top parallel adjustment. The three *Z* axis units mounted on the piezo walking table serve as actuators for the bottom parallel adjustment. The parallelism of the top and bottom wafers is detected through the height displacement of parallelism detection points at three *Z* axis units by means of the lower camera and is automatically adjusted through the operation of the top and bottom actuators, respectively. The height displacement at the three parallelism detection points converges relatively easily within ± 2 μm. A repetitive correction enables adjustment to less than ± 1 μm. Metallic alignment marks were previously formed on the top and bottom silicon wafers, and the top and bottom marks can be detected by transmitting an IR beam and observing through an IR camera (Fig. 2). The IR camera and light source are installed outside the chamber above and below the viewing parts. The alignment uses highly accurate image processing to recognize the position of the marks on the top and bottom wafers and to align the bottom wafer by means of the piezo walking table to the top wafer.

Figure 3 shows the data for eight measurements obtained from nine different alignments of the top and bottom wafers using the piezo walking table, starting with a shift of approximately 100 μm on *X*, *Y*, and θ, respectively. Two 140 mm pitch alignment marks were used on 8 in. wafers. Furthermore, as the piezo walking table is installed on a 190 mm pitch circle, we can see that a high level of

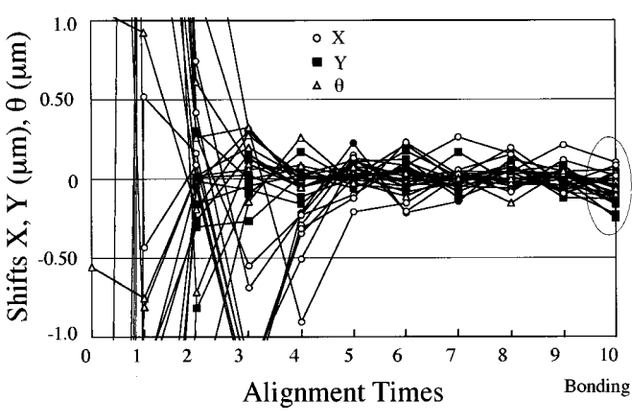

Figure 3. Alignment data for X, Y, and θ of top and bottom wafers using alignment marks.

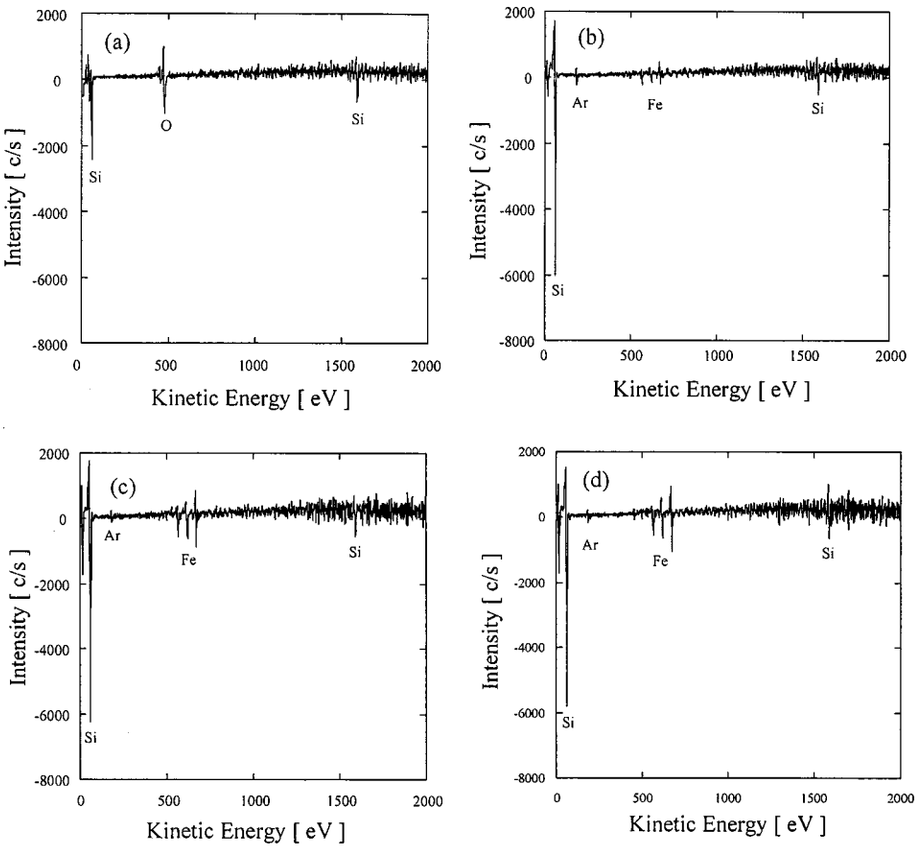

Figure 4. AES spectra for Si wafer (a) before, (b) after 1 min, (c) after 6 min, and (d) after 36 min irradiation with a modified Ar-low energy ion beam source of 80 eV and 3 A.

accuracy can also be obtained for θ. The results obtained showed an alignment accuracy within ±0.5 μm for *X*, *Y*, and θ (θ determines any shift in the outer mark position).

High alignment accuracy can also be maintained for the bonding. After alignment, bonding is performed by lowering the bonding head and using a pressure cylinder with a maximum pressure capacity of 500 N. The bonded wafers are transferred onto the wafer transfer pins again and discharged by means of the transfer chamber's transfer robot.

Bonding Experiments

Samples of mirror-polished single-crystalline silicon(100) wafers of 200 and 100 mm diameter with the respective thickness of 730 and 450 μm, Au 500 nm/Ti 200 nm deposited Al silicate glass wafer of 125 mm in diameter and 670 μm thick, and bare quartz wafers of 75 mm diam and 375 μm thick were used in this experiment. Samples, except Si/Au/Ti/Al silicate glass wafers, were cleaned with H_2SO_4 and H_2O_2 solution at 340 K followed by HF dip. The samples were then boiled in a solution of NH_4OH, H_2O_2, and H_2O at 340 K. The samples were rinsed in water after each chemical treatment. Finally, the samples were spun-dried. Si/Au/Ti/Al silicate glass wafers were cleaned with acetone and ethanol only. Three trays for holding 75, 100, and 125 mm sized wafers were prepared using a 200 mm Si wafer because the robot can only accommodate the 200 mm size wafer. Samples with smaller diameter than 200 mm were considered as the bottom sample, whereas the 200 mm Si samples were used as the top sample.

The wafers were loaded into the load lock chamber and then sputtered separately in the processing chamber by a hollow cathode low energy argon ion source (Mark II, Commonwealth Scientific Corp., Alexandria, VA, USA.) at an incident angle of 90° with a voltage of 80 V and an amperage of 3 A for 30-1800 s. The ion source was modified in order to sputter-deposit Fe with simultaneous sputter cleaning. The modification to the ion source was accomplished by covering a Fe ring on the hollow cathode surface. The accelerated ions in the discharged plasma have significant components in both the radial and axial directions.[9] The radial ions may sputter Fe from the Fe ring surface and deposit on the sample surface used for sputter cleaning. The top sample was turned over in the turning over and prealignment chamber and then transferred to the alignment and prebonding chamber. The bottom sample was directly transferred to the alignment and prebonding chamber after being sputtered in the processing chamber. Preliminary bonding was performed in the alignment and prebonding chamber under a load of 500 N. Later the preliminarily bonded wafers were transferred to the bonding chamber and cold rolled on the bonded wafers under a load of 1000-10,000 N. First, the load was applied to the middle of the wafers and then the roller (stainless steel) was shifted to the left and to the right from the middle. Some of the samples were annealed in the atmospheric pressure of air, and the annealing temperatures were noted in the specific results.

Results and Discussion

UV intermediate layers.—Surface analysis.—In order to maintain optically transparent wafers, we utilized a very thin layer of Fe as an adhesive layer for the integration of Si/Al silicate glass, Si/quartz, and quartz/quartz wafers. Fe was chosen because it is being used as one of the main impurities in device fabrication. Figure 4 shows a comparative AES analysis of the Si surface before and after sputtering with the Ar-ion source for 1, 6, and 36 min. Contaminants like native oxides disappeared even after a short sputtering time for 60 s. However, a low amount of Fe is detectable on the Si surface treated for 60 s, and Fe counts appear to be constant with the increase of sputtering time up to 2160 s (36 min).

An optically transparent quartz wafer integrated with single-crystalline Si is very attractive in image sensors and optical waveguides applications. Therefore it is very important to keep optical transparency of quartz wafers even after sputter cleaning and

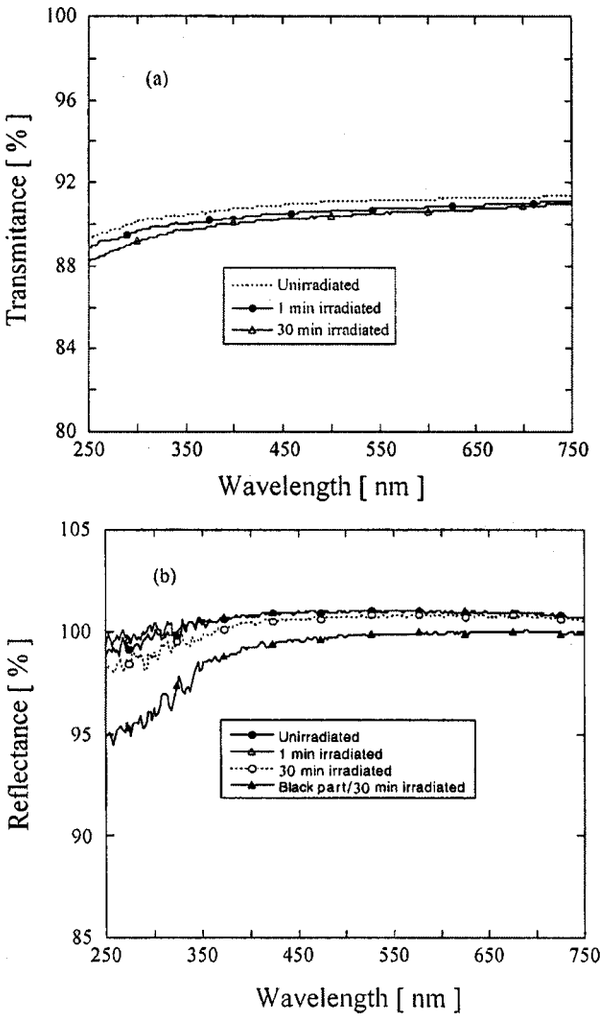

Figure 5. Transmission and reflection spectra for quartz wafers before and after sputtering with an Ar-low energy ion source for 1 and 30 min. Reflection spectra also include the data for the black area of 30 min irradiated sample.

bonding. In order to evaluate whether the surfaces are UV transparent after deposition of a few nanometers of Fe, we have examined the deposited surfaces using an ellipsometer (J. A. Woollam Co., Inc., HS-190). Three quartz samples of 20×20 mm^2 were used to investigate the transmittance and reflectance behavior before and after irradiation.

Samples were sputtered using the modified hollow cathode low energy ion source, which was capable of depositing ultrathin Fe layers during sputter cleaning on the surfaces. Only two samples were irradiated for 1 and 30 min. As a result of measurement on each sample, there was no characteristic absorption seen either in the transmittance spectrum of each sample or in the reflection spectrum over the ranges from UV to near infrared regions (250-2000 nm) (Fig. 5). The transmittance rate declined over the ranges from infrared to UV regions, which was more significant in the 30 min sputtered sample than that of 1 min irradiation. There was no significant difference recognized among various samples for the near infrared region. As for the reflection spectrum, there was almost no difference between the unirradiated and 1 min irradiated surfaces, although we saw a slight reduction in the reflection rate in the UV region with the 30 min irradiated sample. The edge area of the 30 min irradiated sample was found to be black, possibly due to excess Fe, and a reduction of reflection rate over the ranges from near the infrared region to the visible region. In particular, a reduction of the reflection rate in the UV region was significant.

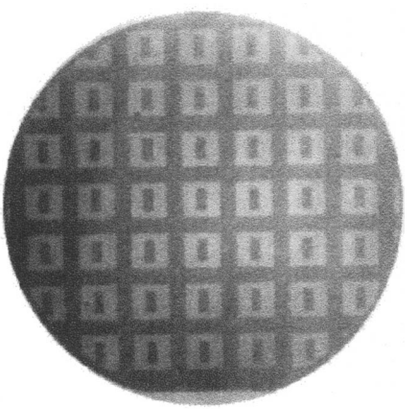

Figure 6. IR image of 200 mm bare Si bonded with 100 mm patterned Si at room temperature. The samples were sputtered for 300 s with a low energy hollow cathode Ar ion source of 80 eV and 3 A. Bonded samples were cold-rolled under a load of 400 MPa.

Infrared (IR) transmission image.—The IR transmission image of a 200 mm bare Si/100 mm patterned Si interface bonded at room temperature is shown in Fig. 6. The figure shows the interface image only for 100 mm diam area. The white area shows the bonding region, whereas the rest of the area is the unbonded area. The cavities of sizes $5.6 \times 2.6 \times 0.02$ mm^3 were surrounded by the bonded area of 9×9 mm^2 (which includes the cavity area). A void-free interface is evident throughout the whole contact area. Recently, fabrication of Si multistacked microengines and microdevices[10] has been reported by wafer level fusion bonding at high temperature. However, the yield in the reported work could be low due to process complexity at high temperature. From that perspective, a process engineer can achieve high yield for the fabrication of such complicated multilayered Si devices using this room temperature integration process.

Bonding strength and mechanism.—For tensile pulling tests, bonded wafers were cut into 10×10 mm^2 sizes to measure the interface strength. Chip size samples were randomly picked up for the test. The tensile pulling test results for Si/Si, Si/Al silicate glass, Si/quartz, and quartz/quartz wafers with transparent Fe layers including bonding and annealing conditions are shown in Table I. The sputter cleaning time for Si/Si, Si/Al silicate glass, Si/quartz, and quartz/quartz were 30/30, 600/1800, 600/1800, and 1800/1800 s, respectively. As stated previously, the Ar-ion source is capable of sputter cleaning with simultaneous Fe deposition. The irradiation time for Si/Si was very short, because there is no concern of adhesion between Si/Si. Si/Si wafers were not annealed due to spontaneous covalent bonding. On the other hand, surface adhesion layers were

Table I. Tensile results of various combinations of Si, Al silicates glass, and quartz wafers bonded with transparent Fe layers at room temperature. A few pairs were annealed in air at temperature ranges up to 723 K.

Mating pair	Irradiation time (s)	Annealing condition (K)	Interface strength (MPa)	Remarks
Si/Si	30:30	No annealing	10-20	Bulk fracture
Si/Al silicate glass	600:1800	573/8 h	15.8-45.2	Bulk fracture
		673/8 h	11.2-31.4	
Si/quartz	600:1800	573/8 h	6-14.4	Interface fracture
Quartz/quartz	1800:1800	723/1 h	8-15	Bulk fracture

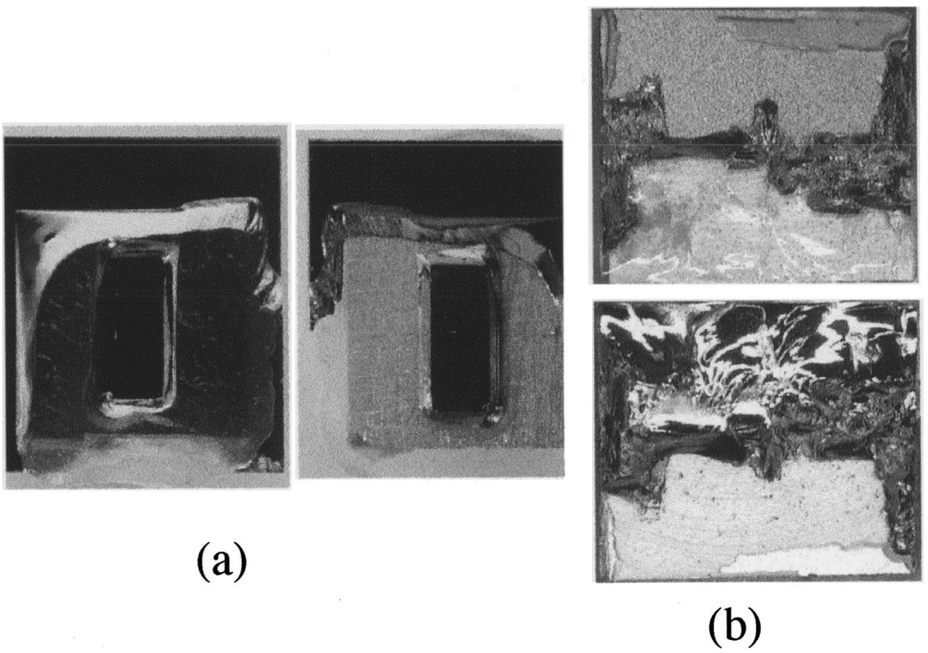

Figure 7. Fracture images of (a) bare Si/patterned Si and (b) bare Si/bare Al silicate glass wafers bonded at room temperature. Si/Al silicate glass wafers were annealed in the atmospheric pressure of air at 573 K.

needed to produce adhesion between Si/Al silicate glass, and quartz/quartz wafers. In addition, these bonded wafers were annealed at atmospheric pressure in air at the specified temperatures (Table I) because of low interface strength at room temperature. In fact, Si/Al silicate glass and Si/quartz, quartz/quartz wafers annealed at temperatures below 470 K were debonded across the interface at the time of dicing. The interface strengths of Si/Si, Si/Al silicate glass, and quartz/quartz wafers are found to be comparable to that of bulk materials. Figure 7 shows the optical images for bulk fractured Si/Si and Si/Al silicate glass. The three-dimensional fracture of the bonded materials is evident, indicating strong interface strength, which may be sufficient to withstand the back thinning processes of device fabrication. Si/quartz wafers were debonded across the interface even though the tensile strength was varied from 8-15 MPa, suggesting a requirement of higher temperature annealing. The strong adhesion of Si/Si bonded by the SAB process at room temperature is due to the covalent nature of surface atoms of bonding mates. The atomic forces are thought to be responsible for bonding if both the sputter cleaning and bonding are done in an UHV pressure. However, long exposure (up to 26 h) to sputter-cleaned Si surfaces in an UHV pressure caused the increase of the electrical resistance of the Si/Si bonded interface because of the deposition of residual gas atoms on the surfaces.[11] In addition, the sputtering induced amorphous layer did not appear to have an effect on bonding strength, but it extended bonding flexibility in diverse crystallographic-oriented wafers. The fact indicates that the sputter-cleaned surfaces remain activated despite the existence of defects and absorption. On the other hand, the question is raised as to why the SAB technique was not successful in the case of ionic crystal integration without an intermediate adhesion layer. Generally positive and negative ions are positioned side by side in the ionic crystal. Under irradiation effect, cations and anions in ionic crystals like SiO_2 could form Frenkel pairs that results in discontinuous polarized surfaces. Arguably, inhomogeneous charging states[12] might be generated even on identical surfaces that may have a larger repulsive force than an attraction force. Therefore, the polarization characteristics are believed to control the adhesion of Si/glass and glass/glass wafers. Deposition of very thin Fe layers could result in charge transfer between Si and Fe, and Fe and glass wafers. Subsequent bonding and annealing could induce adhesion by the cross-linking of Fe on mating surfaces.

Sealing tests.—The bonded wafers with cavities, as shown in Fig. 8, were cut into chip size samples for the radioisotope fine leak test. Sealed cavities were exposed to a mixture of Kripton-85 gas of specific radioactivity of 1.6×10^{12} Bq/m^3 in a background high pressure of 5×10^5 Pa in order to measure the leak rate of the cavities. The background dose was 90-116 cpm. The leak rate of exposed cavities was measured outside the chamber using a scintillation counter (by measuring radiation counts). The estimated leak rate was 1.0×10^{-12} Pa m^3/s, which satisfies the requirements of 1×10^{-9} Pa m^3/s for MIL-STD-883E[13] encapsulation standard in the hazard environments. In addition, vacuum seal behavior was examined by the measurements of quality factor *vs.* chamber pressure. The quality factor (vibration characteristics) of a damped system can be defined by $Q = 2\pi U_i / U_d$, where U_i is the stored vibration energy and U_d the dissipated energy per period.[14] For the fabrication of vacuum seal cavity, first a Pyrex glass wafer was bonded to the back side of oxidized/patterned Si wafers by anodic bonding followed by anisotropic tetramethylammonium hydroxide (TMAH) etching on Si to fabricate cavities.[15] The wafer was cut into chip-sized samples and the size of the cavities was $5.6 \times 2.4 \times 5$ mm^3. Then a $300 \times 35 \times 2$ μm^3 sized microcantilever of 33 kHz resonant frequency was placed in the cavity structure and fixed with indium paste in order to measure Q values of the cavities. Finally the cavities with the cantilever fabricated on Si on anodic-bonded Pyrex glass and Si wafer were simultaneously sputter cleaned by using two Ar-FAB sources with 45° incident angles in an UHV single-chamber SAB tool and bonded. The energy and current of the Ar-FAB sources used for sputter cleaning were 1.5 keV and 15 mA, respectively. Then the time-dependent Q values of the sealed cavities were measured by using an atomic force microscope (AFM, Seiko Instruments, Inc., SPI3800N). On the other hand, the Q dependent chamber pressure was measured using a similar cantilever in the AFM chamber (Fig. 8a) and the reference Q value was identified at the vacuum pressure at the time of sputter cleaning from the Q-dependent chamber pressure. Identical Q values at the reference vacuum level at the time of sputter cleaning and of cavities are indicative of airtight cavities. However, the leak rate (quantity of air in cubic meters flowing through a leak per second)[13] of the vacuum-sealed cavities estimated from the difference between the maximum and minimum Q values and the cavity volume (cantilever

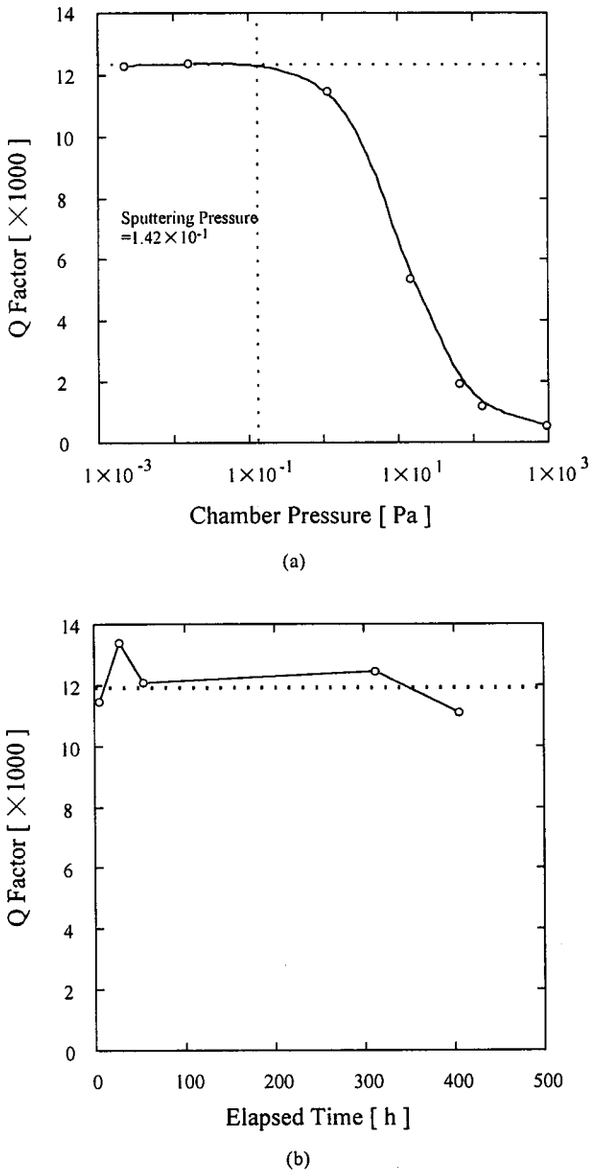

Figure 8. (a) Pressure and (b) time dependence on the *Q* factor measured in an atomic force microscope. The *Q* value is about 1.2×10^4 at a reference chamber pressure of 1.42×10^{-1} Pa m^3/s, which is almost constant over 400 h. The estimated leakage rate was 2.6×10^{-16} Pa m^3 s after 400 h.

volume was deducted) is found to be 2.6×10^{-16} Pa m^3/s after 400 h, which is better than that of the radioisotope fine leak test.

Microstructural observation.—Figure 9 shows the high-resolution transmission electron microscope (HRTEM) images for Si/Si and quartz/quartz wafers bonded by the SAB process. An amorphous layer of about 5 nm thick is detected across the interface of Si/Si bonded at room temperature (Fig. 9a). Perhaps the amorphous layer is generated due to irradiation damage of the ion beam used for removing surface oxides and contaminants. Similar interfacial behavior with an amorphous layer of 100 nm is also observed in quartz/quartz samples, which were annealed at 723 K for 1 h (Fig. 9b). In both cases, due to the amorphous layer, no distinct Fe layer was evident, and Fe was below the detection level of EDS measurements. However, the amorphous interfacial layer was found to have full strength material at both room temperature and high temperature, as shown in tensile results.

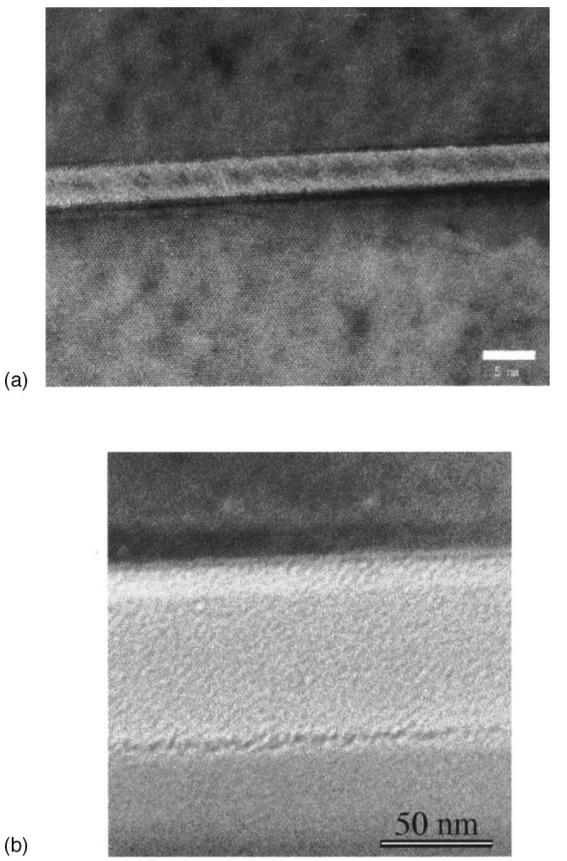

Figure 9. HRTEM image of (a, top) Si/Si and (b, bottom) quartz/quartz interfaces. Si/Si wafers were not annealed, whereas quartz/quartz wafers were annealed at 723 K for 1 h.

Non-UV transparent layers.— Surface analysis.—In the case of non-UV transparent intermediate layers, an Al silicate glass wafer was coated with Au/Ti layers. Since the SAB process deals with the atomic level interaction of mating surfaces, surface smoothness must be very high (rms value: subnanometer to nanometer) to get an intimate contact between the paired surface atoms. To activate surfaces is an important criterion for adhesion, which was performed by etching with a low energy Ar ion beam. Therefore, surface roughness of sputtered Au/Ti film on glass should be observed. Figure 10

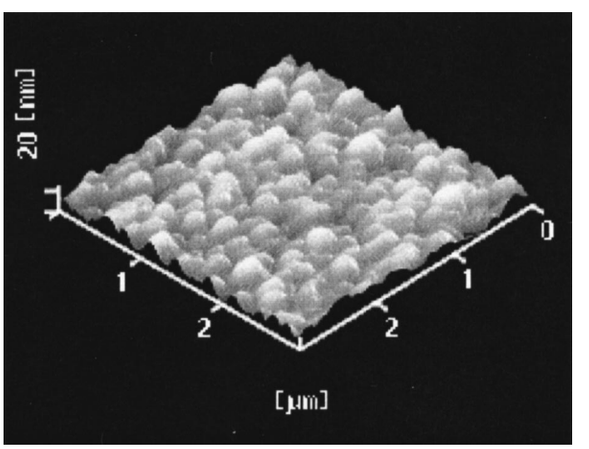

Figure 10. AFM image of the Au/Ti/glass surface before sputter cleaning.

Table II. Tensile result of Si and Al silicates glass wafers bonded with nontransparent Au/Ti layers on glass wafers at room temperature. Bonded samples were annealed in air at 573 K for 8 h.

Mating pair	Irradiation time (s)	Annealing condition (K)	Interface strength (MPa)	Remarks
Si/Au/Ti/Al silicate glass	300:300	573/8 h	10-23	Fracture across Ti and glass wafer

shows the atomic force microscope (AFM) image of the Au/Ti sputtering surface on a Si wafer, before irradiation. The scanning area was 3×3 μm^2. As expected, the average, peak to valley, and rms values of the surface roughness before irradiation were 3.4, 30.8, and 4.3 nm. Deformation under bonding load may lower the surface roughness of Au. No significant change in the surface roughness was found after 300 s sputtering with the ion source (not shown).

Bonding strength.—Tensile pulling tests of Si/Au/Ti/Al silicate glass wafers showed that the fractures mainly took place across the interface of Ti/SiO_2, but not from the bonding interface of Si/Au. The wafers were annealed in atmospheric pressure of air at 573 K for 8 h. The estimated interface strength was varied from 10 to 23 MPa (Table II). The cause of interface strength variation may be associated with the inhomogeneous oxidation growth of vacuum-deposited Ti due to oxygen transport from glass.[16] Since TiO_2 is brittle in nature, debonding was taking place across the newly formed weak interface of TiO_2/SiO_2. However, inhomogeneous growth of oxidation of Ti can be controlled by the insertion of Si between Ti and Al silicate glass.

Conclusions

This paper demonstrates the development and application of an ultrahigh vacuum (UHV) wafer level surface activated bonding (SAB) tool. The tool enables parallelism between 8 in. wafers with high accuracy alignment and bonding. Silicon wafers of 8 in. diam have been successfully bonded with 3-5 in. Si, Al silicate glass, and quartz by the SAB process at temperature ranges from room temperature to 723 K with and without UV transparent Fe adhesive layers. No substantial influence of Fe thin layers on the transmission and reflection behavior of quartz is found. The infrared transmission image indicates void-free interfaces. The fine leak test of sealed silicon cavities shows a leak rate of 1.0×10^{-9} Pa/m^3 s, which is lower than the American military standard encapsulation requirements for MEMS devices in harsh environments. A superior leak rate of 2.6×10^{-16} Pa/m^3 s is measured after incorporation of a cantilever in the cavity prior to bonding in vacuum. An average bonding strength higher than 10 MPa is achieved with bulk fractures in Si/Si, Si/glass, and quartz/quartz wafers. In Si/Au/Ti/Al silicate glass samples, fracture takes place across the Ti and glass interface, but not in the Si/Au interface. Inhomogeneous oxidation of Ti may attribute to the variable bonding strength of the Ti/glass interface. HRTEM observation on Si/Si and quartz/quartz interfaces reveals amorphous layers of about 5 and 100 nm thick, respectively. Based on the performance of the SAB tool with bonding results, it can be concluded that the developed SAB tool has potential application for microelectronics and MEMS device packaging.

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