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Nanobonding for Multi-Junction Solar Cells at Room Temperature

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Direct nanobonding of *p*-Si/*n*-GaAs wafers based on surface activation that uses an Argon (Ar)-fast atom beam at room temperature has been investigated. The bonding strength of the interface was 14.4 MPa at room temperature, and remained nearly constant after annealing up to 600 °C. An amorphous layer with a thickness of 11.5 nm was found across the interface without annealing. After annealing, the electrical current-voltage (*I-V*) characteristics were improved and the amorphous layer was diminished across the interface. The thermal stability of the interfacial properties of Si/GaAs indicates its potential use on the fabrication of multi-junction solar cells with Si substrate to lower the cost while improving the solar cells' efficiency. The thickness dependence of *p*-Si/*n*-Si interfacial *I-V* characteristics using COMSOL simulation indicates the decrease of breakdown voltage and current with the increase of the junction thickness.

Introduction

Renewable energy sources such as solar, wind and hydropower are ecologically friendly. These sources will eventually replace the conventional sources such as fossil fuel energy to meet the energy requirements of the future and to avoid emission of green house gases, which lead to global warming. As a potential substitute of conventional energy, recently photovoltaic solar cells have drawn lots of attention. They were incorporated in windows, roofs and outside walls of new houses and buildings at the construction stage [1]. Among various types of solar cells being studied, semiconductor multi-junction solar cells are gaining special interest. They are known for their high efficiency, which is achieved by dividing the absorption of light spectrum power to different subcells [2]. Multiple semiconductors provide the selectivity for different photon wavelengths. Currently, the highest efficiency reported for a triple junction solar cell system is 41.6%±2.5 (from Boeing Spectrolab) [3]. In order to fabricate this solar cell, the optimum bandgaps for the highest efficiency were compromised to minimize the lattice mismatch between the epitaxial layers.

Multi-junction solar cells can be fabricated using the direct wafer bonding technique reported here without compromising the bandgaps. Direct wafer bonding describes the adhesion phenomenon between mirror polished, flat, and clean wafers with diverse crystal structures through the Van der Waals forces when brought into contact at room temperature. These forces result in strong bonding between the wafers [4]. As previously mentioned, the direct wafer bonding addresses the lattice mismatch issue in the integration of different materials. Therefore, it is very important for the fabrication of solar cells with optimized bandgaps. While a four-junction solar cell structure [GaInP/GaAs/InGaAsP/InGaAs] has been proposed, the epitaxially grown GaInP/GaAs junction on Ge layer bonded with oxidized Si substrate and the epitaxially grown InGaAsP/InGaAs junction on InP layer bonded with oxidized Si substrate have also been investigated [5-7]. In specific, the influence of the bonded interfaces on the performance of the two separate subcells of the proposed four junction solar cell system has been characterized. For bonding, the wafers were treated by wet chemical cleaning to remove organic and particulate contaminations followed by surface activation using atmospheric pressure plasma and bonded at 150 °C or higher. For layer exfoliation, InP and

Ge wafers were implanted respectively using He^+ and H^+ ions with energy between 115 and 180 keV to a dose of at least 1.0×10^{17} cm^{-2}. In both cases, the open circuit voltages and overall performances were slightly degraded compared with those of the solar cells with original bulk substrates (InP and Ge), probably due to the introduced SiO_2 layer at the bonding interfaces [7].

To address the influence of the thermally oxidized layer at the interface, an improved direct bonding technology, known as nanobonding based on surface activation [8], has been proposed to fabricate multi-junction solar cells. The nanobonding offers atomic scale bonding at lateral dimensions in ultra-high vacuum (UHV) or in air at room temperature [8]. Compared with other existing direct bonding technologies, such as thermal compression bonding [9], fusion bonding [10], plasma bonding [11] and adhesive bonding [12], nanobonding technologies offer significant advantages. These advantages include high bonding strength, submicrometer alignment accuracy, optical transparency and high conductivity at the bonding interface without the requirement of chemical treatment before the bonding process. In addition, the bonding process does not require high external pressure or high temperature [8]. The high bonding strength offers the wafers higher tolerance of handling during the solar cell manufacture such as grinding and polishing. The sub-micrometer alignment accuracy enables a good performance of the solar cells after integration with other microelectronic systems. Optical transparency decreases the light reflection at the bonding interface, allowing more photons to travel down to the bottom subcells and enhances their performances [8]. With the high conductivity, the ohmic loss at the interface is reduced and the current flow is enhanced. Therefore, these properties can be very beneficial in fabricating multi-junction photovoltaic solar cells.

For mass production such as in household use, the fabrication cost of highly efficient semiconductor multi-junction solar cells is not affordable [1]. One way to reduce the cost is to use cheaper material, such as Si for the substrate. Si wafers are cheaper than most III-V wafers such as gallium arsenide (GaAs). Although Si handling substrate doesn't contribute to the solar energy conversion, it plays an important role in determining the solar cell performance. Since the photon generated current flows through the substrate before being collected by the back contact (cathode), the characteristics of the interface (i.e. thickness, resistance) between the Si substrate and the solar cell directly affect the overall energy conversion efficiency. From the practical and fabrication perspective of solar cells [13, 14], the influence of heating and the thickness of junction materials on the performance of the solar cells is of great importance. Moreover, Si substrates can also provide integration of solar cells with other microelectronic systems. Si is the most widely used semiconductor material in electronic industry. Therefore, multi-junction solar cells with Si substrate are very promising both in terms of the cost and compatibility.

This article reports the nanobonding of Si/GaAs in ultra-high vacuum at room temperature. The bonded interface has been investigated at different temperatures ranging from room temperature up to 600 °C to observe the thermal influence on the solar cell performance. These observations are critical because during the fabrication of solar cell electrodes, high temperature (800 °C) is often required to perform the electrode metal deposition. The current-voltage characteristics of the bonded interface as a function of junction thickness have been compared with the results from COMSOL multi-physics simulator.

Experimental

Commercially available one side mirror polished 2 inch *n*-Si (100) and *p*-GaAs (100) were used for the bonding experiments. The resistivity of *n*-Si and *p*-GaAs was 1-20 Ω-cm and > 0.001 Ω-cm, respectively. The wafer thickness of Si and GaAs was 275 ± 25 μm and 350 ± 25 μm, respectively.

The Si and GaAs specimens were bonded by surface activation based nanobonding technology in UHV using a nanobonding and interconnection system (NBIS), as shown in Fig.1 [15]. The NBIS consists of a load-lock chamber and a bonding chamber. The bonding chamber has two argon fast atom beam (Ar-FAB) sources and a bonding head. The vacuum pressure of the bonding chamber was 1.9×10^{-7} Pa before bonding, and the specimens were activated using a 1.5 keV Ar-FAB with a current of 48 mA in the bonding chamber at a background pressure of 5.6×10^{-2} Pa for

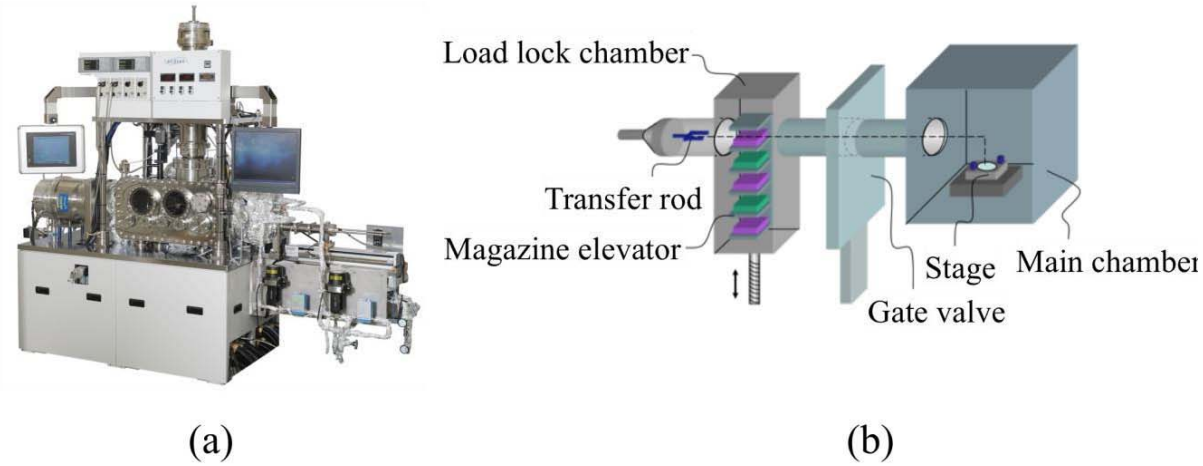

Figure 1. (a) Optical image and (b) schematic diagram of an automatic controlled surface activation based nanobonding and interconnect system (NBIS).

300 s. The activation sources were placed at 45° with respect to the center of the specimens. The beam activated the surfaces homogeneously throughout the 2 inch diameter wafers. Finally, the specimens were contacted under the bonding head in UHV at room temperature. After bonding, the bonded interface was investigated by infrared (IR) camera. The bonded specimen was then cut into 10 mm×10 mm chips and annealed at 200, 400, and 600 °C, respectively for 1 h in air. After being cooled down to room temperature, the interfaces of annealed chips were characterized through current–voltage (*I–V*) measurements, tensile pulling and high resolution transmission microscopy (HRTEM) techniques. For *I–V* measurements, conductive silver electrodes of 2 mm diameter were made and pasted at the center on the top and bottom surfaces of the bonded specimen before and after annealing. A semiconductor parameter analyzer (model #HP-4145B) was used for measuring the *I-V* characteristics of *p*-Si/*n*-GaAs bonded specimens at different annealing temperatures.

Results and Discussion

Fig. 2 shows the IR image of a 2 inch Si/GaAs wafer bonded at room temperature using nanobonding technology. The damage near the edge was due to the blade test. The bright areas were the bonded areas. Some voids were presented across the interface due to the presence of particles on the activated surfaces and air trapping at the interfaces during the bonding process.

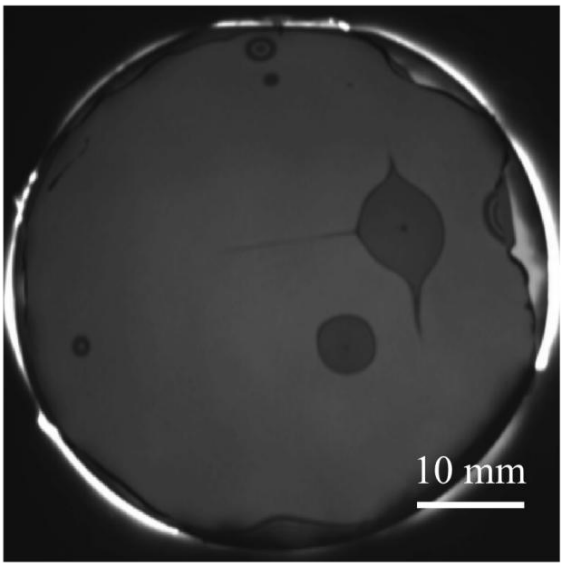

Figure 2. Infrared transmission image of bonded Si/GaAs wafers at room temperature.

For practical application, a high bonding strength is required for layer transfer process [16]. The bonding strength of Si/GaAs specimens without annealing and with annealing at 200, 400 and 600 °C was measured by a tensile pulling tester. The bonding strength was 14.4, 10.7, 9.9 and 11.9 MPa for samples at room temperature, 200, 400 and 600 °C, respectivly. No significant influence of annealing temperatures on the bonding strength was observed. However, bulk fractures were observed after tensile pulling test (Fig. 3) across the bonded interface which is an indication of

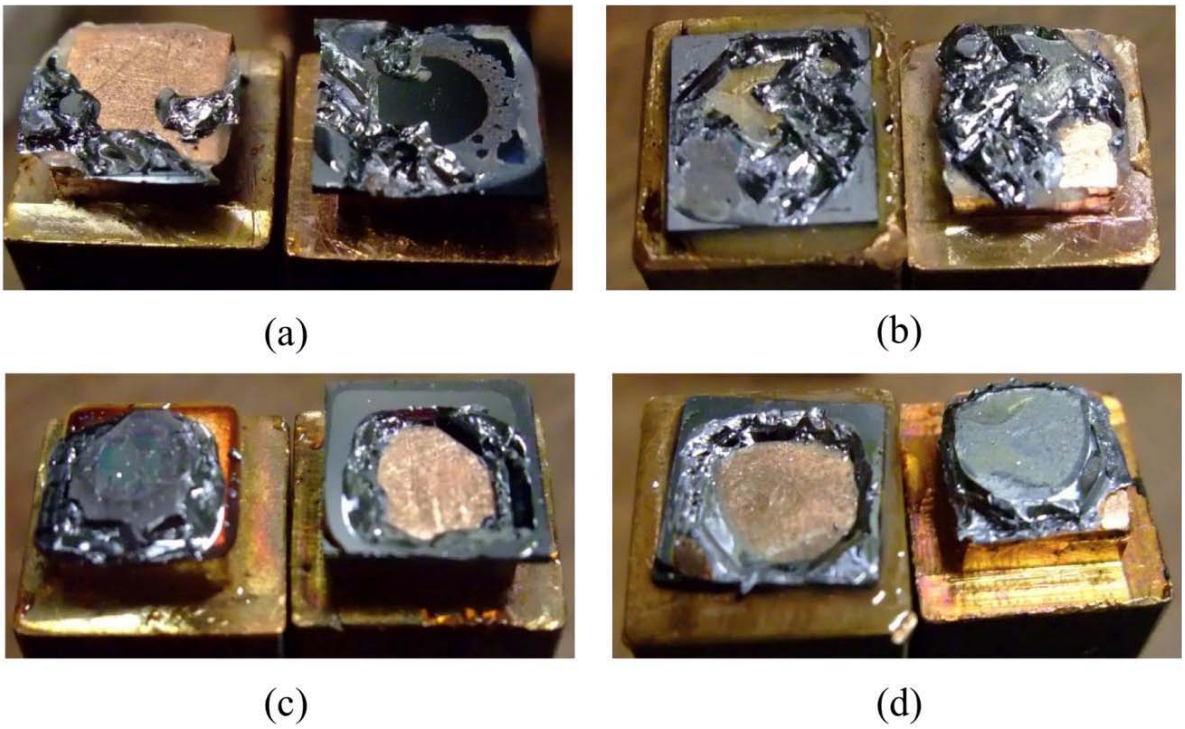

Figure 3. Fracture images of bonded Si/GaAs wafers after tensile pulling test at (a) room temperature, (b) 200, (c) 400, and (d) 600°C.

strong bonding strength at different temperatures. On the other hand, the bonding strength in the sequentially plasma activtion bonding decreased after annealing temperature above 300 °C due to the thermal induced voids existing at the bonded interface. The high bonding strength was attributed to the spontaneous adhesion through intimate contact between the clean and smooth surfaces [8] after activation in UHV. Therefore, the bonded Si/GaAs with high bonding strength with thermal tolerance up to 600 °C has demonstrated that it can be utilized in the layer transfer both for low temperature and high temperature applications.

The *I-V* characteristics of the bonded *n*-Si/ *p*-GaAs at different annealing temperatures are shown in Fig. 4. The *I-V* characteristics show that the forward current density reduced after annealing at 200°C. The subsequent annealing steps at 400 and 600 °C increased the forward current density. This behavior is different from that of the hydrophilic direct bonding of *p*-Si/*n*-GaAs, where the forward current increased with increasing thermal annealing temperature [17]. The reverse leakage current density decreased as the annealing temperature increased. An ideal *p*-*n* diode behavior was observed at the annealing

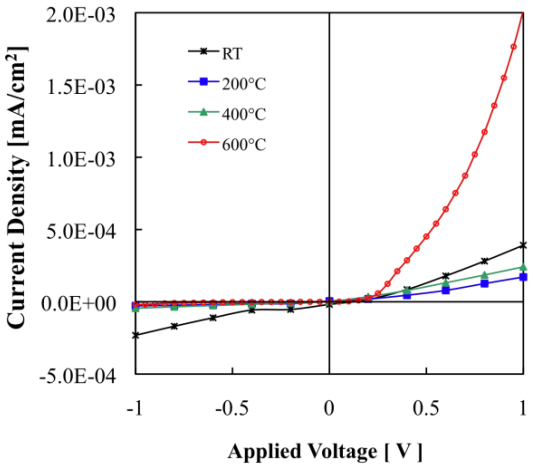

Figure 4. Interfacial current density of *p*-Si/*n*-GaAs as a function of applied voltage.

temperature of 600 °C. This high temprature tolarence is very useful during the fabrication of solar cells since the deposition of electrodes onto the solar cells normally requires a temperature around 800 °C, therefore it is critical for the interface to maintain the electrical properties under high temperature [14]. In this study, the improved *I-V* characteristic behavior was caused by the annealing induced change of defects and doping profiles at the bonded interface and thermal oxide of the Si surfaces during annealing [18, 19]. The temperature dependent *I-V* characteristics can further be explained by the nanostructure of the bonded interface, as discussed below.

Fig. 5 shows the nanostructure of the bonded Si/GaAs interfaces at different temperatures. The bonded interfaces had no interfacial voids or fractures at the nanometer scale in these images. Without annealing (at room temperature), an amorphous layer with a thickness of 11.5 nm was observed at the interface. It has been reported that the Ar atom implantation generates surface damage during the activation, resulting in an amorphous layer at the interface [20]. The existence of amorphous layer across the bonded interface prohibits fracturing caused by the large difference of thermal expansion coefficients between Si and GaAs (Si: 2.6×10^{-6} K^{-1}, GaAs: 6.8×10^{-6} K^{-1} at 25 °C) during annealing. The thickness of the amorphous layer was reduced from 11.5 nm to 3.0 nm upon annealing at 200 °C. When the annealing temperature increased to 400 °C, the amorphous layer was

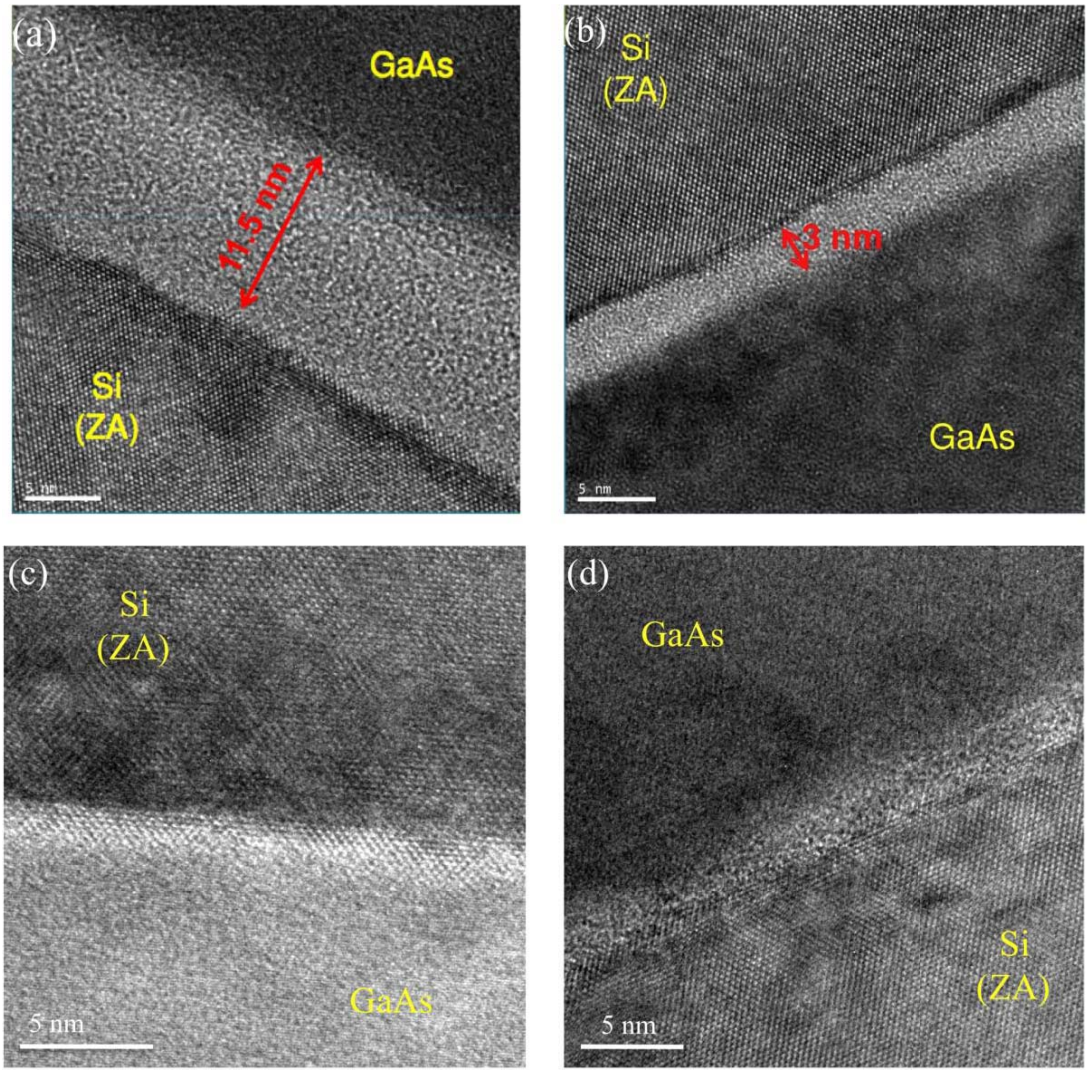

Figure 5. HRTEM images of bonded interface between Si and GaAs (a) before annealing, and after annealing at (b) 200, (c) 400, and (d) 600°C.

changed to crystalline layer with a thickness of about 2 nm. Finally, at 600 °C, the amorphous layer diminished. Diffusion of Ga and As into Si has been hypothetically discussed through measuring the interfacial resistance of Si and GaAs bonded using the hydrophilic technique [17]. The diffusion increases with the increase of annealing temperature and time. In this study, while crystallinity at the bonded interface started at 400 °C and the amorphous layers vanished at 600 °C, no perfect crystalline structure was obtained at 600 °C. This can be explained by the diffusion mechanism stated in [17], but it requires further investigation to clarify the fact. Therefore, the reduced amorphous layer thickness upon annealing is responsible for the observed improvement of *I-V* characteristics from 200 °C to 600 °C. This interfacial behavior is consistent with those of GaP/GaAs and Si/Si bonded interfaces [18, 19].

Since multi-physics are involved in the carrier transportations at heterojunction interface, it is easy to study first the homogeneous junction to build a solid understanding in the heterojunction carrier transportation mechanisms. Therefore, the *p-n* junction fabricated by Si-bonded wafers has been simulated in order to understand the influence of thickness of the bonded wafers on the interfacial *I-V* behavior. In the COMSOL simulation [21], we modified the existing semiconductor model into different dimensions, mainly to observe the thickness dependence of *I-V* characteristic of the junction interface. The doping concentration is assumed to be a Gaussian distribution within the junction, with maximum donor and acceptor concentrations of 1.0×10^{17} cm^{-3}. The cross sectional junction dimensions simulated were 7×5, 35×20, 140×100 and 280×200 μm, respectively.

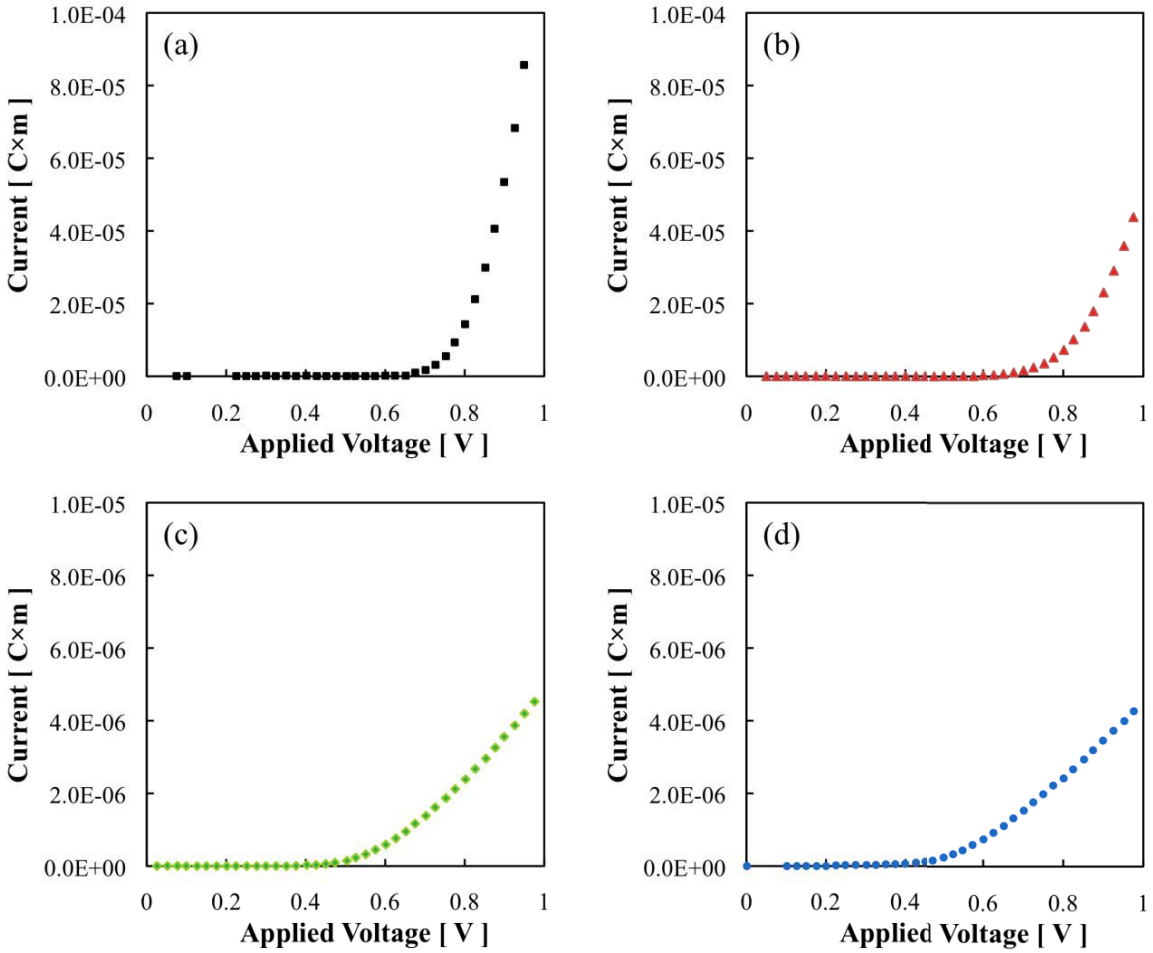

Figure 6. Simulated *I-V* curve of *p*-Si/*n*-Si junction with cross sectional dimensions of (a) 7×5, (b) 35×20, (c) 140×100, (d) 280×200 μm showing the thickness dependence of junction materials. The sequence of the dimension is the thickness and length. The unit of current is coulomb meter.

In the simulation, a single electrostatic node was used to calculate the potential distribution within the *p*-*n* junction under zero bias and forward bias from 0 to 1 V. Two transports of diluted species nodes were used to model the carrier (electrons and holes) distribution and motion within the junction under bias.

Fig. 6 shows the simulated results of the *p*-Si/*n*-Si junction. The comparison among (a)-(d) shows that both the breakdown voltage and current decrease with the increase of the material thickness. The breakdown voltage decreased slightly from around 0.7 V in Fig 6(a) to 0.5 V in 6(d), and the current under forward bias of 1 V decreased by orders of 2, 18 and 20 in 6(b), 6(c) and 6(d), respectively. The decrease of both the breakdown voltage and current may be due to the carrier recombination mechanism, which is dominant in bulk materials [13]. As a result in the Fig 6(c) and 6(d), the current decreased significantly compared with that in Fig 6(a) and 6(b). From the practical perspective (such as solar cells embedded on the roof of a house), the thickness issue is very important and needed to be carefully considered in multi-junction solar cell fabrication. This is because the solar cell efficiency can benefit from a thicker layer that can absorb more photons with longer wavelength [13]. However, larger thickness can compromise the current flow and open circuit voltage of the *p*-*n* junction and lower the overall solar cell performance. Therefore, an optimized design of layer thickness that can balance the photon absorption and carrier recombination should be available by simulation.

Conclusions

The feasibility of direct wafer bonding technology for the application in photovoltaic solar cells for mass production at low cost has been investigated. In this study, *p*-Si and *n*-GaAs wafers were bonded at room temperature by surface activation based nanobonding technology. The influence of thermal annealing on the characteristic behavior of the bonded interface was demonstrated. The tensile pulling test showed that the bonding strength was 14.4 MPa at room temperature and changed to 10.7, 9.9 and 11.9 MPa after annealing at 200, 400 and 600 °C respectively. One amorphous layer with thickness of 11.3 nm was found across the interface without annealing. It was found that annealing improved the electrical *I*-*V* characteristics and reduced the amorphous layer thickness across the interface. This nanobonding technology at room temperature is suitable for the fabrication of multi-junction solar cells. The high bonding strength of the interface provides greater feasibility in the solar cell manufacture, installation and maintenance, and the electrical properties of the Si/GaAs interface offer the possibility of high efficient multi-junction solar cells being embedded on cheaper and more compatible Si substrate. These conditions are critical to the realization of solar energy usage both in terms of low cost and wide range of applications. The simulated results of Si wafer thickness dependence of the *I*-*V* characteristics may provide insights into the use of Si as a rigid and stable substrate for photovoltaic solar cell applications. In future work, nanobonding between other materials suitable for solar cell fabrications can be studied to design low cost and high efficiency multi-junction solar cells that can be put into mass production.

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