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Surface activation-based nanobonding and interconnection at room temperature

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Abstract

Flip chip nanobonding and interconnect system (NBIS) equipment with high precision alignment has been developed based on the surface activated bonding method for high-density interconnection and MEMS packaging. The 3σ alignment accuracy in the IR transmission system was approximately ± 0.2 μm. The performance of the NBIS has been preliminarily investigated through bonding between relatively rough surfaces of copper through silicon vias (Cu-TSVs) and gold-stud bumps (Au-SBs), and smooth surfaces of silicon wafers. The Cu-TSVs of 55 μm diameter and the Au-SBs of 35 μm diameter with ~6–10 nm surface roughness (RMS) were bonded at room temperature after surface activation using an argon fast atom beam (Ar-FAB) under 0.16 N per bump. Silicon wafers of 50 mm diameter with ~0.2 nm RMS surface roughness were bonded without heating after surface activation. Void-free interfaces both in Cu-TSV/Au-SB and silicon/silicon with bonding strength equivalent to bulk fracture of Au and silicon, respectively, were achieved. A few nm thick amorphous layers were observed across the silicon/silicon interface that was fabricated by the Ar-FAB. This study in the interconnection and bonding facilitates the required three-dimensional integration on the same surface for high-density electronic and biomedical systems.

(Some figures in this article are in colour only in the electronic version)

Introduction

According to the International Technology Roadmap for Semiconductors (ITRS) [1], the packaging of new micro-electro-mechanical systems (MEMS), nanostructures, and emerging device technologies is a critical research area of electronic and biomedical systems. It further states that electrical and optical interface integration in system packaging is a key challenge to be solved. An example of the emerging systems is the noninvasive wireless imaging capsule for the early detection of defective cells in human organs, such as the gastrointestinal (GI) tract [2]. In order to package such systems, devices with high-density inputs/outputs are indispensable to be bonded on the package substrate. Currently the size of chip wiring such as global and intermediate layers (~sub-μm) in CMOS technology is much lower than that of the adhesive and solder bumps (~20 μm) in flip-chip packaging technology. This technological gap in the scaling pushes the bonding and packaging technology to a level as close as possible to the chip wiring. In fact, current integration and packaging technologies, such as thermocompression bonding [3], fusion bonding [4] and adhesive bonding [5], are incompatible with the scale and type of the materials in the bonding for the systems. This is because of the need for high pressure [6], elevated temperatures (~1000 °C) [4], chemical solvents [5, 7] and other processing conditions. Therefore, the challenges of the current bonding techniques for system integration are (1) the difficulty of integrating dissimilar materials across multiple dimensions [8], (2) the inaccuracies in optical alignment and deformation of optical components such as polymer lenses [9] and delicate MEMS devices [10] caused

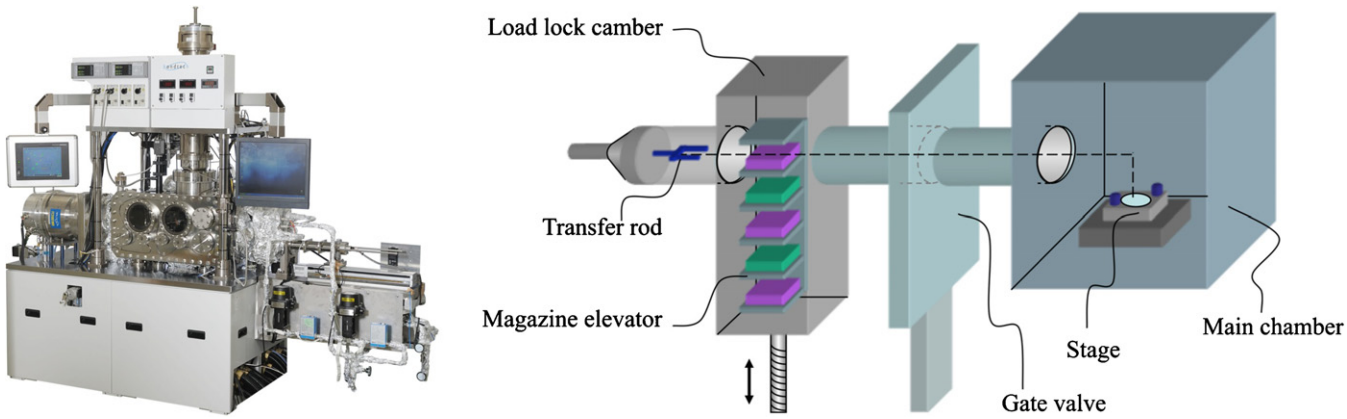


Figure 1. (*a*) Optical image and (*b*) schematic diagram of an automatic controlled surface activation-based NBIS. The NBIS accommodates specimens with sizes from a few mm to 50 mm.

by existing heat- [4, 7] and pressure-based bonding techniques [6], and (3) the need to integrate temperature sensitive MEMS devices [11].

To alleviate the bonding and packaging issues for the integration of the miniaturized systems, a custom designed nanobonding and interconnect system (NBIS) based on the surface activated bonding (SAB) method has been developed. The NBIS allows chip-size and wafer-level high-density interconnection, and bonding of materials, devices and components from dissimilar technologies on a single substrate. Surface activation refers to removing native oxides, carbon contaminants and particles from the surface. When the surfaces are properly prepared (roughness <1 nm and activated), placing the surfaces in direct contact using the flip-chip technique causes the surface atoms to attract each other and the atomic forces 'zip' the surfaces to a solid interface at room temperature [12–14]. Therefore, the inherent advantages of the nanobonding over other bonding methods are (1) spontaneous adhesion between two materials without precursor (such as hydrogen bonds in hydrophilic and hydrophobic methods), (2) bonding dissimilar materials with high bond strength without heating, which extends the range irrespective of thermal expansion mismatch, (3) no requirement of high external pressure, adhesive, or chemicals, (4) sub-micrometer alignment accuracy, (5) biologically compatible (i.e. non-toxic) interface, (6) preserves delicate components and biological specimens, (7) applicability to the bonding of nanostructures (i.e. nanowires), and (8) mechanical, electrical, and optical connections on the same surface. Currently, copper-through silicon vias (Cu-TSVs) are being widely demanded for the system integration because of the low electromigration and high conductivity of Cu [15]. On the other hand, gold stud bumps (Au-SBs) have been utilized in microelectronics packaging [3] for a long time. The bonding between Au-SBs and Cu-TSVs allows three-dimensional integration with reduced interconnection distance resulting in lower signal delay and higher reliability compared to the traditional solder bumping bonding [3]. However, the bonding between Au-SBs and Cu-TSVs has not yet been investigated using the SAB because of constraints induced from size, shape, and surface roughness. In practical applications, the wafer bonding and interconnection involve materials with a wide range of surface roughness. In addition, silicon direct bonding has been widely used in the fabrication of silicon-on-insulator substrate, optoelectronic devices and three-dimensional MEMS packaging [4, 8, 10]. For these applications, direct bonding of silicon requires high bonding strength at room temperature without interfacial voids.

This paper reports the development of a surface activation-based NBIS with its functionalities for heterogeneous wafer bonding as well as interconnection. Interconnection between rough surfaces of Cu-TSVs and Au-SBs, and bonding between smooth surfaces of silicon (Si) wafers have been demonstrated as the first step to achieve three-dimensional (3D) heterogeneous integrated systems on the same surface using NBIS. Preliminary results on the bonded interfaces are included.

Development of NBIS

Structure and operation of NBIS

Figures 1(*a*) and (*b*) show the optical image and schematic diagram of the NBIS equipment, respectively. The NBIS accommodates specimens as big as 2 inch wafers. The NBIS consists of a load lock chamber and a bonding chamber separated by a gate valve. The load lock chamber has a six-stage elevator to hold the specimens. The chip with topside face down and the substrate with topside face up were placed in the jigs and loaded in the elevator of the load lock chamber. The jigs hold the chip and substrate and maintain their external shapes. The jigs have mechanical and electrostatic chucking capabilities on the bonding head and the lower stage. The door of the load lock chamber was closed and the chamber was vacuum pumped. As soon as the vacuum pressure was decreased to 10^{-6} Pa, the gate valve was opened and an automated transfer rod was used to transfer the specimens from the load lock chamber to the bonding chamber. An ultrahigh vacuum (UHV) pressure ($\sim 10^{-7}$ Pa) was maintained in the bonding chamber using a high efficiency turbo molecular

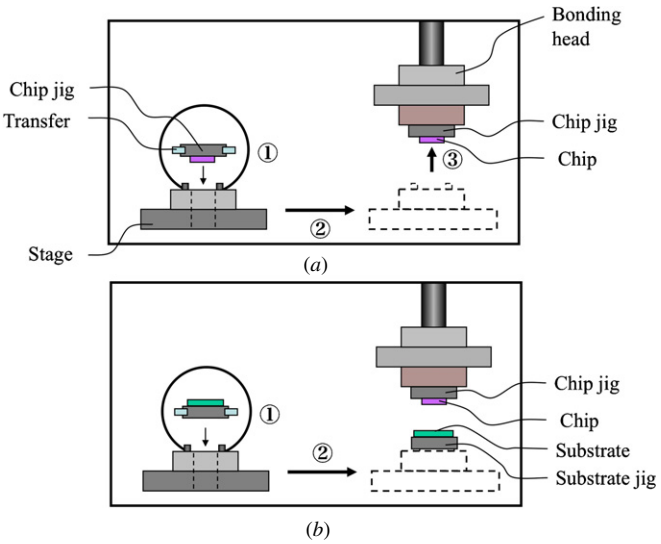


Figure 2. Schematic diagrams for positioning of (*a*) the chip and (*b*) the substrate.

pump (TMP), and titanium sublimation pump. As shown in figure 2(*a*), the jig with chip was temporarily placed on the stage of the rail in the bonding chamber and moved the rail in order to bring the stage under the bonding head. The chip jig (top specimen) was held by the piezoelectric bonding head. The rail was then returned to the front location of the load lock chamber. The substrate jig (bottom specimen) was transferred from the load lock chamber and placed on the stage, as shown in figure 2(*b*). On the top of the electrostatic chuck, a heater was equipped that allows heating up to 150 °C.

Surface activation

Figure 3 shows that the top and bottom specimens were activated using either argon (Ar) fast atom beam (FAB) or Ar-low energy ion bombardment in the bonding chamber. Two FAB sources are installed at 45° in the bonding chamber to activate the top and bottom wafers. The activation energy and current of the Ar-FAB sources are 1.5 keV and 48 mA, respectively. The single Ar-low energy ion source was installed in the bonding chamber, which allows activation of the top and bottom specimens simultaneously. The activation energy and current of the ion source are 80 eV and 3 A, respectively. The surface activation in the ion gun was done from the side of the specimens. The amount of gas was 100 standard cubic centimeters per minute (sccm) in both methods. During the activation, the pressure of the chamber was about 10^{-2} Pa. The energy of the Ar-ion source is much lower than that of the FAB, but the power of the Ar-FAB is lower than that of the Ar-ion source. Also, while the FAB had strong directional characteristics, the ion source beam had circular with directional characteristics resulting in exposing the beam over a wider area than the specimen (see figure 3).

Alignment procedure

After surface activation, alignment between the chip and the substrate was done using alignment marks. The bonding

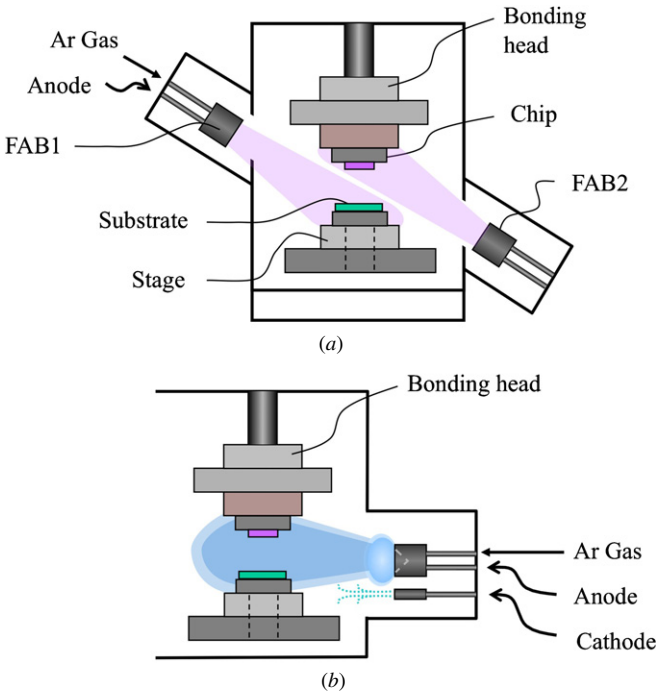
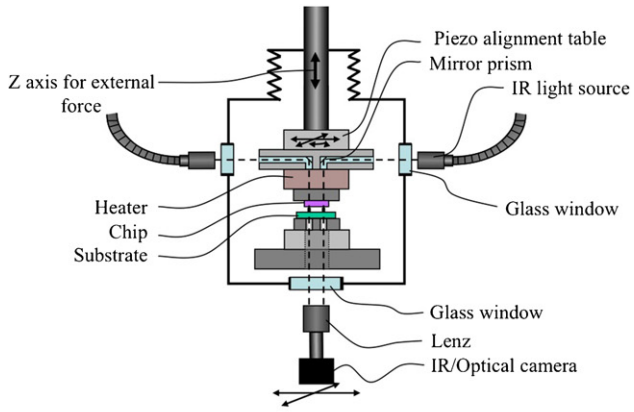


Figure 3. Schematic diagrams of surface activation systems using (*a*) two Ar-FAB sources and (*b*) an Ar-low energy ion source.

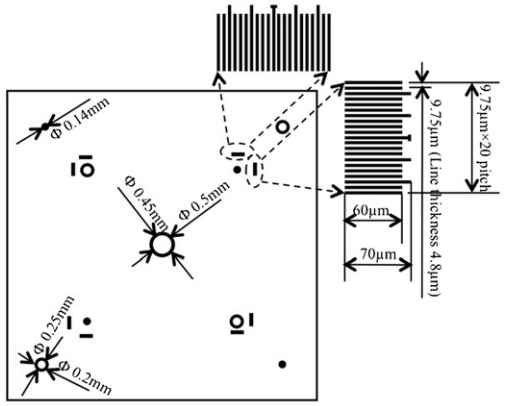
chamber was equipped with a high precision alignment system, as shown in figure 4(*a*), which consisted of an optical and an infrared (IR) transmission camera to detect the alignment marks of the substrate and the chip. The optical camera was located outside the bonding chamber above the position where the specimens were received on an automated rail. The IR/optical camera was located outside the bonding chamber underneath the bonding head. A special type of glass was used for the window of the IR camera. The piezo elements attached to the bonding head and the *Z*-axis units attached to the piezo table were used to perform the parallel adjustment function of the top and bottom wafers.

The position of alignment marks on the chip and substrate was recorded through optical and IR transmission and the displacement in the alignment was confirmed by image data processing (figure 4(*b*)). The displacement was corrected by a piezo actuator, and by repeated runs, sub-micrometer alignment accuracy would be achieved. The use of the piezo actuator is very important to carry out the alignment. In the UHV chamber, a servomotor or LM (linear motion) bearings cannot be used due to issues such as gas emissions caused by grease or heat resistance caused by the baking heater temperature. Therefore, a heat resistant structure comprising a six-shaft piezo actuator was developed that can withstand up to 150 °C baking without gas emissions. Moreover, the cameras were placed outside the chamber in order to maintain an ultrahigh vacuum in the bonding chamber. The placement of the cameras results in a longer working distance of the lens, which is approximately at 20 cm. So cameras with large magnification, such as microscopic lenses, could not be used.

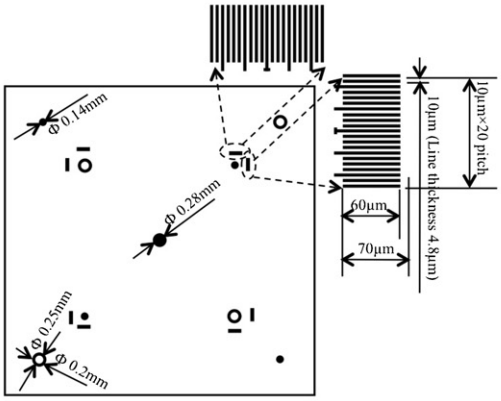
For the measurements of alignment accuracy, four sets of Au alignment marks were fabricated on the silicon substrate



(*a*)



(i) Alignment mark on the substrate



(ii) Alignment mark on the chip

(*b*)

Figure 4. Schematic diagrams for (*a*) the alignment system of NBIS and (*b*) alignment marks on (i) the substrate and (ii) the chip.

and the silicon chip, as shown in figure 4(*b*). They are shown as a filled circle (first), an unfilled circle (second), a filled circle with 21 discrete lines on the top or bottom corresponding to right or left, respectively (third), and an unfilled circle with 21 discrete lines on the top or bottom corresponding to left or right, respectively (fourth). The dimension of the first set was 140 μm diameter. The dimensions of the second set were the inner and outer diameters of 200 and 250 μm, respectively. The dimensions of the third set were the same as the diameters of the first set including the discrete lines with 9.75 (for the substrate) and 10 μm pitch (for the chip). The dimensions of the fourth set were the same as the diameters of the second set including the discrete lines with 9.75 (for the chip) and 10 μm pitch (for the substrate). The width of discrete lines was 4.8 μm. In addition, an unfilled circle of inner and outer diameters 450 and 500 μm and a filled circle of diameter 280 μm were prepared at the center of the substrate and chip, respectively. The captured images using the IR camera were processed by the image recognition method. In the image recognition method, sub-pixel processing with an accuracy of 1/40 pixel can be done using matching of alignment marks in the gray scale. The use of this method provides a better resolution than that in the IR light. In general, there are two methods for image processing: the data from alignment marks are converted into either (1) a binary format image, or (2) an image with the 64-level gray scale. The gray-scale processing is more suitable than the former method for the blurry image of alignment marks taken by the IR camera, because the edges of the blurry IR images can be characterized by the gradient of gray-scale levels. At each segment of the images' edge, the vectorized data of the gray-scale levels are correlated to get unique outline information of the alignment marks. Thus the pattern matching of the outline information between the alignment marks results in sub-micrometer alignment accuracy independently of the shape of the alignment marks. Table 1 shows the IR transmitted alignment accuracy of the alignment system of the NBIS. In table 1, X, Y, and θ indicate the accuracy in the planar and rotational directions. After alignment and image processing, the 3σ accuracies in the IR transmission alignment system were 0.09 μm, 0.18 μm and 0.0016°, respectively. If the specimens are opaque, the alignment can be done using the optical system. In this case, the alignment accuracy is ± 5 μm.

Table 1. IR transmitted alignment accuracy of X, Y and θ for the NBIS.

Alignment repeats	X (μm)	Y (μm)	θ (°)
1	−0.08	−0.07	0.000 25
2	−0.13	0.19	0.000 35
3	0	0.18	0.000 49
4	−0.11	−0.08	0.002 73
5	−0.09	0.02	0.002 47
6	−0.09	0.04	0.001 87
7	−0.17	−0.13	0.000 21
8	−0.17	−0.16	0.000 58
9	−0.11	−0.07	0.000 26
10	−0.01	0	0.002 63
Maximum	0	0.19	0.002 73
Minimum	−0.17	−0.16	0.000 21
Range (±)	0.085	0.175	0.001 26
σ	0.06	0.12	0.0011
3σ (±)	0.09	0.18	0.0016

Bonding procedure

Figure 5 shows the schematic diagram of the bonding chamber of NBIS. After the alignment, the top specimen was brought down, and contacted with the bottom specimen under an external force. The external force can be as high as 1000 N

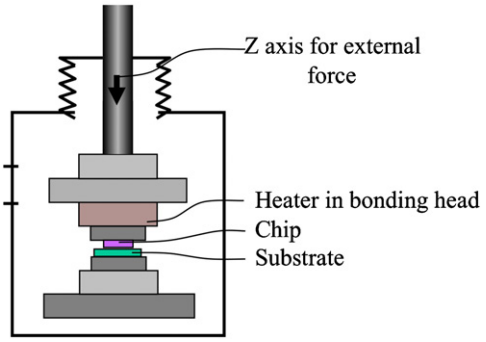


Figure 5. Schematic diagram of the bonding chamber of NBIS.

over an area with 50 mm diameter, which can be applied during bonding with and without heating at 150 °C. Then the jig on the bonding head was released. The top and bottom jigs with the bonded specimens were left on the stage and discharged to the elevator in the load lock chamber, using the transfer rod, and the rail in the bonding chamber. Finally, the bonded specimens were removed after venting the load lock chamber. As a first step of the long-term goal to realize the interconnection as well as bonding on the same substrate using the NBIS, the Cu-TSVs were vertically integrated with the substrate of Au-SBs, and the silicon wafers were bonded separately. These individual bonding experiments facilitate interconnection as well as bonding on the same substrate.

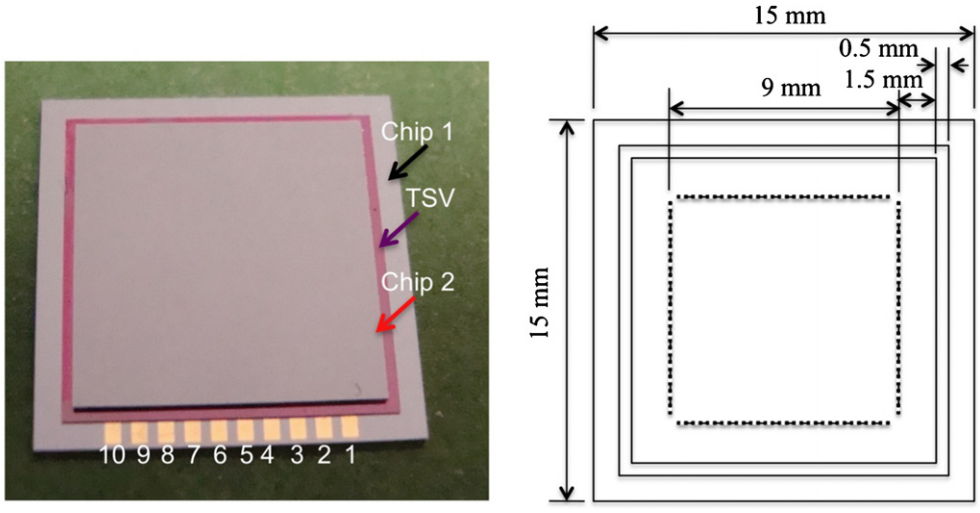
Bonding specimens of Cu-TSVs and Au-SBs preparation

Figure 6 shows the optical image and schematic diagrams of the vertically sandwiched Cu-TSVs between chip 1 and chip 2 with Au-SBs. The dimensions of chip 1, TSV chip and chip 2 were 15 × 15, 13 × 13, and 12 × 12 mm^2, respectively, as shown in figure 6(*b*). The Au-SBs and Cu-TSVs were located 4.5 mm from the center of the chips. The numbers of both Au-SBs and Cu-TSVs were 120 (figure 6(*b*)). Each Cu-TSV was bonded with top and bottom Au-SBs. The standard Cu-TSVs and Au-SBs were used for the bonding experiments. For Cu-TSVs, the vias in silicon were filled with Cu using an electroplating technique. The height and diameter of the Cu-TSVs were 150 and 55 μm, respectively. Silicon oxide with thickness 1 μm was deposited in the vias before Cu filling in order to isolate the Cu-TSVs. The Au-SBs were fabricated by the ultrasonic bonding of Au wire on Au bump on silicon. The base diameter and height of the Au-stud bump were 50 and 37 μm, respectively.

Bonding results and discussion

Cu-TSVs–Au-stud bumps bonding

One of the challenges of wafer bonding and interconnection in the SAB is the surface roughness. In the SAB, for room temperature bonding the requirement of the surface roughness in root mean square is less than 1 nm. In fact, Au-SBs have an oval shape at the top surface and do not allow bonding (figure 7(*a*)). In order to improve the surface roughness, the specimen was flattened using 20 N of external force over the chip (0.16 N/bump). Therefore, the external compressive pressure over each bump was about 40 MPa. Figures 7(*a*), (*c*) show the scanning electron microscope (SEM) (from JEOL) images of Au-stud bump before and after deformation (applying external force), (*b*) shows the optical image and (*d*), (*e*) show the atomic force microscope (AFM) (ICON from Veeco) images of one Au-stud bump after deformation with an external force of 20 N. After flattening the surface, the size (diameter) of the top surface was about 35 μm, which consisted of deformed and non-deformed areas. The surface roughness of the deformed and non-deformed areas over 10 × 10 μm^2 was 9.6 and 36.1 nm, respectively. Figure 8 shows the optical and AFM images of Cu-TSVs. The surface roughness of the



(*a*) (*b*)

Figure 6. (*a*) Optical image and (*b*) schematic diagram of the vertically integrated system with locations of Cu–TSVs and Au-SB. The Au-SB of chip 2, and Au-SB with probe electrodes of chip 2 are bonded on the top and bottom of the TSV chip.

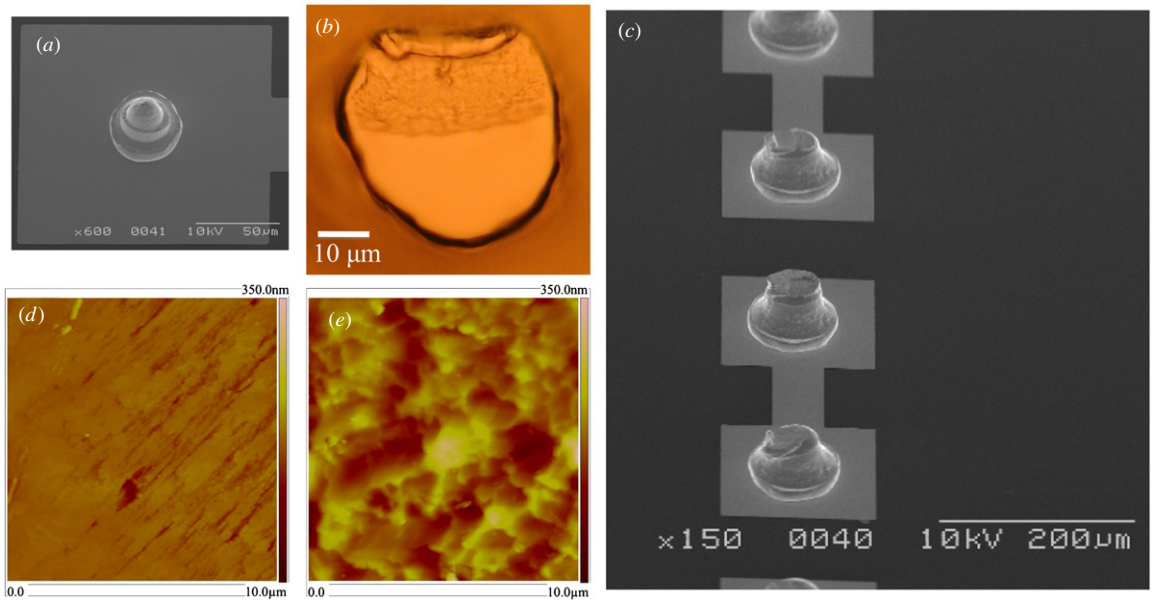


Figure 7. (*a*) SEM image of one Au-stud bump, (*b*) optical image of one Au-stud bump after deformation with external force of 20 N, (*c*) SEM image of Au-SB after deformation, (*d*) and (*e*) AFM images of one Au-stud bump with deformed and non-deformed areas after deformation. The scan area of AFM image is $10 \times 10\ \mu m^2$.

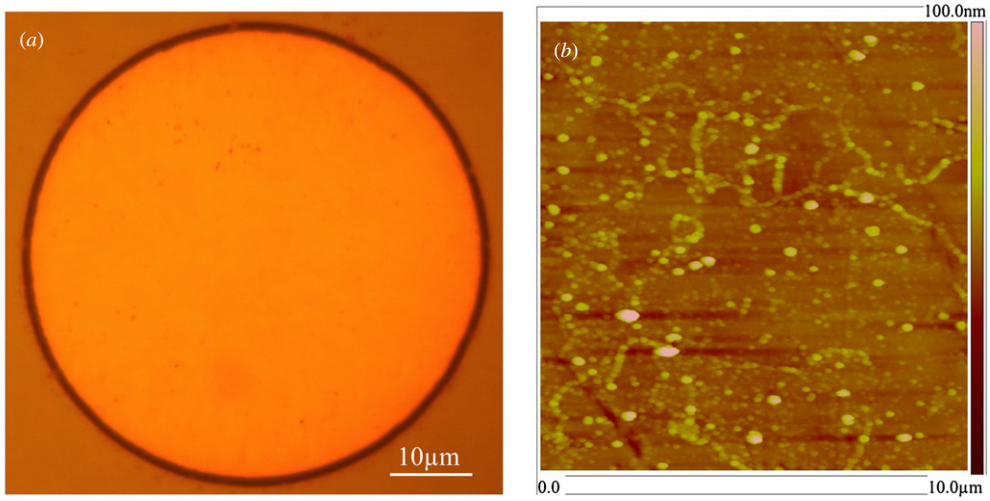


Figure 8. (*a*) Optical image and (*b*) AFM image of Cu-TSVs surface. For AFM image, the scanned area is $10 \times 10\ \mu m^2$.

TSV over an area of $10 \times 10\ \mu m^2$ was 6.0 nm. Therefore, the amplitude of the surface roughness of both Au-bumps and Cu-TSVs was higher than that of the requirement in the SAB.

Figure 9(*a*) shows a typical example of the optical image of the cross-sectional view of the bonded interface of Au-stud bump and Cu-TSV that were bonded with an external bonding force of 20 N at room temperature. There was no considerable misalignment between the bumps and TSVs were observed throughout the whole bonding area. The bonding strength was investigated using a tensile strength tester from Instron. After the tensile pulling test, fracture was not observed at the bonded interface but in the bulk of Au bumps. The fractured Au bump remained on the Cu-TSV, as shown in figure 9(*b*). The estimated bonding strength of Cu-TSV/Au-SB was 110 ± 10 MPa. Recently, for 3D assembly at room temperature, the mechanical-caulking technique has been used to bond Au-SBs with TSVs through squeezing the former into the latter by applying compressive pressure. This pressure has caused plastic deformation into the gold bumps due to their skirted shape and resulted in electrical connections between the bumps and TSVs on the sidewall [6]. The compressive pressure is about 150 MPa, which is about 3.5 times higher than that of the pressure used in this study. Also, the electrical contact between Au-SBs and Cu-TSVs has been intensively investigated elsewhere and confirmed the electrical conduction among bonded interfaces of 120 Au-SBs and Cu-TSVs [16]. The electrical resistance of the interface (i.e. two interfaces of Au-SBs and Cu-TSVs including the height of one Cu-TSV) was as low as 0.5 Ω [16]. Five sets of vertically integrated specimens of Cu-TSVs/Au-SBs were prepared using the NBIS. In each set, first, chip 2 (Au-SBs) was bonded with one side of the Cu-TSV chip and then the other side of the

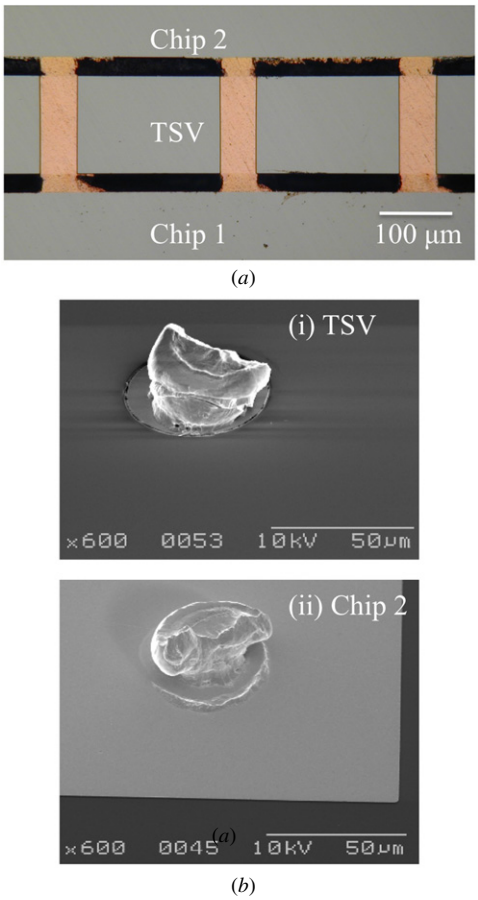


Figure 9. (*a*) Optical image of vertically integrated the Au-stud bump and the Cu-TSV interface under an external force of 20 N and (*b*) fracture images of (i) Cu-TSV and (ii) Au-stud bump on chip 2 after tensile pulling test.

Cu-TSV chip was bonded with chip 1 (substrate). One set of the specimens failed because of unexpected misalignment (∼20 μm) between the unbonded side of the TSV chip and chip 1 which was due to narrow gap between them during IR alignment. The yield of Cu-TSVs/Au-SBs bonding was 90%. The bonding of the rough surfaces of Au-SBs and Cu-TSVs is attributed to the surfaces free from native oxides and carbon contaminations [12] with higher contact area under comparatively lower external compressive force. Therefore, the bonding between rough surfaces at room temperature and low bonding pressure can be applied for low-cost solution for high-density interconnection of the systems [17].

Silicon wafer bonding

Figure 10 shows AFM images of silicon surface before activation (*a*), after activation using 1.5 keV and 48 mA, Ar FAB ions, for 300 s (*b*) and after activation using the 80 eV and 3 A ions source for 300s (*c*) and 1200 s (*d*). The quantitative values of the surface roughness relevant to figure 8 along with those of other activation times in both the FAB and the ion source are shown in table 2. In the FAB activation, the surface roughness was not significantly changed up to 1200 s. On the other hand, the surface roughness was insignificantly

Table 2. Comparative studies of the surface roughness of the silicon wafer in the FAB and Ar-low energy ions source activation with different activation time.

Activation time (s)	Activation energy (eV)		Activation current (A)		Surface roughness (nm)		Relevant figures	
	FAB	Ion	FAB	Ion	FAB	Ion	FAB	Ion
0			0		0.17		*a*	
60					0.18	0.15	–	–
90					0.16	0.13	–	–
180					0.13	0.12	–	–
	1500	80	0.048	3				
300					0.11	0.09	*b*	*c*
600					0.21	0.19	–	–
1200					0.20	0.55	–	*d*

decreased in the ion source activation up to 300 s, but it was abruptly increased from 600 to 1200 s (figure 10(*d*)). The surface roughness of the 300 s activated specimen in the FAB and ion source activation was 0.11 and 0.09 nm, respectively, which is indicative of smooth surfaces of silicon wafers, as shown in figures 10(*b*) and (*c*) and table 2. As previously mentioned, this is attributed to the removal of native oxides and carbon contaminants and particles from the surface. Once activated surface is achieved, further treatment causes rough surface (see the specimen activated for 1200 s using the ion source) in both methods. The high surface roughness of silicon in the ion source activation compared to that in the FAB is due to the higher power of the ion source as well as particles generated during activation from the surrounding which stick on the surface. Therefore, this study indicates the bonding feasibility not only on the smooth surfaces of silicon/silicon wafers without heating [18, 19] but also on the rough surfaces of Au-SBs and Cu-TSVs.

Figure 11 shows the IR images of the silicon/silicon interface bonded after activation with the Ar-FAB in comparison with the Ar-low energy ion beam. The activation time in both methods was 300 s. While the interface in the Ar-FAB method showed no voids, few voids appeared in the ion beam method. As previously mentioned, the ion source spreads the beam over the area in contrast to the FAB. Therefore, particles from the surrounding (during activation in the bonding chamber) stick on the surface which generates voids only in the ion beam activation method. Recently, the post-bonding annealing influence on the interfacial voids of silicon/silicon activated using the Ar-FAB has been investigated. No voids have been observed up to annealing at 600 °C [20].

Figure 12 shows the tensile strength of the silicon/silicon interface in the FAB activation method for different activation times compared with the ion source activation method. In the figure, FAB and IG stand for the fast atom beam and ion gun, respectively. Time dependence of tensile strength in both methods was observed. In the FAB activation method, the tensile strength rapidly increased to a maximum value of 18 MPa from 60 to 180 s. This value remained constant for the specimen activated for 300 s and was then reduced by 50% at 600 s. In the ion activation method, the tensile strength

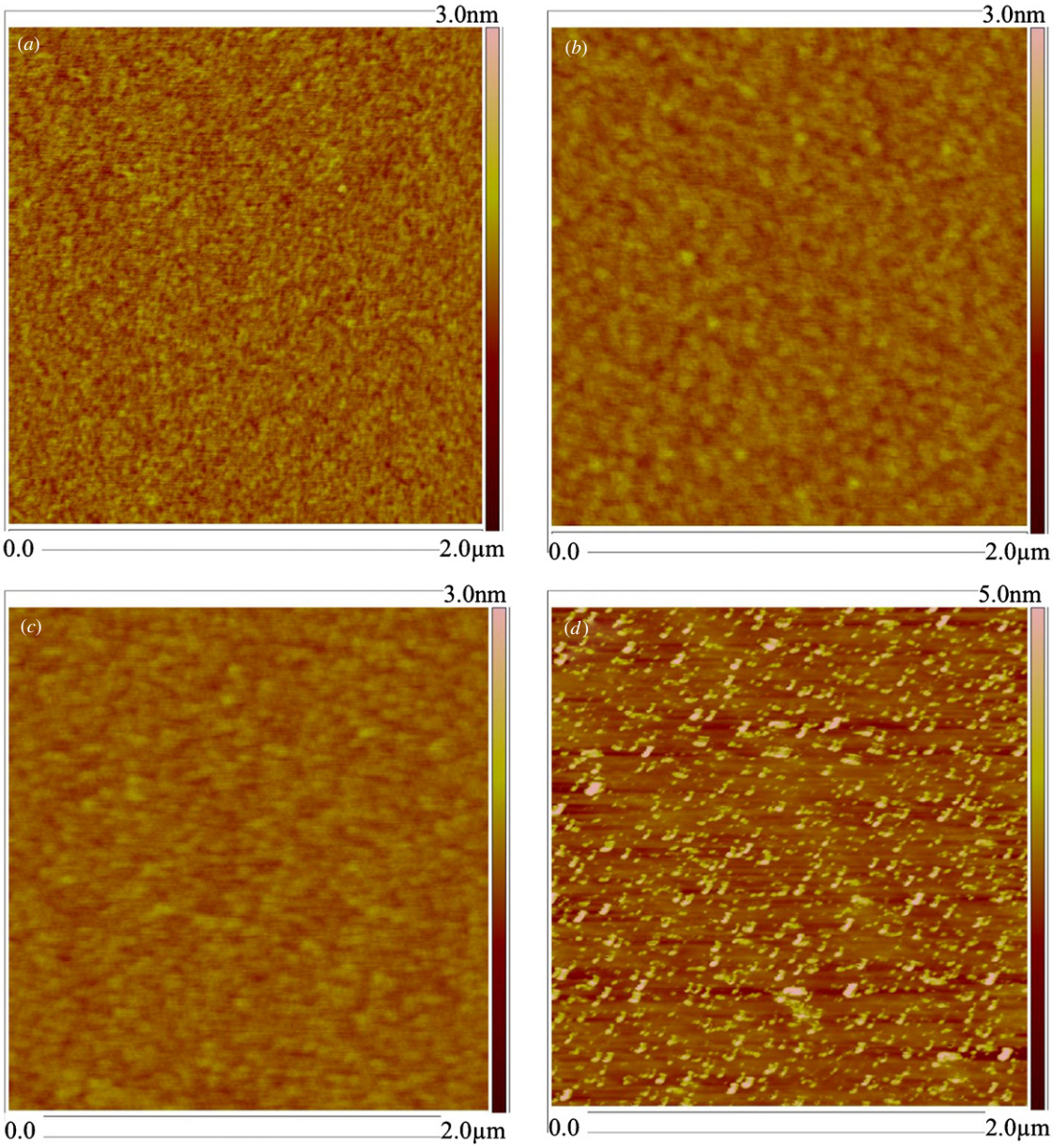
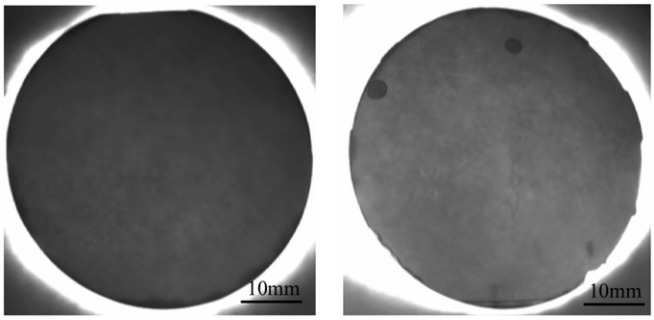


Figure 10. Atomic force microscopy (AFM) images of silicon surface (*a*) before activation, (*b*) after activation using the FAB ion source with 1.5 keV and 48 mA for 300 s, after activation using the Ar-low energy ion source with 80 eV and 3 A for (*c*) 300 s and (*d*) 1200 s.

proportionally increased with increasing activation time up to 300 s, and at 180 s the tensile strength was almost half of the value in the FAB activation. After that, the bonding strength suddenly dropped at 600 s. This reduction was about ten times lower than that in the FAB activation. The time-dependent behavior of the bonding strength in each method is due to the roughness of the activated surface (table 2). Also, prolonged surface activation may reduce the hardness of the silicon wafer due to the radiation effect of Ar ion implantation [21]. The surface activation time (i.e. 300 s) at maximum bonding strength in the Ar-FAB activation method is relatively higher than that in the previous report [14]. This is due to differences in the distance and angle between the source and specimens. Also, the activation energy and background vacuum pressure are different. Furthermore, the high bonding strength and smooth surface in the prolonged activated specimen indicate the feasibility of sequentially bonding many chips on the same wafer surface. On the other hand, in order to evaluate the high-temperature applicability of the silicon/silicon bonded interface [22], the bonded wafers activated using the Ar-FAB have been annealed up to 600 °C and the bonding strength has been unchanged [20]. Therefore, the void-free interface of silicon/silicon with bonding strength equivalent to bulk fracture of the wafers achieved in both methods can be applied not only for low-temperature but also for high-temperature MEMS packaging.

Figure 13 shows (*a*) the fracture image and (*b*) the HRTEM image of silicon/silicon bonded interface in the FAB. The activation time was 300 s. Voids or defects, except in the amorphous layer, were not observed across the interface. The



(*a*) (*b*)

Figure 11. IR images of 2 inch silicon/silicon interfaces for the surfaces treated using (*a*) the 1.5 keV and 48 mA Ar-fast atom beam and (*b*) the 80 eV and 3 A Ar-low energy ion source for 300 s.

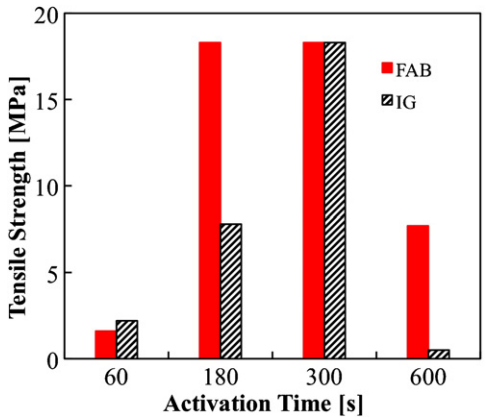


Figure 12. Time dependence of the tensile strength of silicon/silicon bonded after surface activation using the fast atom beam (FAB) and the low-energy ion source at room temperature.

thickness of the interfacial amorphous layer was 8.3 nm. The interfacial amorphous layer was caused by the Ar ion induced surface damage during activation [12, 23]. Despite the presence of the amorphous layer at the bonded interface, high bonding strength was achieved, as previously shown (figure 12). This implies that the interfacial amorphous layer does not have an influence on bonding strength. Identical thickness was observed at the silicon/silicon bonded interface in our previous study before annealing [14].

Conclusions

A flip chip NBIS bonder with high precision alignment has been developed to bond chips and wafers with sizes ranging from 5 × 6 mm^2 to 50 mm in diameter. The NBIS was built on the Ar-FAB and the Ar-low energy ion beam based SAB method. The rough surfaces of Cu-TSVs and Au-SBs were interconnected at room temperature and low external force after surface activation using the Ar-FAB with 1.5 keV energy and 48 mA current. On the other hand, smooth surfaces of silicon wafers of 50 mm diameters were bonded without heating after activation using both the Ar-FAB and Ar-low energy ion beam. The void-free silicon/silicon interface with bonding strength equivalent to bulk fracture of silicon was achieved. A few nm thick amorphous layers were observed across the silicon/silicon interface that was fabricated by the Ar-FAB; however, they appear to have no effect on bonding strength. This investigation shows that the NBIS bonder can be utilized for high-density interconnection and MEMS packaging.

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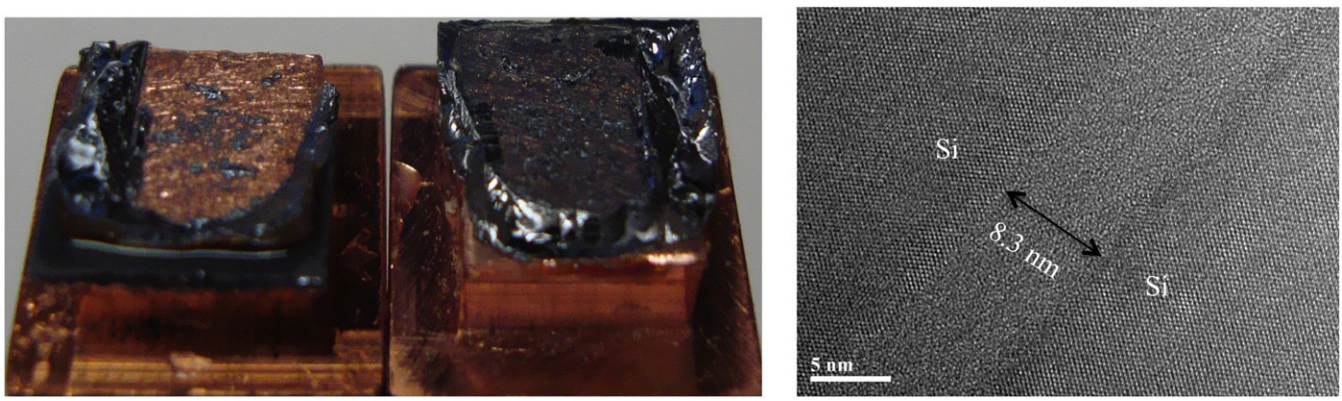

(*a*) (*b*)

Figure 13. (*a*) Fracture images and (*b*) nanostructural behavior of the silicon/silicon interfaces prepared in the FAB activation methods.

References

[1] International Technology Roadmap for Semiconductors (ITRS) 2007

[2] Wang T D and Dam J V 2004 *Clin. Gastroenterol. Hepatol.* **2** 744

[3] Chuang C L, Aoh J N, Liao Q A, Hsu C C, Liao S J and Huang G-S 2008 *J. Electron. Mater.* **37** 1742

[4] Cheng Y T, Lin L and Najafi K 2000 *J. Microelectromech. Syst.* **9** 3

[5] Song S, Holl S, Colinge C, Byun K Y, Hobart K and Kub F 2008 *ECS Trans.* **16** 287

[6] Tanaka N *et al* 2009 *IEEE Trans. Adv. Packag.* **32** 746

[7] Lai S, Lin H and Hu C 2004 *Mater. Chem. Phys.* **83** 265

[8] Dragoi V, Mittendorfer G, Thanner C and Lindner P 2008 *Microsyst. Technol.* **14** 509

[9] Huang Z R, Guidotti D, Wan L, Chang Y J, Yu J, Liu J, Kuo H F, Chang G K, Liu F and Tummala R R 2007 *IEEE Trans. Compon. Packag. Technol.* **30** 708

[10] Miki N, Zhang X, Khanna R, Ayón A A, Ward D and Spearing S M 2003 *Sensors Actuators* A **103** 194

[11] Jeung W K, Lim C H, Yuan J and Park S W 2008 *DTIP MEMS MOEMS—Symp. Design, Test, Integration Packaging MEMS/MOEMS* p 201

[12] Howlader M M R, Suga T, Zhang F, Lee T H and Kim M J 2010 *Electrochem. Solid-State Lett.* **13** H61

[13] Howlader M M R, Suga T and Kim M J 2006 *Appl. Phys. Lett.* **89** 031914

[14] Howlader M M R, Okada H, Kim T H, Itoh T and Suga T 2004 *J. Electrochem. Soc.* **151** G461

[15] Kamto A, Liu Y, Schaper L and Burkett S L 2009 *Thin Solid Films* **518** 1614

[16] Howlader M M R, Zhang F and Kibria M G 2010 *J. Vac. Sci. Technol.* A submitted

[17] Cale T S, Lu J Q and Gutmann R J 2008 *Chem. Eng. Commun.* **195** 847

[18] Conrad D, Scheerschmidt K and Gosele U 1996 *Appl. Phys.* A **62** 7

[19] Gosele U, Stenzel H, Martini T, Steinkirchner J, Conrad D and Scheerschmidt K 1995 *Appl. Phys. Lett.* **67** 3614

[20] Howlader M M R and Zhang F 2010 *Thin Solid Films* **519** 804

[21] de Boer W, Bol J, Furgeri A, Muller S, Sander C, Berdermann E, Pomorski M and Huhtinen M 2007 *Phys. Status Solidi* **a 204** 3004

[22] Kruger S and Gessner W 2002 *Advanced Microsystems for Automotive Applications* (Berlin: Springer) p 253

[23] Takagi H, Maeda R, Hosoda N and Suga T 1999 *Japan. J. Appl. Phys.* **1 38** 1589