Review

Low-Temperature Bonding for Silicon-Based Micro-Optical Systems

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Abstract: Silicon-based integrated systems are actively pursued for sensing and imaging applications. A major challenge to realize highly sensitive systems is the integration of electronic, optical, mechanical and fluidic, all on a common platform. Further, the interface quality between the tiny optoelectronic structures and the substrate for alignment and coupling of the signals significantly impacts the system's performance. These systems also have to be low-cost, densely integrated and compatible with current and future mainstream technologies for electronic-photonic integration. To address these issues, proper selection of the fabrication, integration and assembly technologies is needed. In this paper, wafer level bonding with advanced features such as surface activation and passive alignment for vertical electrical interconnections are identified as candidate technologies to integrate different electronics, optical and photonic components. Surface activated bonding, superior to other assembly methods, enables low-temperature nanoscaled component integration with high alignment accuracy, low electrical loss and high transparency of the interface. These features are preferred for the hybrid integration of silicon-based micro-opto-electronic systems. In future, new materials and assembly technologies may emerge to enhance the performance of these micro systems and reduce their cost. The article is a detailed review of bonding techniques for electronic, optical and photonic components in silicon-based systems.

Keywords: hybrid integration; low-temperature bonding; silicon photonics; optical detection systems; surface activated bonding

1. Introduction

Silicon (Si)-based micro-optical systems are of great importance for environmental and healthcare applications. Such systems, which can be highly integrated, enable fast and efficient signal acquisition and data processing. In addition, the fabrication of Si-based devices is compatible with parallel processing which can potentially lower the cost. One practical example of such system is the early diagnosis and monitoring of human diseases using autofluoresnce or fluorescence lifetime imaging [1]. Another example is a bioanalytical sensing system that allows detection and monitoring of Escherichia coli cell in food and water [2]. One of the challenges for such systems is to integrate optical, electrical, and fluidic components on a single platform. In addition, these systems should be portable, easy-to-use, power efficient, and low-cost. Therefore, fabrication, integration and assembly of components or modules in a small form factor are required, but this is not easy to realize in practice.

One of the challenges to realize the highly-integrated systems is the electrical interfacing among the components and modules. It is required for the transmission and distribution of electrical power and data signal. The data rate for the integrated optical systems is expected to be 80 Tb/s to 780 Tb/s by 2022 [3]. In such high-speed systems including electronic components, the geometries and materials for electrical interconnects must be carefully designed to optimize their high frequency performance [4]. In general, interconnects with smaller dimensions can help to reduce electrical resistance, capacitance and/or inductance to improve the high-frequency performance.

Another challenge for systems integration is the optical interfacing among optical components. It is required for transmitting optical signals. The quality of optical interfaces is determined by the extent of matching between the electromagnetic fields of the optical sources, detectors and waveguides. A high coupling efficiency is required for transferring optical energy efficiently across the interface between the coupled components. For example, since the relative position offsets between the optical source and detector control coupling loss [5], their alignment accuracy during integration is critical. Briefly, passive alignment using groove structures is more practical than active alignment for commercial micro-optical systems.

Currently, wafer bonding technologies are used to attach two or more substrates with different functional components, and are being used for the electrical interconnection and optical coupling [6]. These technologies provide bonding of devices with small dimensions and short interconnects throughout the wafers. Also, these technologies offer high throughput and low cost, because all components on the same wafer are processed in parallel [7]. Therefore, the total cost of the parallel-processed product is lower than that of the products assembled discretely.

Bonding of Si wafers with direct band gap materials (III-V materials) offers the possibility to fabricate Si-based photonic devices such as laser diodes [8]. In this case, Si, as a substrate, guides the optical signals generated from the III-V materials, which have high optical gains. Also, it is important to integrate the optical devices with complementary metal-oxide-semiconductor (CMOS) circuits to read, process, store, and transmit obtained optical signals.

For the integrated optoelectronic systems, the development of suitable bonding technologies for Si wafers is one of the critical steps. Unfortunately, current bonding technologies, such as fusion bonding [9] or thermo-compression bonding [10], do not provide the following properties at the same time: (1) high bonding strength, (2) high electrical conductivity, (3) hermetic sealing, (4) high transparency of

the bonded interface, and (5) low thermomechanical stress in the bonded components. Also, since many optoelectronic systems operate at a temperature lower than the temperatures used for fusion and thermo-compression bonding, the mismatch of coefficient of thermal expansion (CTE) of different materials would introduce alignment error during bonding. The misaligned components would result in degraded system performance. Moreover, the CTE mismatch between metal coating and Si-based micromirrors causes unwanted mirror wrapping and bowing [11,12]. Therefore, low-temperature bonding for the integration and assembly of optical detection systems is required. Indirect bonding uses intermediate layers such as solders, metals, and adhesives. In contrast, direct bonding uses atomic forces between the surfaces of mating pairs. Surface activated bonding (SAB) is an example of the direct wafer bonding [13]. The SAB technologies do not require high temperature, high pressure, and extra additives to provide bonding interface with high bond strength, high electrical conductivity and low optical loss [13–28].

There are optically sensitive materials such as carbon nanotubes (CNTs) [29], graphene [30], molybdenum disulfide (MoS_2) [31], tungsten disulfide (WS_2) [32], and organic polymers [33] to be integrated with Si-based optical systems. This integration offers highly-sensitive and power efficient systems because of the unique properties of the optical materials such as short response time and high photoresponsivity. Thus, advanced assembly methods for new materials are required to be developed. Monolithic integration and heterogeneous integration contribute to the advanced assembly concepts to further enhance the performance of devices and systems. Note that the targeted assembly cost for Si-based optical detection systems is majority of the overall cost [34]. This cost may be increased when new materials are to be integrated with Si.

In this article, we review in detail the fabrication, integration, and assembly of Si-based micro-optical systems using wafer bonding at low temperatures (below 450 °C). We focus on the electrical and optical interfaces in such systems. In Section 2, we present basic concepts and technologies for electrical and optical interfaces in micro-optical systems. In Section 3, we describe low-temperature wafer bonding technologies in detail, with emphasize on the SAB technologies. Different aspects of direct bonding without intermediate layers and indirect bonding with intermediate layers are explained. In Section 4, we identify different aspects, such as new materials, technologies, and cost, for future Si-based micro-optical systems.

## 2. Electrical and Optical Interfaces in Micro-Optical Systems

2.1. Electrical and Optical Interfaces

A typical microsystem requires electrical interconnects and optical coupling for the communication among neighboring components, as shown in Figure 1. This system consists of electronic, optical and photonic devices with packages. The electrical and optical interfaces help to attain system functions, performance, stability, and reliability. For example, the intensity of electrical signals in the system is affected by resistance of interconnects. Thus, the location, dimensions, and materials of electrical interconnects have to be well designed. In addition, the intensity of optical signals received by the detectors impacts the sensitivity and detection limit of the system. Therefore, precise alignment among

the optical components is indispensable to ensure efficient signal transmission. For this purpose, the electrical and optical connection in a Si-based microsystem will be discussed in detail in this subsection.
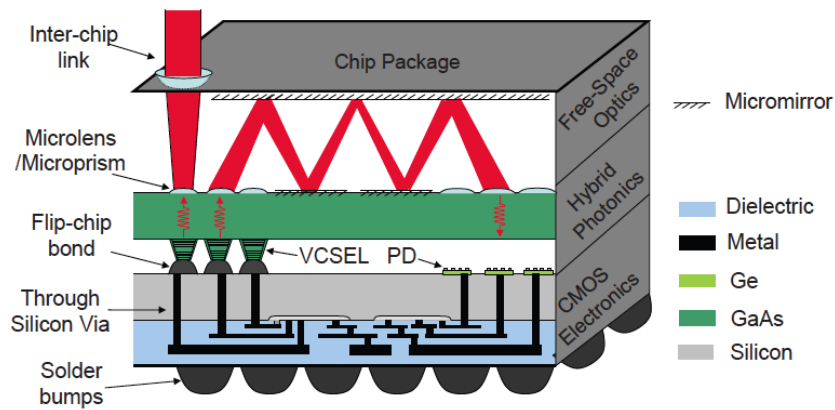

(**a**)
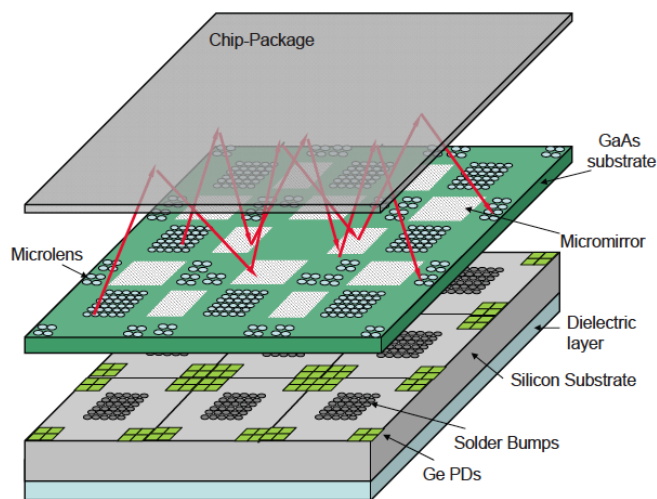
(**b**)

Figure 1. (**a**) Cross-sectional and (**b**) three-dimensional view of a typical microsystem that consists of electronic (*i.e.*, complementary metal-oxide-semiconductor (CMOS) transceivers and amplifiers), optic (*i.e.*, lenses and mirrors) and photonic (lasers and photodetectors) components with packages [35] (Reproduced with permission from Ciftcioglu *et al.*, *Opt. Express*; published by OSA, 2012).

2.1.1. Electrical Interconnects

Electrical interconnects are necessary for transmitting power and signals in many systems with electronic components. Propagation, delay, attenuation, noise, crosstalk and the rise and fall times have been observed in high frequency signals [36]. The electrical interconnects in a system with optical components should possess small time constant with low resistance. Also, the impedance between the signal sources and interconnects requires being matched [37]. Vertical interconnections, as one type of electrical interconnects, offer reduced resistance and parasitic parameters, and the device can also be densely integrated due to the reduced in-plane space [38]. Micro bumps and through-hole vias are needed

for vertical interconnections with small foot-print. The schematic of vertical interconnections using bumps and through-hole vias is shown in Figure 2.
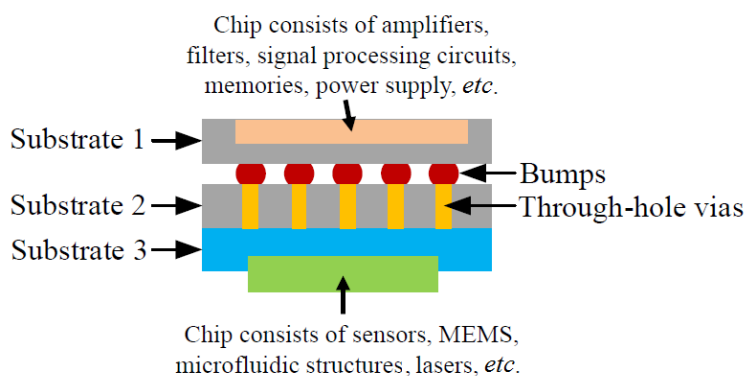
Figure 2. Schematic of vertical interconnections between bumps and through-hole vias for the components shown in Figure 1.

Bumps are formed in the last few steps of fabricating a component before it (substrate 1) is assembled onto target substrates (substrates 2 and 3 in Figure 2). Conducting adhesives and metals/alloys are generally being used to make bumps. Bumps made of conducting adhesives are not discussed here due to their low conductivity, although, in some studies, nanoparticles are added in polymer matrixes to enhance the conductivity, the conductivity is still lower than that of metal [39]. Bumps made of metals and eutectic alloys are mostly used because of their good electrical and thermal conductivity that reduces electrical power consumption, and increases heat dissipation. By controlling the size of the metal/alloy bumps, the capacitance and inductance of the interconnections could be minimized [40].

The diversity of the bump materials and substrates causes compatibility issues during heating steps in assembly. To address this issue, soft alloys, for example tin-lead (Sn-Pb), have been applied to reduce stress in the assembled devices and systems [41]. However, the European union regulations on the restriction of hazardous substances in electrical and electronic equipment stimulated the development of lead-free soldering and bumping technologies [42]. Lead-free alloys for bump materials include Sn-silver (Ag), Sn-Ag-copper (Cu), Cu-Sn, gold (Au)-Sn and Au-indium (In). Metallic bumps such as In and Au have also been used. Indium bumps are required for optical detection systems because of its low stress [43]. The low stress is attributed to its high ductility and low Young's modulus. This property is important for structures having mismatches in coefficient of thermal expansion (CTE). Besides, Gold micro stud bumps have been used to connect Si substrates with photonics materials such as $LiNbO_3$ [26].

Vacuum deposition and electroplating techniques are used to fabricate bumps, but the electroplating approach is now preferred because of its low cost. Electroplating has been demonstrated for making bumps with pitches of 40 μm [43,44], or even smaller [45]. Furthermore, special techniques in electroplating such as pulse plating or pulse reverse plating may improve the uniformity and consistency of the bump height throughout the wafer.

In addition to bumps, through-hole vias are required in vertical interconnections. Large-scale optical detector arrays were assembled in the form of sensing surface facing up, and the electrical signals were extracted from the back side of the chip using through-hole vias [46]. This approach does not sacrifice the sensing surface area of the front side and maximizes the fill-factor of the sensing component. The

vias can be vertically fabricated by etching, filling, and grinding through the substrates. The lengths of the interconnections are identical to the substrate thicknesses, thus this interconnection method can achieve high conductivity. Also, low parasitic capacitance, high breakdown voltage, and small leakage current can be realized when proper passivation techniques are used [46].

System integration using through-hole vias could be divided into three categories [13,47]: via-first, via-middle and via-last. In via-first processes, the components and filled vias are fabricated on different substrates before wafer bonding. During wafer bonding, structures to be aligned are close to bottom-level components, which are densely distributed and small in dimensions. Therefore, precise alignment is required but challenging. Also, high precision alignment is time-consuming. It reduces yield, increases processing complexity and cost. Similarly, via-middle process is carried out after the device fabrication but before metallization steps. The small and dense structures make the alignment challenging. On the other hand, the via-last processes are done at the last step in the assembly. Therefore, via-last approaches do not require precise wafer-to-wafer alignment during wafer bonding, thus reducing the processing complexity and cost.

2.1.2. Optical Coupling

A microsystem with optical components uses optical signals from optical sources, waveguides for signal transmission, and often detectors for signal detection (Figure 1). These components may be discrete or integrated. In the case of discrete components, optical coupling is realized between them. For practical applications, for example for detecting weak signals such as biological fluorescence, high coupling efficiency is one of the most important parameters of the interface. The coupling efficiency is affected by the position misalignment between optical sources, waveguides, and detectors, the numerical aperture mismatch of waveguides, and the refractive index mismatch between coupled components. Among them, misalignment between optical sources and detectors has a significant impact on coupling efficiency [5]. Thus, the optical source and detector have to be precisely aligned. Although the alignment tolerances of large diameter fibers may be relaxed for short distance optical interconnect systems [48], they are very tight for both lateral coupling (±0.3 μm for 1 dB decrease in coupling efficiency) and vertical coupling (±2 μm for 1 dB decrease in coupling efficiency) of small-size integrated systems. There are mainly two schemes to achieve optical alignment [49]: active alignment and passive alignment.

Active alignment (Figure 3a) has been demonstrated in an indium phosphide (InP) photonic device for an integrated wavelength division multiplexing transceiver [50]. In this approach, a lensed fiber was precisely aligned to the optical output using closed-loop optimization. It is a time consuming and expensive process with low throughput, especially when multiple fibers are to be connected.

Passive alignment (Figure 3b) is a promising strategy because of its short alignment time, high throughput, low cost, compatibility with micro-structures, and multichannel compatibility [26]. It may also eliminate the need for equalization circuits and transmission lines used in active alignment. In this approach, optically connected components can be densely assembled on one substrate using this approach [51,52]. However, the performance of systems assembled by passive alignment varies from each other. This variation is due to the reduced alignment accuracy resulting from the accumulated mechanical tolerance of the alignment machine [38].
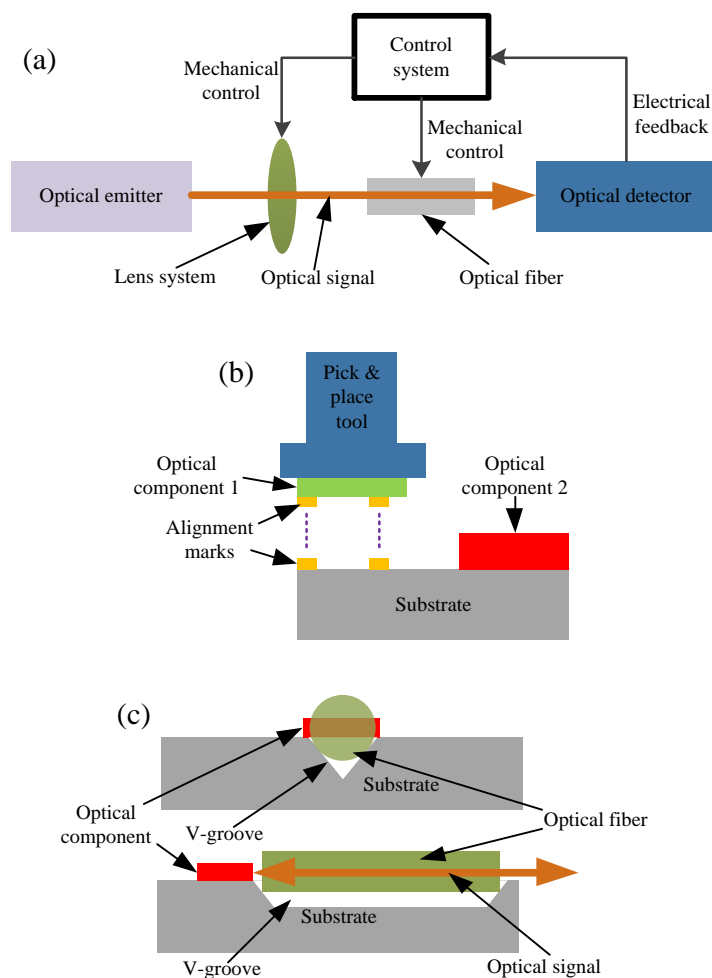
Figure 3. Schematic of optical alignment methods. (**a**) Close-loop active alignment; (**b**) Passive alignment using alignment marks; (**c**) Self-alignment using V-groove.

Several methods of low process complicity were developed to improve passive alignment accuracy. In the first method [53], the challenge in the planar alignment due to height differences of the optical components has been addressed. Firstly, the optical source and detector are mounted on a planar substrate with a mirror parallel to the substrate. When the optical signal is generated from the source, it is reflected by the mirror and finally recorded by the detector. By this process, coupling of optical signals in the vertical orientation through the edge of devices can be eliminated. In another study, the high temperature issue in alignment was addressed using low-temperature bonding to avoid re-melting of the bumps in highly integrated micro-optical systems. This method gets rid of the surface tensions of melted bumps (liquid state) that may displace connected structures [54,55]. Low-temperature integration technology based on passive optical alignment using SAB has been demonstrated to minimize alignment offset induced by mismatch of materials' CTE [56]. Germanium (Ge) [56] and LiNbO$_3$ [8] were bonded to Si by this method for the fabrication of micro-laser sources and micro-optical sensors. Finally, precise alignment through glass was demonstrated for optoelectronic modules. The benefits of this method were to utilize the dimensional stability under thermal load, transparency, and CTE matching to Si [57].

Besides active and passive alignment, a self-alignment concept for high-quality optical interface has been presented (Figure 3c) [38,58]. Firstly, a groove structure is fabricated on the substrate to hold the waveguide according to the position of the optical source/detector. The dimensions of the groove are

designed for fitting the waveguide (optical fiber in this example) with a certain diameter. Then, the optical fiber can be placed and fixed inside the groove. Finally, the alignment between the waveguide and the source/detector is automatically achieved by the specified position of the waveguide in the groove. The grooves could be a V-shape trench prepared by Si wet etching or a rectangular trench realized by Si deep reactive ion etching (RIE) [59]. In another study, low-cost devices like datacom modules have been fabricated using similar MEMS technologies [60].

2.2. Wafer Bonding for Electrical and Optical Interfaces

A schematic representation of a Si-based optical sensing microsystem is shown in Figure 4. It consists of an optical source, waveguides, gratings, detectors, electronics, a power supply and a wireless unit. All these components should be integrated on a single common platform for miniaturization. The electrical interfaces should possess interconnects with criteria of low loss, high conductivity, and high signal transmission rate. The optical components should be precisely aligned to obtain maximum coupling efficiency across the interfaces. Conventional approaches, such as wire bonding and lead frame assembly, require large footprint of device because of the long wires and housing lids, which introduce extra cost. Wafer bonding is an improved technology that meets requirements of downscaling, increasing integration density and lowering fabrication cost [61].
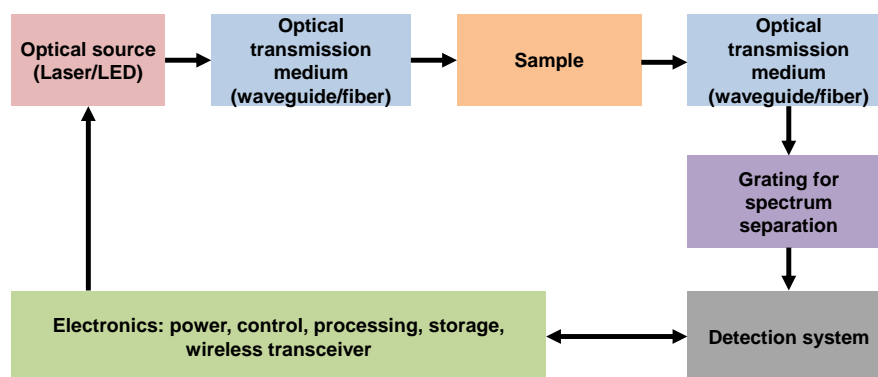
Figure 4. Schematic of an optical sensing microsystem using a Si-based platform. The sample could be a fluidic system with biological species, a chamber with gas, or a solution with target molecules.

Creating electrical interfaces by wafer bonding usually incorporates the mechanical interconnection of conductive materials (bumps) on two wafers. The dimensions of such interconnections are minimized to reduce the capacitance and leakage current at the interface. Specifically, stud bump bonding is a high-speed, modified wire bonding process that is compatible with wafer-level processing and can be used for electrical interconnection. Different stud bumping processes are available. Gold stud bumping has been reported with a bump pitch less than 50 μm when wires with 15–33 μm diameters are used [37]. An example of Au microstud bumps have been used to connect Si substrates with photonics materials such as LiNbO$_3$ is shown in Figure 5 [26]. One example of Cu TSV bonded with Au stud bump is also shown in Figure 5 [62]. Also, Cu stud bumping has been demonstrated on Al metallization in CMOS technologies [63]. Cu is preferred over Au stud bumping because of the slower growth of Cu-Al intermetallic phases and the lower cost of the material [64]. However, when implementing Cu as the

bumping material, the oxidation of Cu surfaces and the requirement for large bonding forces should be taken into consideration.
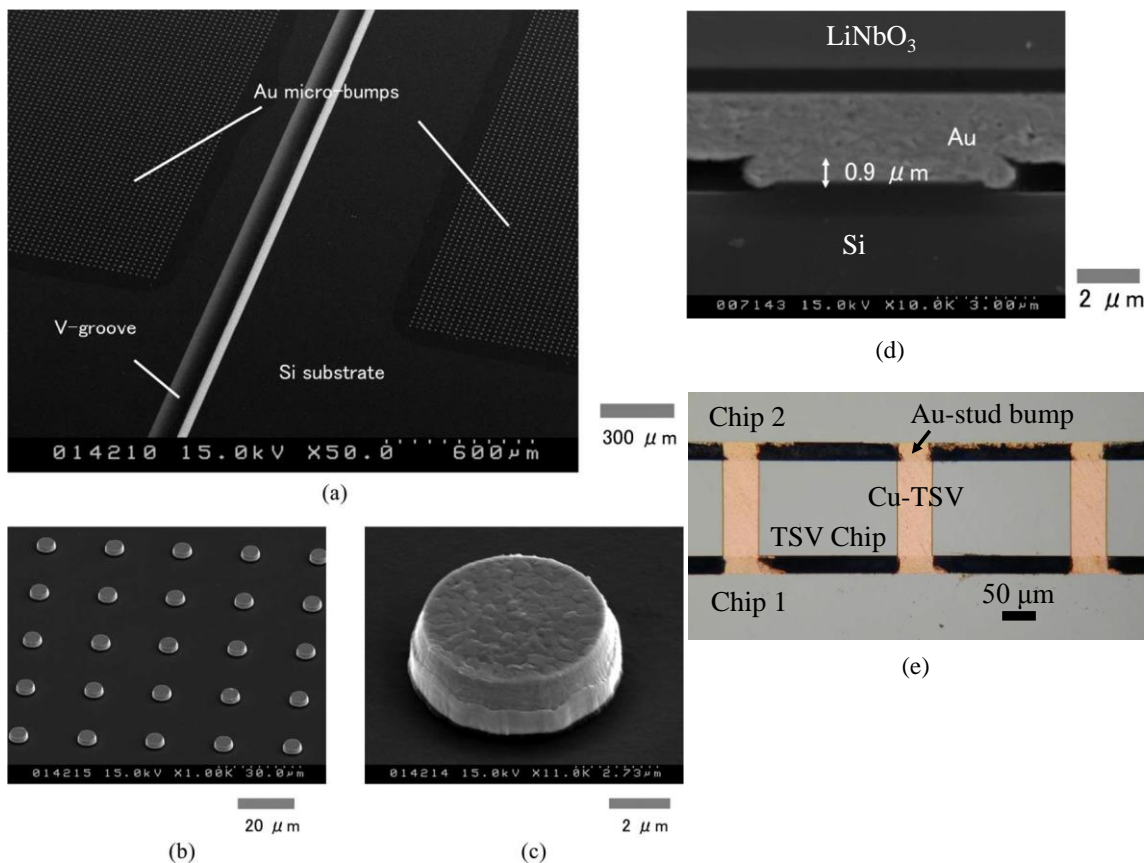

Figure 5. (**a**) SEM image of a Si substrate with a V-groove and Au micro-bumps; (**b**) SEM image of Au micro-bumps; (**c**) Magnification of (b); (**d**) Cross-sectional SEM image of an Au micro-bump on a Si substrate after bonding with a LiNbO$_3$ substrate [26] (Reproduced with permission from Takigawa *et al.*, *IEEE J. Sel. Top. Quantum Electron.*; published by IEEE, 2011); (**e**) Optical image of cross-sectional view of vertically integrated system between Au-stud bumps and Cu-TSVs [62] (Reproduced with permission from Howlader *et al.*, *J. Vac. Sci. Technol. A*; published by AIP, 2011).

In terms of optical interfaces, one study has shown that hermetic sealing is necessary for high performance optical detection systems [65]. For example, infrared detectors such as microbolometers must be packaged inside vacuum cavities (normally with a getter inside the cavity for the level of low pressure needed for microbolometers). The minimization of thermal conduction through controlling residual gases in the well-controlled package environment reduces the loss of thermoelectricity of the detectors. Here, this wafer level vacuum assembly is carried out by bonding of wafers with cavities to house the detectors in the hermetically sealed vacuum [66]. Thus, wafer bonding provides the system with a low-loss optical interface between the system and external environment.

In addition to the housing technique, wafer bonding can also be used for the fabrication of optical devices with high-quality interfaces between optical sources/detectors and waveguides. Current Si photonic technologies combine the efficient light emission benefit of III-V materials (such as InP) with the low losses and high index contrast waveguiding benefit of Si [67,68]. An approach has been

developed to combine these advantages. In one attempt, III-V materials are directly deposited on Si substrate. However, this approach failed due to the lattice mismatch between the deposited materials and the underlying Si substrate. This mismatch was because of the large differences between the deposition temperature and the temperature for using the devices [69,70]. An alternative approach using wafer bonding was developed to address this integration problem by directly bond two wafers at low temperatures [63,71]. The low-temperature direct wafer bonding technologies allow for reducing the lattice mismatch and results in high-quality integration with void-free bonded interfaces. For example, a III-V wafer is bonded to a Si-on-insulator (SOI) wafer with optical waveguides (Figure 6). The III-V quantum wells in the bonded wafer provide optical gain by electrical injection of electrons and holes across a pn junction. The small index difference between Si and III-V materials provides a degree of freedom in manipulating modal confinement in Si and III-V, which is realized by adjusting the III-V layer thickness and SOI waveguide dimension. To decrease the cost in this process, a die-to-wafer bonding process was employed [64]. Also, an InP microdisk laser was bonded to a Si wafer with waveguide by hydrophilic wafer bonding at room temperature [40]. By post-annealing at 200 °C, a good optical interface between the InP laser and Si waveguide was realized.
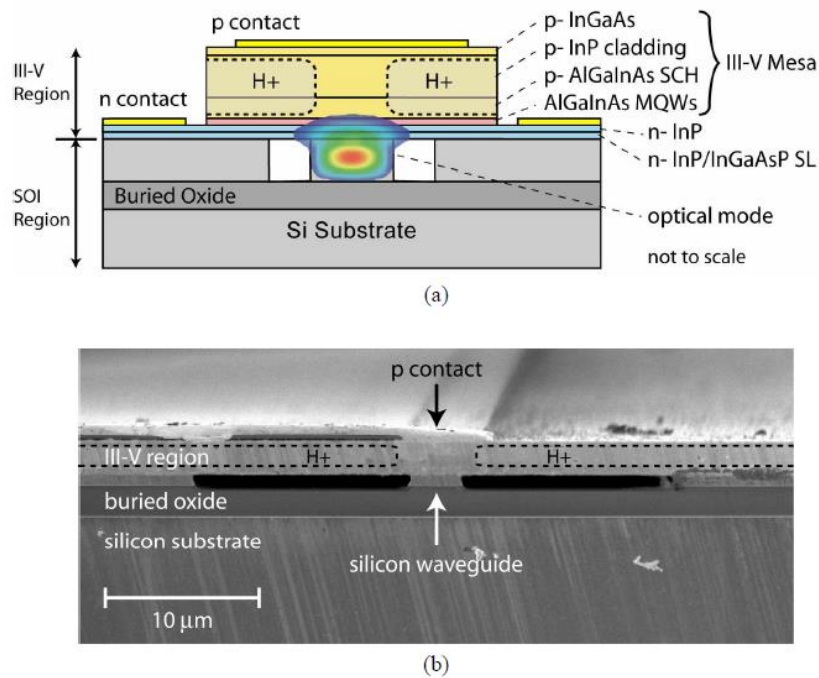
Figure 6. (**a**) Cross-sectional schematic of hybrid Si evanescent platform; (**b**) SEM image of hybrid Si evanescent platform [72] (Reproduced with permission from Fang *et al.*, *Opt. Express*; published by OSA, 2006).

In addition to III-V compounds, single crystalline Ge is also an important material in high sensitivity and high-speed optical detectors at wavelengths up to 1.6 μm. Low-temperature wafer bonding has been observed to create junctions between Ge and Si for the detectors [73]. This method provides less dislocation defects and better crystal quality than in the epitaxially grown Ge which has a lattice mismatch as large as 4.2%. The junction resistance of the two bonded Ge wafers was similar to their bulk resistance, showing a high-performance bonding interface in terms of electrical conduction [56].

Moreover, Ge optical detectors with Si waveguides have been fabricated using Si-Ge wafer bonding. The resulting dark current density was 4 nA/μm^2 and the quantum efficiency was over 90% [73].

Lastly, another advantage of wafer bonding is that different types of components (electronics, optical units, packages) can be developed, processed, and optimized separately before bonding [44]. Many bonding technologies used in the fabrication and assembly of Si-based micro-optical systems use high temperature, high pressure, vacuum bonding chamber, and thick adhesives [74]. These technologies may degrade the materials on the substrates (e.g., polymer), increase process and assembly costs, require complicated equipment (e.g., ultra-high vacuum bonder for vacuum seal), and sometimes be incompatible with biological specimens. Thus, high-performance, reliable, CMOS compatible and cost-effective wafer bonding technologies using reduced external agents (such as heat, force, and adhesive) have to be developed for emerging sensing applications in health and environmental monitoring. A detailed review regarding these approaches is given in the next section.

3. Low-Temperature Wafer Bonding Technologies

In the previous section, wafer bonding was described as an important technology to fabricate and assemble Si-based micro-optical systems. In order to obtain high performance electrical and optical interfaces, low-temperature wafer bonding is recommended. Thermal treatment at low temperatures minimizes the CTE difference induced alignment offset and stress between materials, thus increasing the optical coupling efficiency and the reliability of the interconnections [61].

The fabrication of Si-based micro-optical systems requires high-quality bonded interfaces. The criteria include but are not limited to [16]:

(1) High bond strength, which ensures the mechanical stability and reliability of the assembled optoelectronic components, and offers stability in the optical alignment.

(2) High electrical and thermal conductivity to reduce the energy loss in the electronic components and the high thermal conductivity enables efficient thermal management of the working device.

(3) High hermeticity of the seal to provide the desired working environment for certain devices (such as infrared detectors), thus improving the performance of the system.

(4) High alignment accuracy, which is essential in optical devices for a high optical coupling efficiency.

(5) Excellent optical transparency to reduce the reflection of incident light.

To achieve the aforementioned requirements of the bonded interfaces for the optical detection systems, low-temperature (below 450 ℃, which is CMOS compatible [75]) wafer bonding processes are needed. They are divided into two categories:

(1) Direct bonding, for example anodic bonding, SAB, hydrophilic bonding, and plasma assisted wafer bonding; and

(2) Indirect bonding with intermediate layers, such as adhesive bonding, solder bonding, and SAB with nanoadhesion layers.

In this section, different types of low-temperature wafer bonding are discussed, with emphasizing on the SAB technologies. Their advantages will be highlighted and their disadvantages will be described.

3.1. Direct Bonding without Intermediate Layers

In optical systems, high transparency of optical interfaces is important to maximize optical coupling efficiency. Therefore, intermediate materials should be minimized at the interface of the coupled structures to avoid attenuation of optical signals and variation of refractive indexes. To address this issue, low-temperature direct wafer bonding technologies were developed.
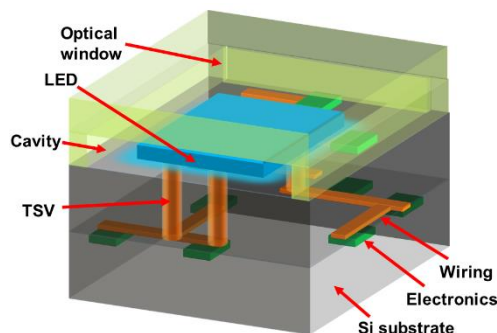
3.1.1. Anodic Bonding

In anodic bonding method, a silicon wafer is bonded with an alkaline (such as sodium) rich glass substrate under the application of 200 V to ~1000 V in the typical temperature ranges of 200 °C to 400 °C [76,77], as shown in Figure 7a. However, the strict requirements may change considerably the volume of glass, causing bowing or warping of the bonded wafer pair. Such mechanical deformation is problematic for optical coupling [78]. Moreover, oxygen anions are generated during anodic bonding at the Si/glass interface. They may oxidize the electrical interconnect metals, resulting in high resistance.
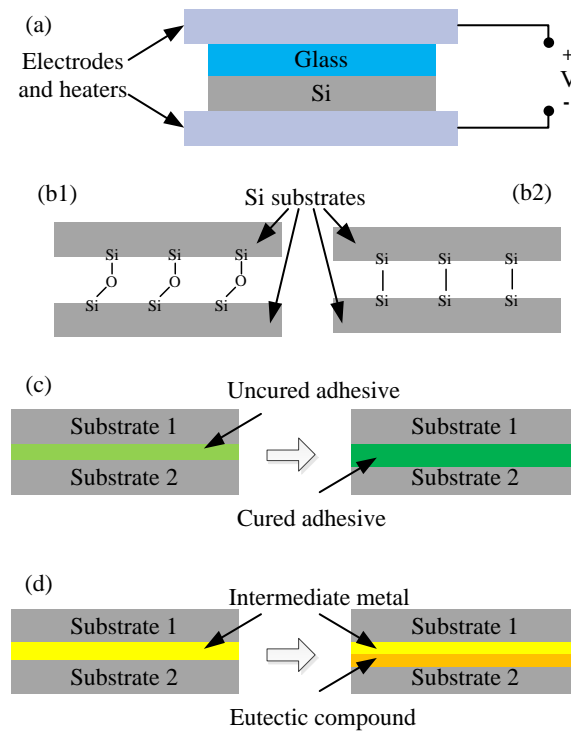
Figure 7. Schematic of: (**a**) Anodic bonding technique to bond glass and Si substrates; (**b**) Hydrophilic and hydrophobic bonding; (**c**) Adhesive bonding; (**d**) Eutectic bonding. Components being used in the substrates for practical applications are not shown in the figure.

In the integration of micro light-emitting diodes (LEDs) or optical detectors, anodic bonding was used to form hermetic optical caps [79] (Figure 8). First, cavities were etched in a Si substrate, followed by mounting optical components such as detectors or LEDs inside the cavities. Then, anodic bonding between the Si substrate and a borosilicate glass substrate was carried out at a maximum electrical field of 20 V/μm and a temperature of 390 °C for 10 min. The fabricated optical windows were smaller than 0.75 mm × 0.75 mm with a yield higher than 95%. Except for the wide applications in fabricating optical

caps [80], anodic bonding was also used for building a vacuum tight vapor cell for optogalvanic spectroscopies [81], microlens arrays [82], 3D microlens scanners [83,84], microfluidic-based optical detection systems [85], micro-optical magnetometers [86], and micro-optical choppers for Raman spectroscopies [87].


Figure 8. Schematic of a 3D-integrated light-emitting diode (LED) with anodically bonded optical window.

3.1.2. Hydrophilic and Hydrophobic Bonding

Anodic bonding requires an alkaline rich glass wafer in the bonding pair. Also, it needs the application of high voltage during bonding. Therefore, hydrophilic and hydrophobic bonding technologies were introduced to bond two pieces of Si wafers. The hydrophobic bonding is resulted from the reactions between chemical terminations on the substrates. For Si substrates, terminations of Si-F and Si-H are formed during surface treatment such as dipping in hydrofluoric acid [88]. Upon post-bonding heating, covalent Si-Si bonds can be formed. On the other hand, hydrophilic (SiO_2-SiO_2) bonding can be attributed to the presence of hydroxyl groups in the form of silanol bonds (Si-OH) on the surface [89]. When two hydrophilic surfaces are contacting, the surfaces adhere to each other by hydrogen bonds. If the attached pairs are annealed at higher temperatures, the initial silanol bond will convert to a siloxane network to form a strong bond between the two surfaces (Figure 7b1). Figure 9 shows the hydrophilic bonding process for InP and SOI wafers [67]. When two hydrophobic surfaces are contacting, the surfaces adhere to each other by van der Waals force. The small amount of surface hydroxyl groups assists the Si-Si covalent bond formation after annealing (Figure 7b2) [90]. To increase the amount of hydroxyl groups, additional plasma treatment is necessary [61]. The requirement of ultra-smooth and clean surfaces is one of the disadvantages in the hydrophilic and hydrophobic bonding technologies. Another drawback is the high temperatures needed in the annealing steps. High temperatures may also affect optical coupling between devices by introducing mechanical deformation of the bonded pairs. In hydrophobic bonding, the bonding temperature could be reduced by introducing nano-scale traps for hydrogen atoms on Si surfaces [91]. Such traps could be formed by implanting arsenic ions to the surfaces of Si substrates, treating the Si substrates using diborane or Ar plasma, or sputtering ~1.5 μm amorphous Si layer onto the substrates. These treatments could reduce the bonding temperature from 700 ℃ to below 450 ℃.

As a coupler between on-chip Si waveguides and external optical fibers, grating structures were integrated on a Si substrate using hydrophilic wafer bonding [92]. First, a Si optical mirror was fabricated

above the encapsulation layer of the grating coupler due to process convenience. Then the surface of the grating coupler was treated by O_2 plasma, flipped and bonded to an optical chip with waveguides. Thus, the mirror was formed beneath the grating, which enhanced the coupling efficiency up to 69%. Some other applications of hydrophilic wafer bonding include the integration of Si photonics and plasmonic waveguides to improve the coupling efficiency [93], the integration of photoluminescence devices on SOI substrates [94], the encapsulation of fused silica optical gratings [95], and the fabrication of heterojunction photodiodes [96].
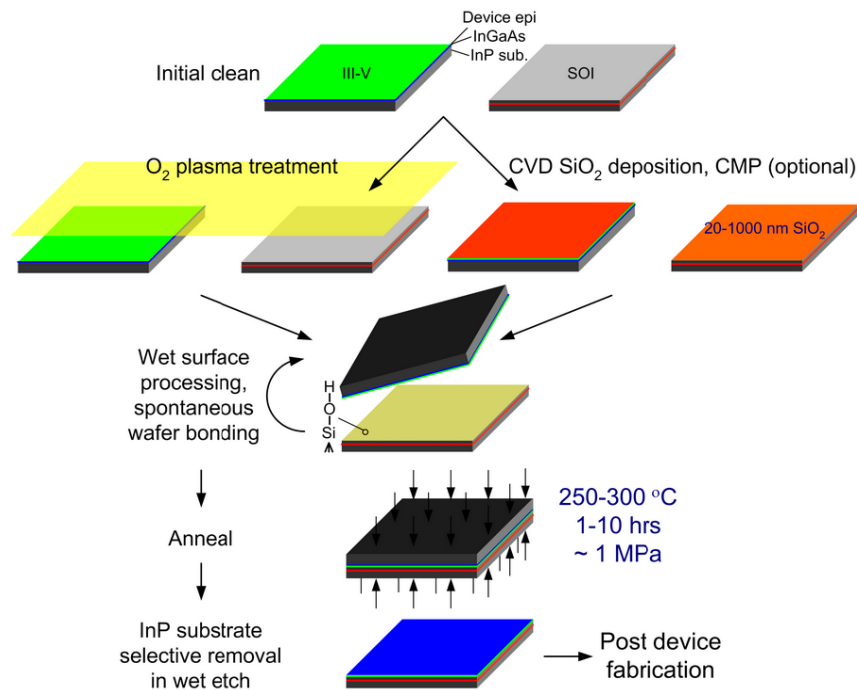

Figure 9. Schematic process flow for hydrophilic bonding of an Si-on-insulator (SOI) wafer and an InP wafer [67].

3.1.3. Surface Activated Bonding

High temperature during or after bonding processes may cause damage at the bonded interface of the optoelectronic components, which was discussed in Section 2.2. One possible solution to address this temperature related issue is to employ the SAB technologies [54,74,97]. The SAB technologies join two clean, smooth and activated surfaces using the adhesion force of surface atoms at room temperature or at low temperatures. The SAB technologies can be categorized into four approaches [14,16], three of which do not need intermediate layers and one approach requires nanoscaled adhesion layer. The three direct bonding approaches will be discussed in this subsection and the fourth one with a nanoadhesion layer is discussed in the next subsection.

For the first direct bonding approach (Figure 10a), the surfaces of bonding pairs are cleaned with an argon (Ar) fast atom beam (FAB), which removes contaminants such as carbon and oxides. Direct adhesion occurs when the surfaces are contacted in an ultra-high vacuum (UHV) at room temperature. High bond strength can be achieved because of the covalent bonding between the atoms of the cleaned and smooth surfaces of the bonded pair [22].
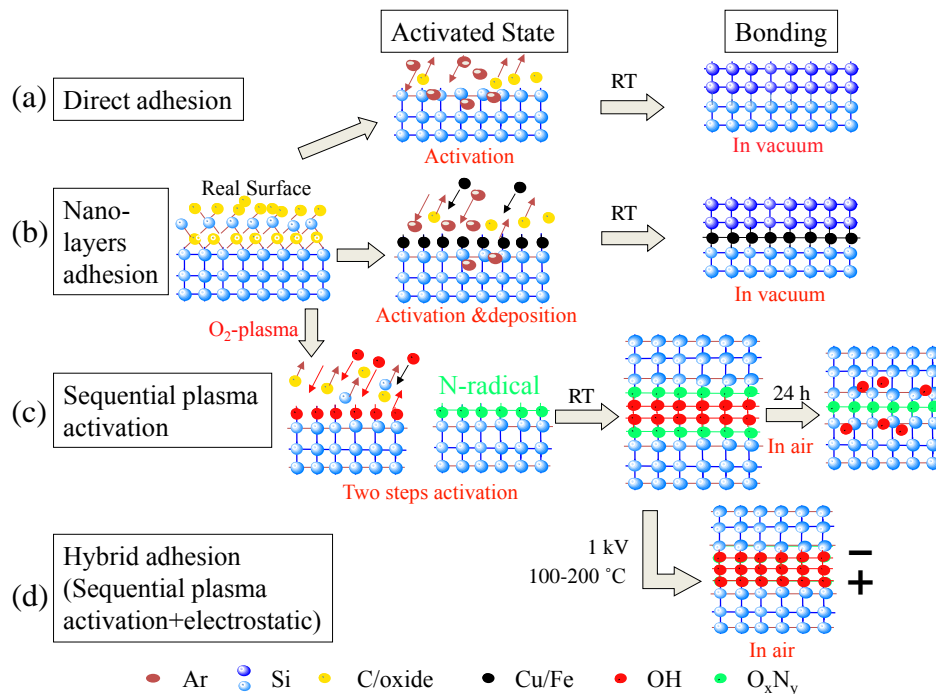
Figure 10. Schematic for surface activated bonding (SAB) technologies that provide atomic-level bonding through: (**a**) Direct adhesion; (**b**) Nano-layers adhesion; (**c**) Sequential plasma activation; (**d**) Hybrid adhesion [16] (Reproduced with permission from Howlader *et al.*, *IEEE J. Sel. Top. Quantum Electron.*; published by IEEE, 2011).

For vertical electrical interconnections, the direct adhesion approach has been demonstrated through bonding of 60 nm height Cu bumps, resulting in high interfacial conductivity [98]. This approach has also been used to bond Cu-filled through-Si vias and Au stud bumps [99]. Using the first SAB approach, material combinations such as Si-InP [20], Si-GaAs [21], Si-GaP, and GaP-GaAs [100] with high bond strength and smooth material interfaces, suitable for optical applications have been reported. There is also demand to bond dissimilar crystalline materials directly for optical isolation in optical systems. A typical example is the bonding of $CeY_2Fe_5O_{12}$ (Ce:YIG) and $LiNbO_3$ [101]. The SAB technique eliminates the difficulties in conventional bonding techniques such as voids formed across the bonded interface [102]. High bond strength has been achieved and the optical isolation performance could be optimized by tuning the Ar FAB irradiation time. In addition, $LiNbO_3$ has been bonded on Ce:YIG after surface activation by Ar and O_2 mixed plasma, and Ce:YIG has been bonded onto a Si rib waveguide by O_2 plasma activation [103].

In the second direct bonding approach of SAB (Figure 10c), the surfaces are cleaned using radio frequency (RF) RIE and microwave-neutral radicals in low vacuum. Then, the bonding is carried out in a cleanroom atmosphere rather than in UHV. The sequential plasma activation provides highly hydrophilic and reactive surfaces. It also generates nanopores and oxides on surfaces that remove and absorb water from the interface to the bulk material, resulting in strong covalent bonding [13–23,27,28,99,100,102,104–107].

Semiconducting material pairs such as Si-Si, Si-Ge, and SiO_2-Ge has been bonded using this method. The bonding strength of SAB processed Si-Si pair can be 30 times higher than using hydrophilic bonding [17,25]. To achieve a strong and reliable bond between Ge and Si/SiO_2, heat treatment should

be applied after bonding to minimize the hydroxyl groups at the bonded interface [27]. The absorbed water in the bulk of materials across the interface in the sequential plasma activated bonding process results in interfacial voids.

The third direct bonding approach of SAB, named hybrid plasma bonding (Figure 10d), addresses the issue of interfacial voids: the bonded wafers in the second approach are post-treated with an anodic bonding method in a cleanroom atmosphere. This treatment resulted in a void-free bonded interface with high bond strength. The high bond strength is attributed to the adhesion between the hydrophilic and reactive surfaces and the electrostatic forces produced by the anodic step in the bonding process [13–23,27,28,99,100,102,104–107].

For Si and glass wafers [15], the hybrid plasma bonding provides much stronger adhesion than pure anodic bonding due to the highly hydrophilic, reactive, and smooth surfaces of Si and glass after plasma activation. Also, the temperature requirement of hybrid plasma bonding is lower than anodic bonding. The hybrid plasma bonding has also been demonstrated with other combinations of wafers such Ge, GaAs, SiO_2 and glass [105,108]. The results demonstrate the combined effect of physico-chemically activated surfaces with electrostatic forces to bond ionic materials and Si/glass in the controlled atmosphere of the clean room. The void free and strong heterogeneously integrated interfaces of silicon with other wafers at low temperature can be used in fluidic systems for detecting optical signals from biological species.

3.1.4. Other Direct Bonding Technologies

Cu-Cu has been bonded at room temperature by direct hydrophilic bonding for electrical interfaces [109–111]. Chemical mechanical polishing is conducted to provide the surface of Cu with low roughness and good hydrophilicity. Also, plasma-assisted bonding effectively cleans the substrate by removing contaminants and introducing a surface disorder layer. For example, a plasma treated Si substrate possesses a large amount of Si-OH groups, which offer the possibility to increase the bonding strength to over 1.6 J/m^2 through the polymerization of such groups [112,113]. The resulted resistivity at the interconnection was as low as 22.5 mΩ·μm^2.

3.2. Indirect Bonding with Intermediate Layers

Although direct wafer bonding in SAB is promising, there are limitations for bonding of certain ionic materials, such as $LiNbO_3$ and $LiTaO_3$ [13,19]. These ionic materials polarize inhomogeneously after surface treatment, which results in repulsive force between the ionic wafers. So the indirect bonding methods are introduced to address this issue.

3.2.1. Adhesive Bonding

In adhesive bonding, often a polymer adhesive is applied between the two wafers to be bonded. Pressure is required to drive the surfaces into intimate contact. Then, the adhesive is cured by either thermal treatment or ultraviolet (UV) light [114], as illustrated before in Figure 7c. The bonding temperature is dependent on the type of adhesive used and can vary from room temperature (for UV cured adhesives) to 100 ℃. One of the commonly used adhesive in photonic integration is

divinylsiloxane-bis-benzocyclobutene (DVS-BCB), because it has a low curing temperature, high degree of planarization, high optical transmissivity, good thermal stability, excellent chemical stability, and low moisture absorption [115]. The process flow of BCB adhesive bonding is shown in Figure 11. The problems of using an adhesive for wafer bonding are now heighted.

A hermetic seal cannot be created due to the gas permeability of the polymer materials.

The CTEs of adhesives are normally quite different from Si or other semiconductors so that the mechanical reliability cannot be guaranteed.

High conductivity bonding interfaces are challenging to realize (even when using conductive adhesives).

Continuity of optical properties of bonded interfaces is disrupted by adding foreign materials with different optical features (such as different refractive indexes).
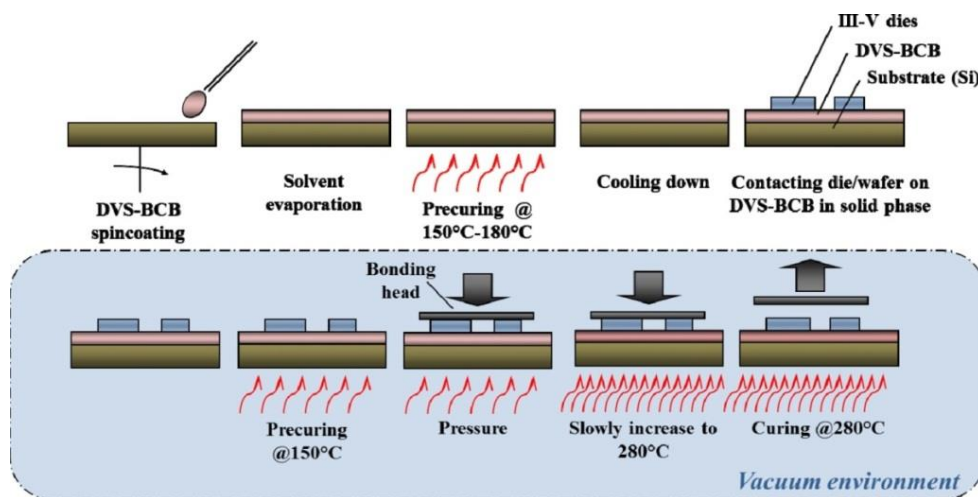
Figure 11. Silicon photonics integration process flow using bis-benzocyclobutene (BCB) bonding [115] (Reproduced with permission from Keyvaninia *et al.*, *Opt. Mater. Express*; published by OSA, 2013).

Since adhesive bonding uses inexpensive polymeric adhesives, it is a cost-effective process and has been implemented in several industrial applications. For instance, miniaturized cameras for cell phones and laptops were fabricated using wafer-level adhesive bonding [116]. Specifically, the adhesive bonding utilized UV-curable epoxies to integrate micro lenses. The bonding process was fast because the epoxy can be cured within 10 s at room temperature. The integrated cameras had a stable optical transmission over 80% for visible light after reliability tests, which was attributed the low outgassing and low shrinkage of the epoxy adhesive. Further, adhesive bonding was used in the fabrication of MEMS micromirror arrays [117], uncooled infrared detectors [117], III-V laser chips with Si waveguides [118,119], integrated photonics chips [120], integrated optical spectrometers and detectors [121,122], and optical circulators [123].

3.2.2. Eutectic Bonding

Eutectic bonding can partially address the low transparency and hermeticity issues of the bonded interfaces in the adhesive bonding by replacing the thick (several hundreds of nanometers to several micrometers) and gas/moisture permeable polymer adhesives. In this method, an intermediate metal

layer is used, which can finally change into a eutectic system with the substrate, as shown in Figure 7d. In industry, Au-Si [124] and Al-Ge [125] intermediate layers are mostly used for bonding semiconductor wafers. Sometimes, an Sn-based system is employed for MEMS assembly [126]. Eutectic bonding uses intermediate metal layer that can produce a eutectic system. The eutectic bond is formed by melting a preform (the melting point of the preform is lower than that of its base materials) consisting of a mixture or alloy of two or more dissimilar metals at the bonding interface. However, this approach requires a metal layer between two wafers that may block the optical pathway in assembly of optical devices. Also, an elevated temperature is needed to accelerate the diffusion of the metal.

Eutectic bonding was used to form electrical interconnects in micro-optical systems. For example, in the integrated avalanche photodiode-based detector arrays and cameras [127], In bumps were deposited on the anode contact of each active region. The eutectic bonding between In and Au (on readout circuits) connected the photodiode array to an appropriate readout integrated circuit. The choice of In-Au eutectic system here was due to the low stress in the In bumps at low temperatures (-25 °C to -20 °C), at which the detectors were operated. Also, eutectic bonding was implemented in packaging of GaN LED chips on Si substrates to enhance thermal dissipation [128], in vertical LEDs [129,130], in the development of high-power laser chips [131], as well as in the packaging of thermal imaging sensors [132] and micromirror arrays [133].

3.2.3. Surface Activated Bonding with Nanoadhesion Layers

Since both adhesive bonding and eutectic bonding reduce the transparency of bonded interfaces, the thickness of the intermediate layer should be minimized. The fourth SAB approach using nanometer-thick adhesion layers to bond specific materials such as ionic materials and polymers is now explained (Figure 10b). Bonding of ionic materials is challenging because of their inhomogeneous polarization due to surface activation. In this indirect SAB approach, surface cleaning and deposition of a nanoadhesion layer (for example, a few nanometers of iron (Fe)) are simultaneously performed. The layer controls the surface polarization and enhances the adhesion between the contacting surfaces [13,19]. The two substrates contact with each other spontaneously in low vacuum or UHV and a high bond strength is achieved.

The single crystalline ionic wafers, such as $LiNbO_3$ and $LiTaO_3$, are materials of interest for the fabrication of optoelectronic devices, such as modulators [134]. The ionic materials are required to be integrated with Si substrates. But these materials polarize inhomogeneously after surface activation, which results in repulsive force between the wafers. In order to depolarize the surface, ultrathin (nanometer thickness) Fe films were deposited on the ionic wafers and the activation was prolonged [13,19]. The Fe adhesion layer increases the bonding strength at the bonded interface (8 MPa without Fe nanolayer and 37.5 MPa with it). In addition, the nanometer-thick layer could maintain the optical transparency of the interface, which is very important for optical applications.

To summarize the low-temperature wafer bonding technologies using the SAB technologies, the following are the importance compared with conventional bonding and integration methods.

(1) The ability to bond varieties of solid-state materials with high bond strength.

(2) The applied pressure and process temperature can be lowered. The chemically induced degradation and defect at the bonding interface can be reduced.

(3) The low temperatures used in the process result in high alignment accuracy between bonding pairs.

(4) The realization of mechanical, electrical, and optical connections on the same bonded substrates with minimized optical disruption.

These advantages benefit Si-based micro-optical systems by: (1) incorporating of various types of materials including Si, glass, III-IV materials, ionic materials and polymers; (2) reducing the mismatch of electrical and optical performance at the bonded interface; (3) maximizing the optical coupling efficiency; and (4) enabling small footprint of the fabricated device through wafer-level bonding. However, the long processing time of SAB remains an important disadvantage.

4. Future Assembly of Optical Systems

In the future, aspects in new materials, assembly concepts, and fabrication techniques should be considered in developing micro-optical systems. First, new materials with unique properties, such as high quantum efficiency, will be integrated with Si to enhance the systems performance such as the increase in signal-to-noise ratio. Second, new integration and assembly concepts will be used to increase the density and reliability of systems. Finally, the cost for development and fabrication of the Si-based systems must be reduced.

4.1. New Materials

Carbon materials have attracted great attention in recent years because of their outstanding mechanical, electrical, thermal, and optical properties. Graphene has properties of strong electron-electron interaction [135] and high photocarrier multiplication [30]. Thus, graphene based photodetectors exhibit ultrafast response. In addition, graphene integrated with micro-/nano-cavities [136,137] or plasmon resonators [138] enhances the detectors' optical absorption and responsivity. Furthermore, hybrid graphene-quantum dot architectures can greatly improve the responsivity of the optical detector. On the other hand, all carbon-based photodetectors have also been demonstrated by integrating zero dimensional graphite quantum dots and 2D graphene sheets [139]. The graphite quantum dots possess high absorptivity, and the graphene sheet has high electrical conductivity. These material properties resulted in a photocurrent responsivity up to 4×10^7 A/W for the all carbon-based photodetector.

CNT, the one dimensional nanomaterial, was found to be sensitive to near infrared (IR) radiation [29]. A CNT based IR detector coated with a pin-hole-free parylene C thin film has been demonstrated with a long lifespan. Also, CNTs has been used as the flip-chip bumps [140,141], and as a filler for TSVs [142].

For the integration of carbon nanomaterials, the CMOS compatible process may be used. There are two possible approaches. In the first approach, low-temperature chemical vapor deposition can be used to directly grow CNTs on Si chips, where electrical and optical components are fabricated. In the second approach, CNTs can be grown on a substrate using high-temperature methods, and then transferred to the target substrate at low temperatures. In terms of electrical contact between carbon nanomaterials and CMOS circuits, CMOS compatible metal (Al) is being studied to replace the materials, such as Au, that are currently used [30].

Another potential new material is MoS_2. A heterojunction photodetector fabricated by combining MoS_2 and amorphous Si (a-Si) has been demonstrated with short response time of ~0.3 ms (Figure 12) [31]. The light is incident from a-Si side, optical absorption occurs in a-Si, and photo-generated electrons

diffuse to the underlying MoS$_2$ layer and are transferred across the MoS$_2$ layer toward a metal contact. The transient response of this material combination did not show persistent photoconductivity. Thus the device was about 10 times faster than amorphous Si-based ones while its photoresponsivity was 2 to 4 times larger. Such device can also be integrated with MoS$_2$ transistor based readout circuits, leading to a monolithic technology. Further, WS$_2$ monolayers are two-dimensional crystals of one atom thickness having direct bandgaps in visible spectrum. At room temperature, the edges of WS$_2$ monolayers with a zigzag termination exhibit surprisingly strong photoluminescence [32]. This new nanoscaled material could be applied as flexible, transparent, and low-energy optical sources and detectors.
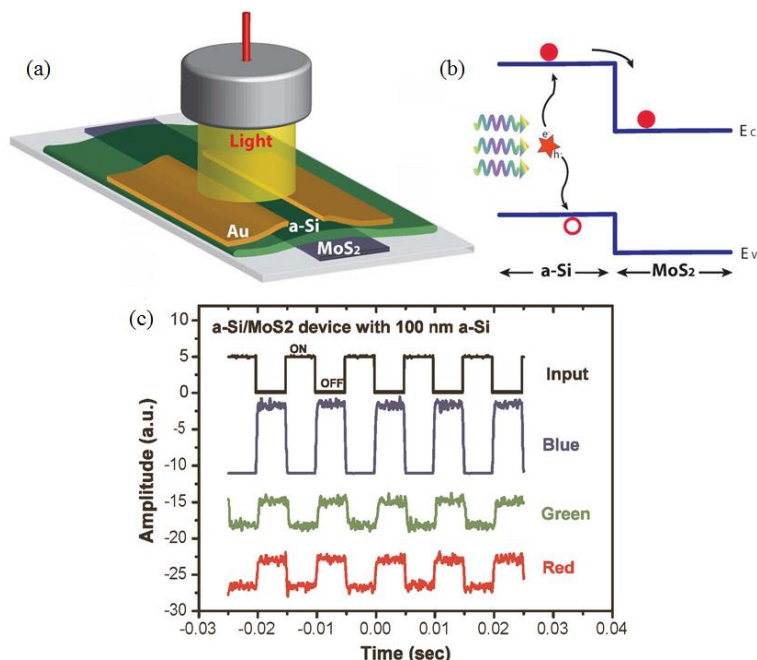
Figure 12. (**a**) Schematic of a-Si/MoS$_2$ heterojunction photodetector; (**b**) Energy band diagram of a-Si/MoS$_2$ heterojunction photodetector; (**c**) Transient responses of the device for three incident wavelengths [31] (Reproduced with permission from Esmaeili-Rad *et al.*, *Sci. Rep.*; published by NPG, 2013).

In addition to the abovementioned inorganic materials such as Ge, Si, MoS$_2$, and WS$_2$, high performance organic semiconductors with rare earth materials can be used to enhance the responsivity of UV photodetectors [33]. For example, the electron acceptor of tris-(8-hydroxyquinoline) gadolinium and the donor of 1,3,5-tris(3-methylphenyl-phenylamino) triphenyamine (m-MTDATA) has been used in UV detectors.

4.2. Advanced Assembly Concepts

Besides the materials aspect, new assembly concepts are required to improve the performance and reduce the size of Si-based micro-optical systems. Such systems containing optical and electronic devices can be assembled using monolithic or hybrid techniques. In monolithically or hybrid integrated systems, the optical coupling loss can be reduced, the data transmitting rate can be increased (to terabits per second speed) and the power efficiency can be improved (to a few milliwatts per gigabit data [143]).

These advantages are attributed to the densely integrated optical and electronic components in a single package [38,144].

4.2.1. Monolithic Integration

Optical components can be monolithically integrated with Si-based CMOS readout circuits. Because all the functional layers in the device are fabricated sequentially on the same substrate, the interconnections between optical and electrical components are fairly short. Thus, high-quality interfaces are easier to realize. Also, the monolithic fabrication of optoelectronic devices is based on current CMOS technology or processing, which reduces the equipment investment.

Ge-on-Si photodetector is an example of a monolithically integrated component (Figure 13) [145]. Here, Si behaves as the waveguide that is interfaced to a Ge optical detector. Such device utilizes the benefits from both Si and Ge: Si's large bandwidth and CMOS compatibility as well as Ge's high responsivity to longer wavelengths than Si. Therefore, the integrated Ge detectors and Si waveguides can provide the detection system with high responsivity and wide bandwidth. This technology requires high-quality epitaxial Ge films grown on Si. One important indication of high-quality Ge on Si is a low threading dislocation density. Several extra steps can be carried out in addition to existing CMOS processes to improve the quality of deposited Ge film on Si. In one approach, a SiGe buffer layer is deposited on the poly-Si gate to reduce the threading dislocation density in the Ge layer which is deposited later. In another approach, a Ge growth plus annealing method was reported [146]. Such process deposited Ge film more uniformly on Si without the formation of localized Ge islands, which significantly reduces the threading dislocation density.
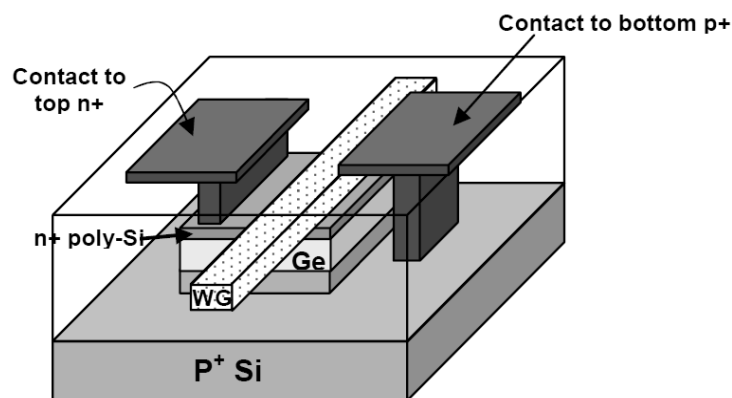
Figure 13. Schematic structure of a waveguide-integrated Ge p-i-n photodetector [145] (Reproduced with permission from Ahn *et al.*, *Opt. Express*; published by OSA, 2007).

Advanced CMOS imagers are three-transistor-based pixel structure which includes Si-based photodectors. They are monolithically integrated by using the existing CMOS processing steps. The electrical interconnection in such a system is small in dimensions and allows the fast conversion of the photogenerated charges to voltages, with signal amplification in the pixels [147,148].

While the standard CMOS processes can be used to fabricate nanometer scale structures and devices, integration of CMOS devices with other optical components on the same chip remains challenging. One of the challenges is the high processing temperature of the optical materials. So the temperature sensitive

materials are difficult to be monolithically integrated. Further, MEMS technology consists of many bulk-processing steps such as deep RIE, cavity wet etching, and electroplating. These steps are not compatible with the CMOS technologies. Thus, the process compatibility is the bottleneck in the monolithic integration of MEMS and CMOS components.
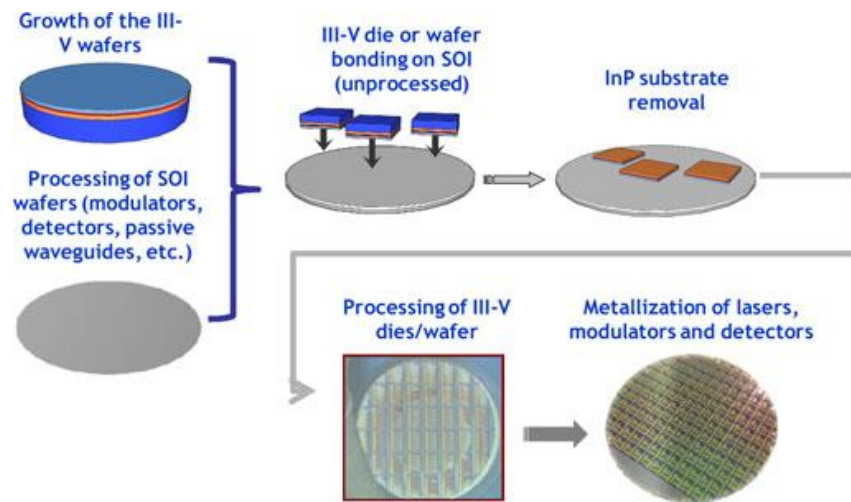
4.2.2. Hybrid Integration

Compared to the monolithic integration, hybrid integration of the optical layers with a completed CMOS chip is more convenient as different components can be processed separately and the process compatibility becomes less critical. The fabrication of optical components is independent of the CMOS processes [40,149]. Therefore, the consumption of optical materials could be reduced, resulting in cost reduction.

Optical detectors can effectively be integrated with electronic circuits by embedding the detector in a polymeric waveguide with high coupling efficiency up to ~95% [51,52]. One way to embed waveguide interconnects using polymers is to utilize thin-film optical detectors and bond them to the substrate with electronic components. The polymer waveguide is then fabricated on the top of the bonded substrates and the optical detectors are embedded beneath the waveguide. The advantage of this method is that the waveguide and the embedded optical detector can be integrated onto the substrate with electronic components by post-processing. Hence, the processing steps of the existing electronic boards/chips will not be affected when implementing the optical structures. Finally, the chip tests can be done separately to improve the yield.

To increase the integration density, the optical chip and the Si CMOS chip have to be integrated and assembled in the same module. Using hybrid integration, the yield and performance of the two categories of the components can be independently optimized before integration [72,150]. To realize this hybrid integration, wafer bonding can be used. The wafer bonding processes such as hydrophilic/hydrophobic bonding, adhesive bonding, and SAB are capable of bonding tiny structures made from different materials, resulting in high electrical conductivity and alignment accuracy. Hybrid integration using bonding can make use of the benefits of different materials, such as the optical gain of III-V materials for efficient optical emission [67], the high optical absorption efficiency of Ge for detection [145], and the low loss and high index contrast of Si for lightwave guidance [72,150].

Hybrid-integrated InP/SOI lasers and transmitters based on wafer bonding were reported [151]. Passive rib waveguides, strip waveguides, Bragg reflectors and vertical output couplers were fabricated on the SOI wafer (Figure 14). At the same time, the p-InGaAs contact layer, p-InP cladding layer, InGaAsP quantum wells and InGaAsP separate confinement heterostructure layers were produced on the InP wafer. Afterwards, surface preparation such as polishing was done on the two preprocessed wafers. Hydrophilic bonding was used to join the substrates in a wafer-to-wafer or a chip-to-wafer fashion. Adhesive bonding using BCB polymer was examined as well. Although this approach did not require complicated surface preparation, the yield of devices was 18% lower than using hydrophilic bonding.

Figure 14. Process flow of hybrid integration of III-V materials on Si [151] (Reproduced with permission from Duan *et al.*, *IEEE J. Sel. Top. Quantum Electron.*; published by IEEE, 2014).

Hybrid integration of thin film devices offers the possibility to fabricate systems with many structures and components. For instance, an integrated lab-on-a-chip system has been demonstrated. This system contained a Si signal processing unit, III-V semiconductor-based optical detection unit, and polymer-based microfluidic unit [152]. The GaAs optical detectors were fabricated on individual substrates and transferred to Si substrates by chip-to-chip bonding. Polymeric materials were used to encapsulate the optical detectors. On top of the polymer encapsulation, the microfluidic components were constructed by soft lithography. The fabrication of individual components used the conventional microelectronic batch processes.

In another example of hybrid integration, cavities were fabricated in the substrates with fabricated photonic devices. The small CMOS chips are placed and bonded inside those cavities to reduce the total size of the products. The photonic substrates with integrated CMOS chips are then bonded to a cap wafer to complete the assembly. The processing simplicity, flexibility, and the ability to integrate wide range of components (microfluidics, optics, electronics, MEMS *etc.*) in hybrid integration make the monolithic integration unappealing [72,150].

Hybrid integration requires technologies such as wafer thinning, vertical interconnection, bumping, molding, dicing and component assembly, and encapsulation. All these technologies need to be optimized and adapted into a modular integrated process flow [153]. Disadvantages of hybrid assembly concept include complex electrical interconnections between the CMOS electronics and optical components. Also, the bonding processes for hybrid integration should be further optimized to improve their compatibility with different types of components to be integrated [40,154].

4.3. Cost Reduction Approaches

The cost of the optical detection systems includes the costs of materials, device fabrication and assembly. The cost may further be increased with the use of new materials such as MoS_2 and their non-conventional integration technologies. Since the CMOS technology is relatively mature and productive, low-cost materials with CMOS process compatibility are required to be developed for the

fabrication of optical systems on a Si-based platform in future. For instance, polymers can be used to replace glass for fabricating optical fibers and conductive polymers can replace metals for electrical connections. Polymers may provide robust, continuous and cost-effective chip-to-chip interconnections [155]. Another benefit of polymers is the ease of processing for various devices [156]. A polymer-based hybrid photonic integration platform was developed recently [157]. Such platform mainly used UV-curable epoxy resins and provided flexible optical I/O interfaces coupled with InP active components, film-based optical elements, and on-chip optical fibers. Figure 15 shows a polymer-based optical network unit fabricated on such platform. Another important CMOS-compatible material is SOI. This material platform is used for both optical components (for example, waveguides) and readout electronics. Despite the relatively high cost of SOI wafers, the existing CMOS processing facilities for SOI wafers enable the fabrication to be high-yield and cost-effective [64]. Examples of integrated micro-optical systems have been shown in previous sections.
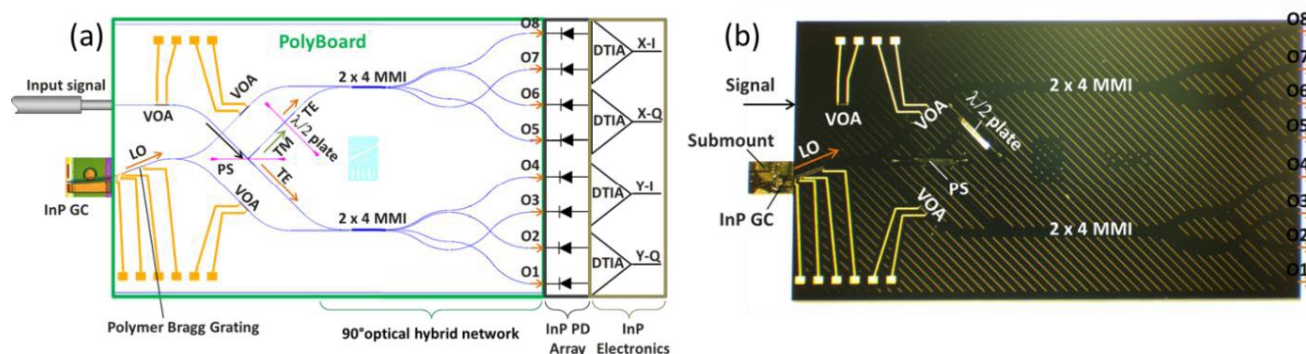
Figure 15. Optical network unit assembled on the polymer-based hybrid integration platform. (**a**) The schematic layout and (**b**) photograph of the assembly [157].

The fabrication and integration cost is the major part of the total product cost [158]. High volume and efficient production may reduce the product cost. Wafer bonding is one of the large volume and high throughput techniques to achieve low fabrication and integration cost. All dies on a wafer are processed in a series of steps, thereby yielding substantial savings in time, materials, and labor [66,159].

To further reduce the cost of labor and equipment, it is necessary to develop highly automated fabrication and assembly equipment for enhancing manufacturing yield [38]. This equipment also requires to be standardized. For example, when using expensive III-V material, a die-to-wafer bonding process is preferred to reduce the material consumption [64]. The die bonding systems, consisting of the automatic passive optical alignment, materials handling and bonding units, are promising. These criteria enable the processing of many photonic dies in a single run for wafer level hybrid integration [160]. It is also expected that one set of equipment can be used to process different types of substrates/products. Finally, considering the CMOS compatibility, utilizing existing CMOS processing facilities for low cost manufacturing is preferred. Also, when developing new integration equipment, its compatibility with current CMOS lines should be considered.

For both CMOS and photonic dies, low-temperature processing technologies are preferred to preserve material properties and device performance. Low-temperature processes also allow the implementation of materials with low glass transition temperatures (for example, polymers), which may lead to cost

reduction [161]. And the time for temperature ramping up and cooling down can be saved to increase the process efficiency.

Finally, the devices should be fabricated using the components with optimized processing steps to meet the application requirements. For instance, the devices should be designed in highly compact form to minimize amount of the optical interconnections and to share common assembly elements such as the heat sink and the substrate [63]. In short distance optical interconnect systems, large diameter fibers could be used to relax the alignment tolerance so that lower the cost of the alignment process [48]. If the products are aimed for low-end market, low cost assembly methods such as liquid encapsulation and transfer molding can be employed.

4.4. Prospected Systems

Recently, a fluorescence spectroscopy based wireless imaging system has been demonstrated using commercially available components for qualitative and quantitative diagnosis of biological cells [162–166]. The system consists of three subsystems: an optical module, an electronic image acquisition module, and an image processing and wireless communication module. The optical module illuminates the biological cells and collects the florescence signal from the cells through optical interfaces between optical components. The image is then acquired by the high-sensitivity image acquisition module, and then sent for further processing via electrical interfaces. The size of the demonstrated system is 2.64 cm × 8.26 cm, as shown in Figure 16. This prototype is too large to fit in gastro-intestinal tract. Therefore miniaturization is required. The miniaturization can be accomplished by shrinking the foot-print of the components, packages and interconnects and by interconnecting them on a single substrate.
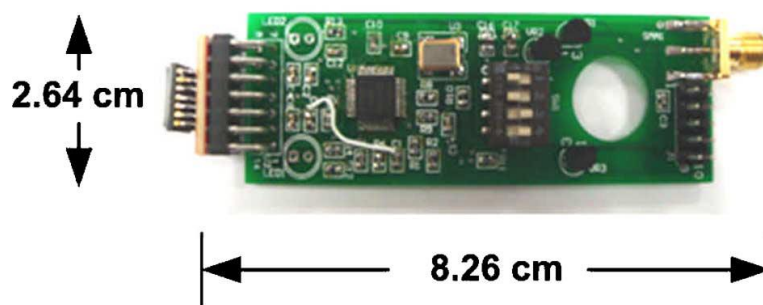
Figure 16. A photograph of the prototype of the imaging acquisition module for diagnosis of biological cells, the imager is on the left mounted perpendicular to the circuit board [162] (Reproduced with permission from Kfouri *et al.*, *IEEE J. Sel. Top. Quantum Electron.*; published by IEEE, 2008.).

Figure 17 shows the schematic diagram of a typical Si-based hybrid integrated wireless health monitoring system with imaging capability of biological cells and proteins. These components guide the light, extract the optical signals, process the signals and transmit the signals wirelessly. The integrated system may provide improved functionality, reliability, performance and reduced cost. Integration and assembly technologies for building up such systems vary a lot depending on their performance requirements, material properties, and application circumstances. Nevertheless, low-temperature wafer bonding is one effective way to realize such system with satisfactory interface qualities.
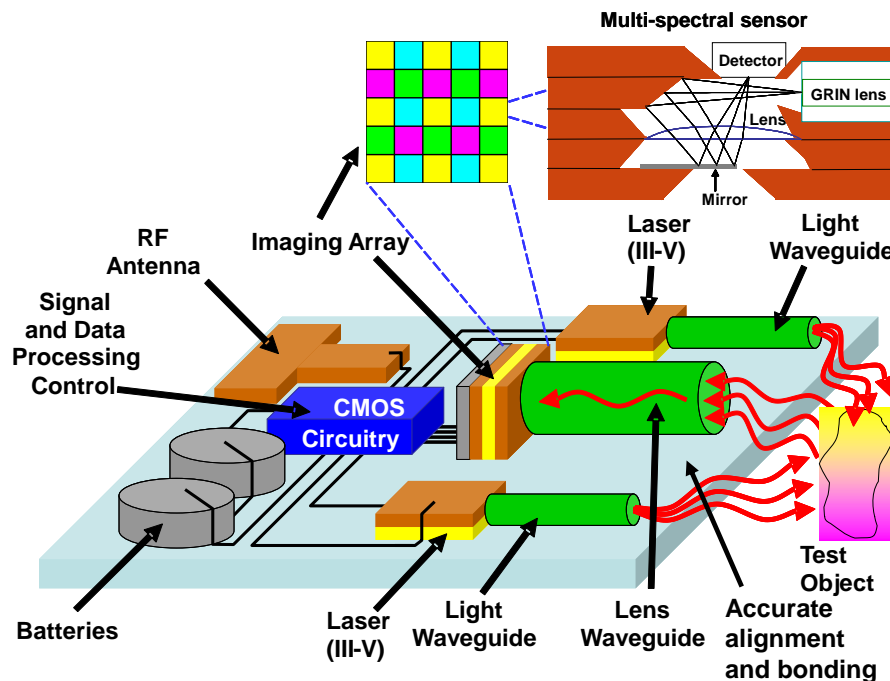
Figure 17. Schematic diagram of an emerging integrated micro-optical system for health monitoring.

5. Conclusions

Si-based micro-optical systems generate, guide, sense, and image optical signals. In order to shrink the sizes and improve the performance of existing systems, components with small footprints have to be densely integrated. The performance of such systems is determined by the quality of interfaces among electrical and optical components. Highly conductive, low-loss electrical interconnections and optical interfaces with high coupling efficiency are two very important factors. Thus, proper integration and assembly technologies are needed. Electrical interconnections fabricated by wafer bonding offer reduced parasitic electrical parameters. Passive optical alignment of different components is an efficient and cost-effective approach to obtain relatively high coupling efficiency. Conventionally, anodic, hydrophilic and hydrophobic, adhesive and eutectic bonding methods have been used for the integration and assembly Si-based microsystems. However, due to the presence of heat-, pressure- and chemical-sensitive components in systems, these methods are less suitable than the surface activated bonding technologies in terms of interface quality and processing simplicity. The SAB technologies are promising for the electrical and optical interfaces because they do not require high temperature and high external pressure. The SAB technologies enable precise alignment of tiny structures as well as electrically low-loss and optically transparent bonded interfaces. For the future improvement of Si-based micro-optical systems, varieties of new materials such as WS_2 and MoS_2 with strong photoluminescence or high photo responsivity may be used. Finally, the cost of such systems which is controlled by the materials, processing technologies, and the manufacturing facilities may be reduced by standardization of wafer level processing equipment compatible with CMOS capabilities.

Acknowledgments

Conflicts of Interest

The authors declare no conflict of interest.

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