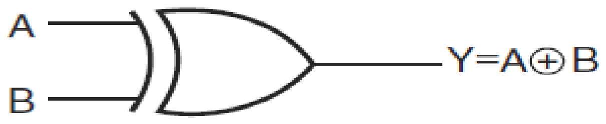
Lecture 22:Arithematic Circuits

Additional Logic Gates, Half Adder, Full Adder, Half Subtractor, Full Subtractor

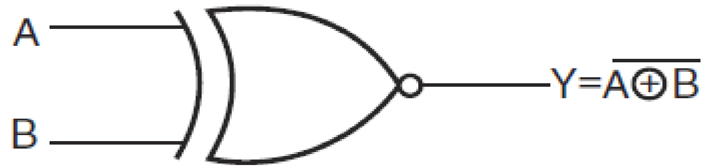
XOR Gate



A	B	Y
0	0	0
0	1	1
1	0	1
1	1	0

output is “1” if only one of the inputs is “1”

XNOR

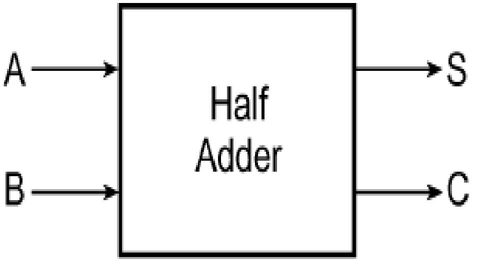


A	B	Y
0	0	1
0	1	0
1	0	0
1	1	1

Output is “1” only if the two inputs are equal

Half Adder

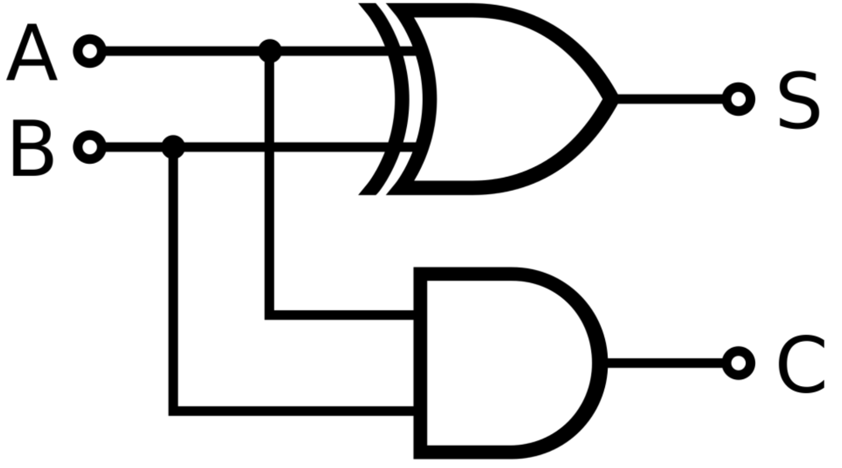
A	B	S	C
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1



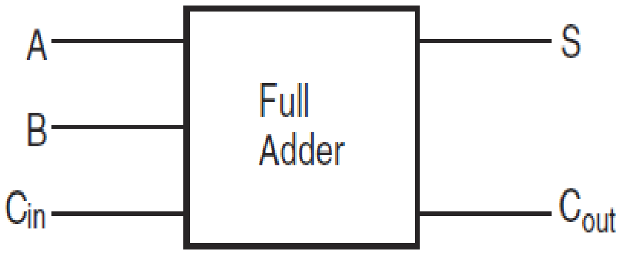
this half adder does not take into account the existence of a carry in

$$S = A\overline{B} + B\overline{A},\ C = AB$$

Half Adder Implementation



Full Adder



A	B	C_{in}	SUM (S)	C_{out}
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

a Kranaugh map is constructed to simplify the implementation of this combinational logic circuit

Kranaugh Maps

AB

C_{in}	00	01	11	10
0	**0**	**1**	**0**	**1**
1	**1**	**0**	**1**	**0**

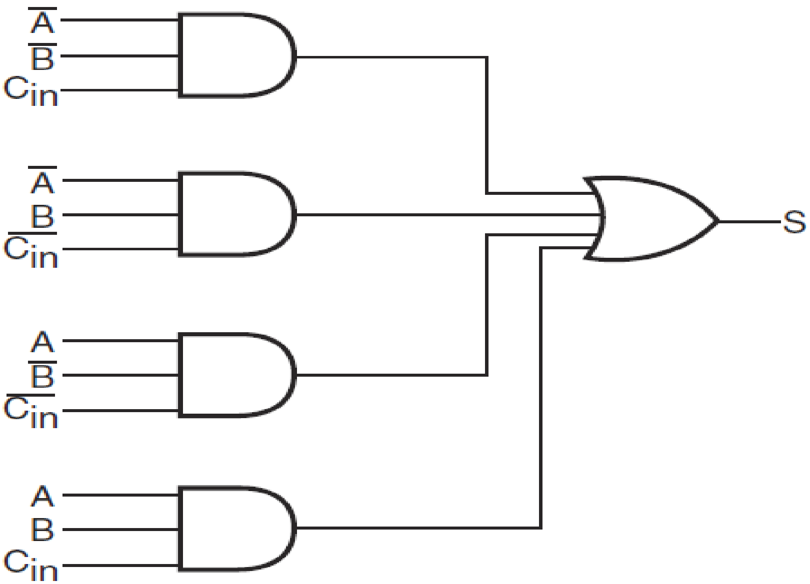
$$S = \bar{A}\bar{B}C_{in} + \bar{A}B\bar{C}_{in} + A\bar{B}\bar{C}_{in} + ABC_{in}$$

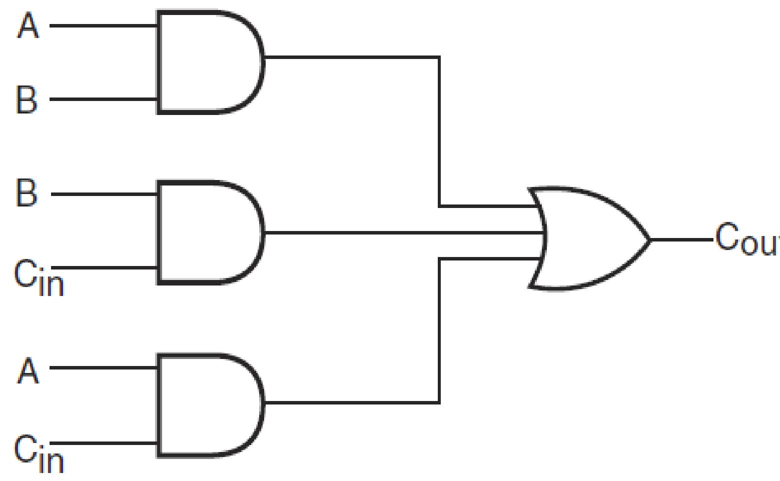
AB

C_{in}	00	01	11	10
0	**0**	**0**	**1**	**0**
1	**0**	**1**	**1**	**1**

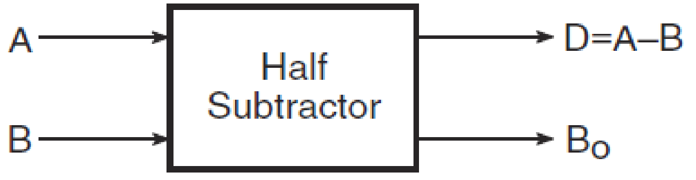
$$C_{out} = AB + BC_{in} + AC_{in}$$

Full Adder Implementation





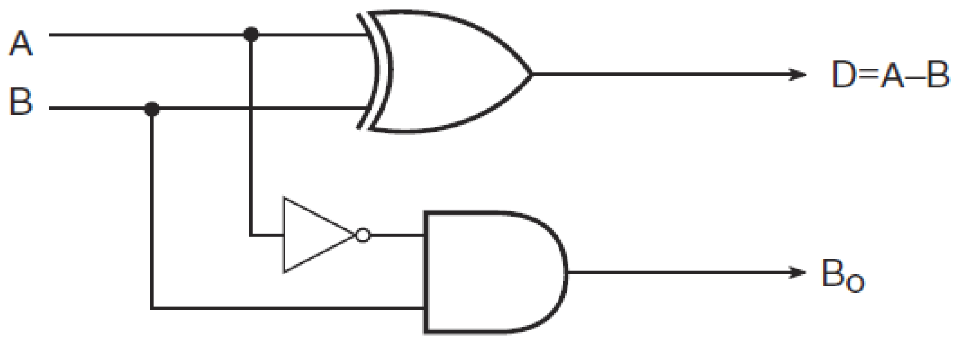
Half Subtractor



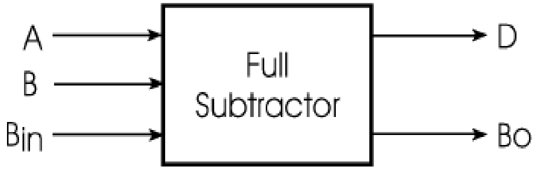
A	B	D	B_o
0	0	0	0
0	1	1	1
1	0	1	0
1	1	0	0

$$D = \bar{A}B + \bar{B}A$$

$$B_o = \bar{A}B$$



Full Subtractor



Minuend (A)	Subtrahend (B)	Borrow In (B_{in})	Difference (D)	Borrow Out (B_o)
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	0	1
1	0	0	1	0
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1

we construct a Kranaugh map for each of the two outputs

Kranaugh Maps

AB

B_{in}	00	01	11	10
0	**0**	**1**	**0**	**1**
1	**1**	**0**	**1**	**0**

Odd parity!

$$D = \bar{A}\bar{B}B_{in} + \bar{A}B\bar{B}_{in} + A\bar{B}\bar{B}_{in} + ABB_{in}$$

AB

B_{in}	00	01	11	10
0	**0**	**1**	**0**	**0**
1	**1**	**1**	**1**	**0**

$$B_o = \bar{A}B + BB_{in} + \bar{A}B_{in}$$

Implementation