Lecture 23: Flip Flops

RS Flip Flop, JK Flip Flop, Toggle Flip-flop

Sequential Logic Circuits

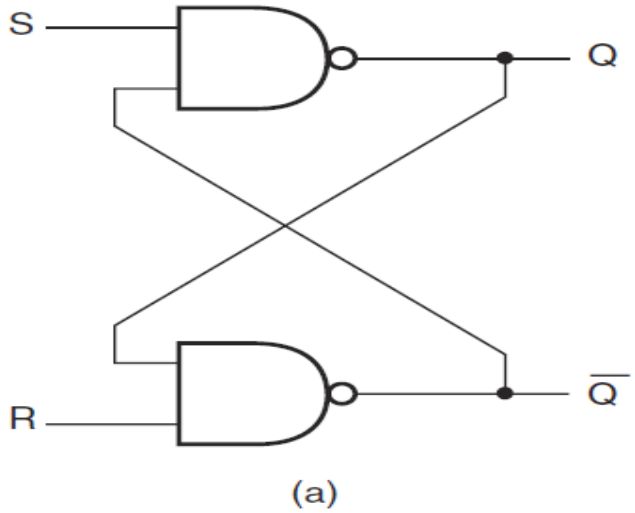
in Combinational logic circuit, the output depends only on the current values of the inputs

in Sequential logic circuits, the output depends on the input and the current state of the output

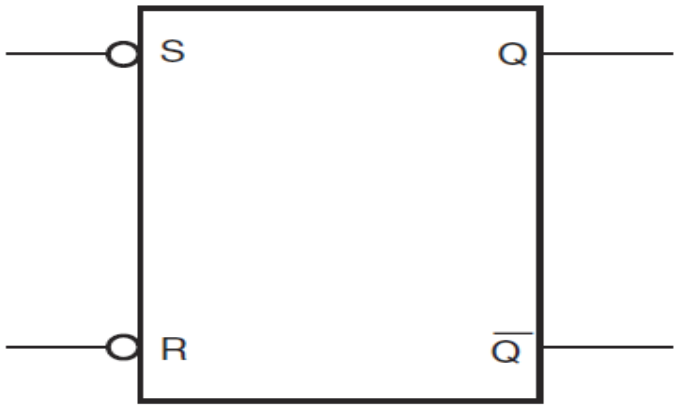
sequential circuits offer a means for creating registers and memory elements

RS Flip-Flop

1. SET=RESET= 1 is the normal resting condition of the flip-flop. Both Q and $\overline{Q}$ remain in the logic state they were in prior to this input condition.
2. SET = 0 and RESET = 1 sets the flip-flop. Q and $\overline{Q}$, respectively, go to the '1' and '0' state.
3. SET =1 and RESET =0 resets or clears the flip-flop. Q and $\overline{Q}$ respectively go to the '0' and '1' state.
4. SET = RESET = 0 is forbidden.



(a)



Truth Table of RS Flip-Flop

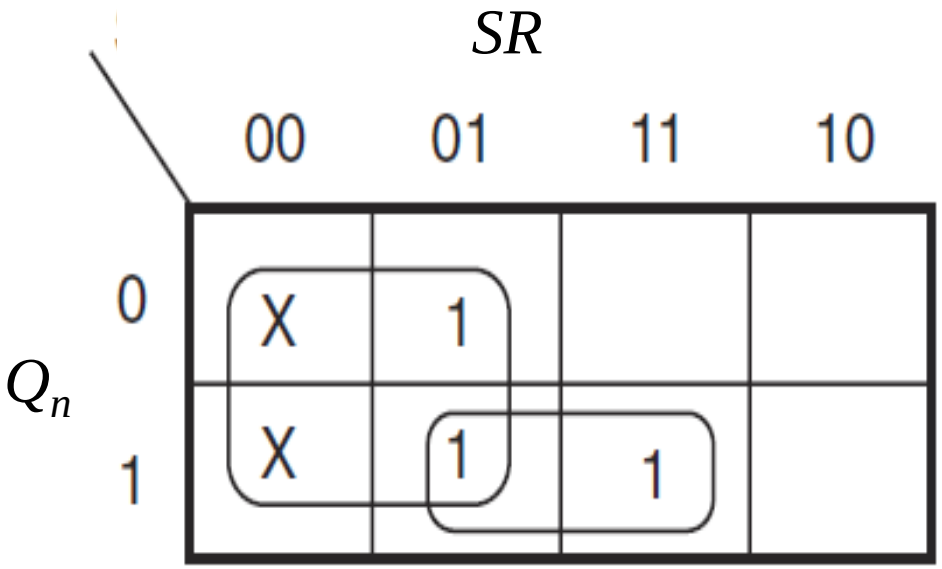
notice that for sequential circuits, the current state is considered as an input!

active low Flip-Flop!

Qn	S	R	Q_{n+1}
0	0	0	Forbidden
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	Forbidden
1	0	1	1
1	1	0	0
1	1	1	1

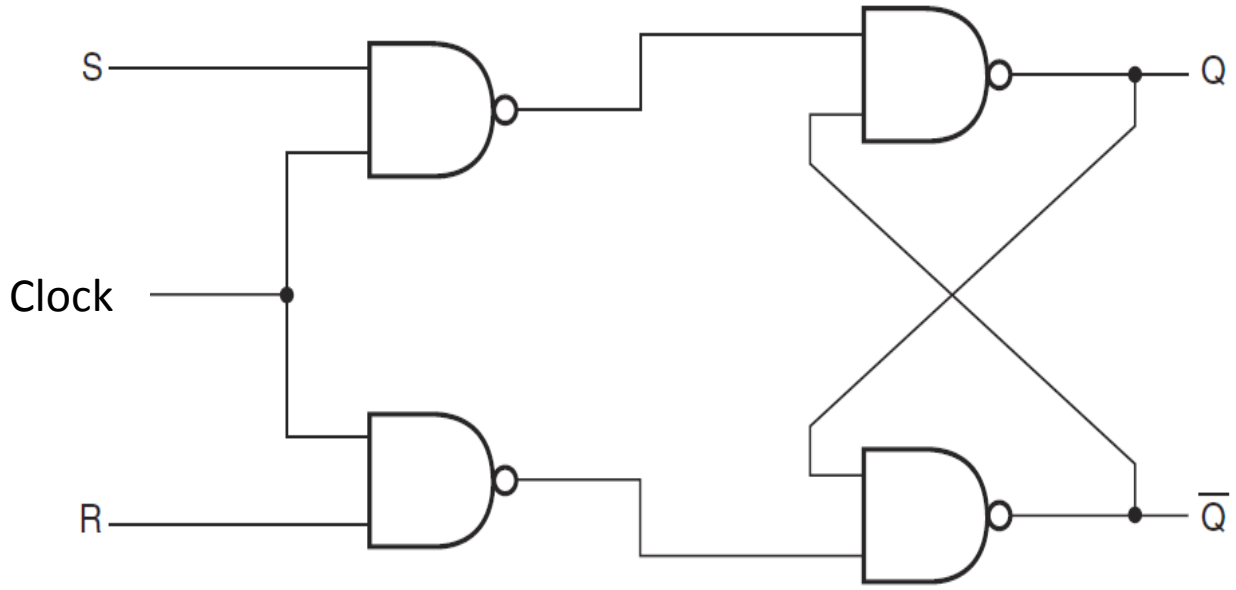
Kranaugh Map

$$Q_{n+1} = \overline{S} + RQ_n$$



notice the use of the do-not-care outputs!

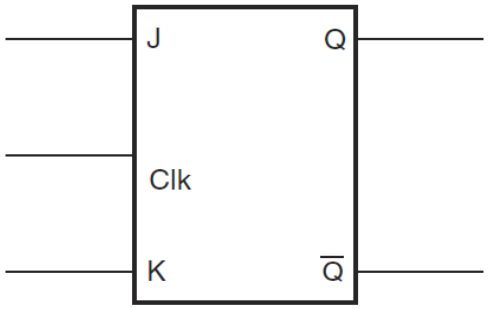
Clocked RS Flip-Flop



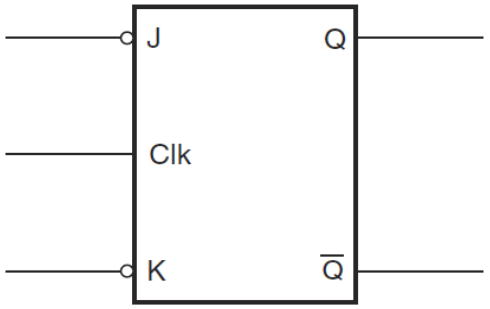
when the Clock is LOW, both inputs are HIGH, indicating no change of state regardless of S and R

when the Clock is HIGH, both the S and R inputs are inverted and transmitted to the input

JK Flip-Flop



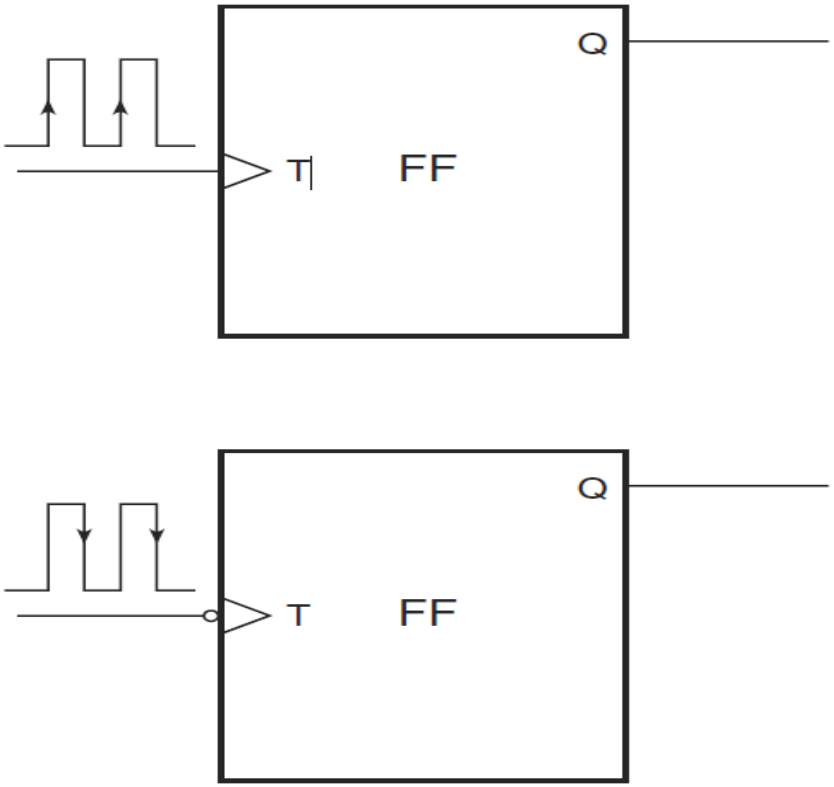
	J	K	Clk	Q_{n+1}
SET	1	0	1	1
RESET	0	1	1	0
NO CHANGE	0	0	1	Q_n
TOGGLE	1	1	1	$\overline{Q}_n$



	J	K	Clk	Q_{n+1}
SET	0	1	1	1
RESET	1	0	1	0
NO CHANGE	1	1	1	Q_n
TOGGLE	0	0	1	$\overline{Q}_n$

the forbidden states for active LOW and active HIGH RS Flip-Flops is replaced by a toggle state where the output changes its value

Toggle Flip-Flop



the output toggles every time there is a rising edge (or falling edge) change at the input of the Flip-Flop