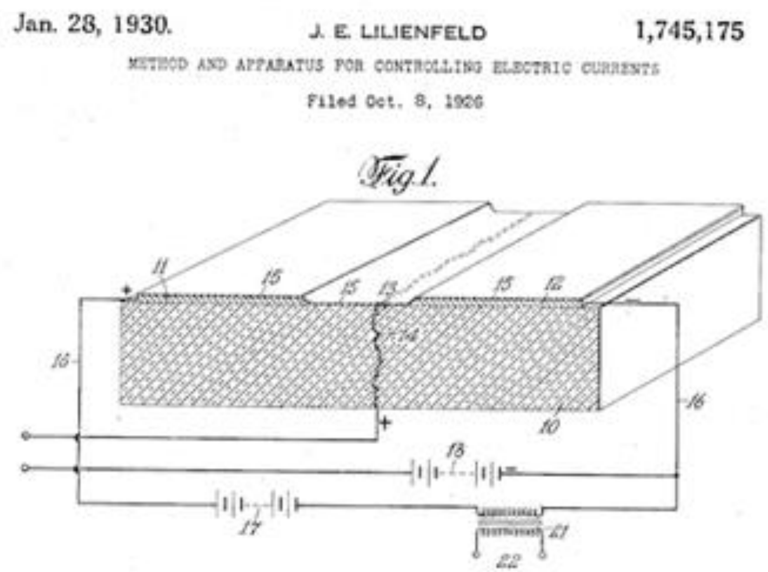
Lecture 15:Field Effect Transistors (FETs) (1)

JFET, Characteristic Curves, Biasing, Examples

FET

The idea for a field-effect transistor (FET) was first proposed by Julius Lilienthal, a physicist and inventor. In 1930 he was granted a U.S. patent for the device.

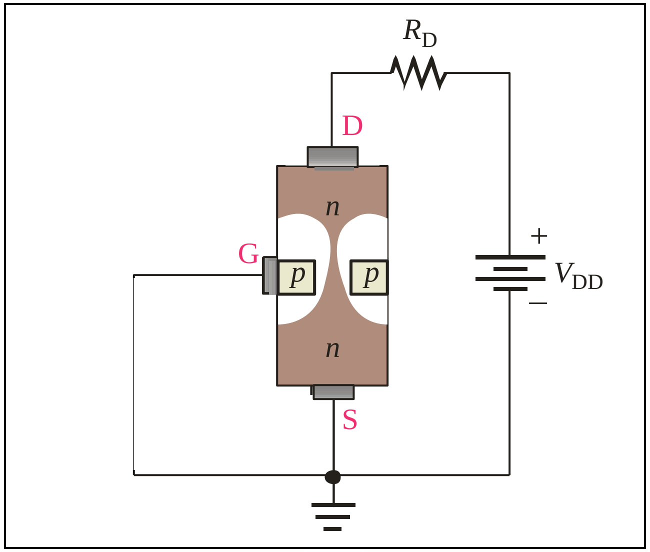
His ideas were later refined and developed into the FET. Materials were not available at the time to build his device. A practical FET was not constructed until the 1950's. Today FETs are the most widely used components in integrated circuits.



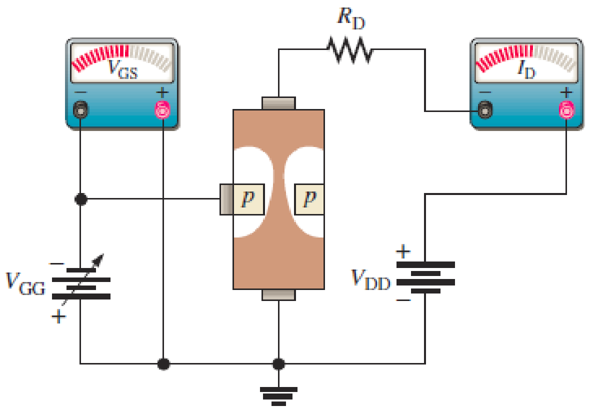
JFET

The JFET (or Junction Field Effect Transistor) is a normally ON device. For the *n*-channel device illustrated, when the drain is positive with respect to the source and there is no gate-source voltage, there is current in the channel.

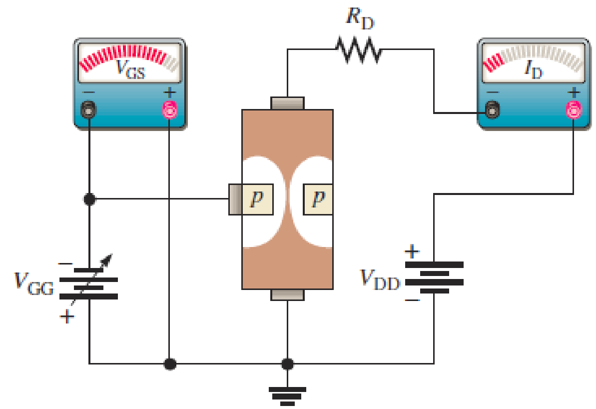
When a negative gate voltage is applied to the FET, the electric field causes the channel to narrow, which in turn causes current to decrease.



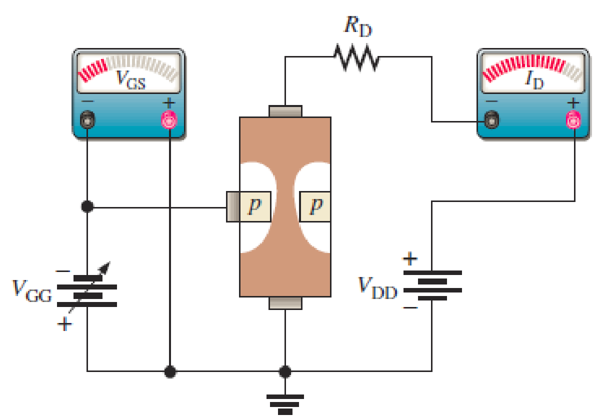
JFET Operation



(a) JFET biased for conduction



(b) Greater V_{GG} narrows the channel (between the white areas) which increases the resistance of the channel and decreases I_D.

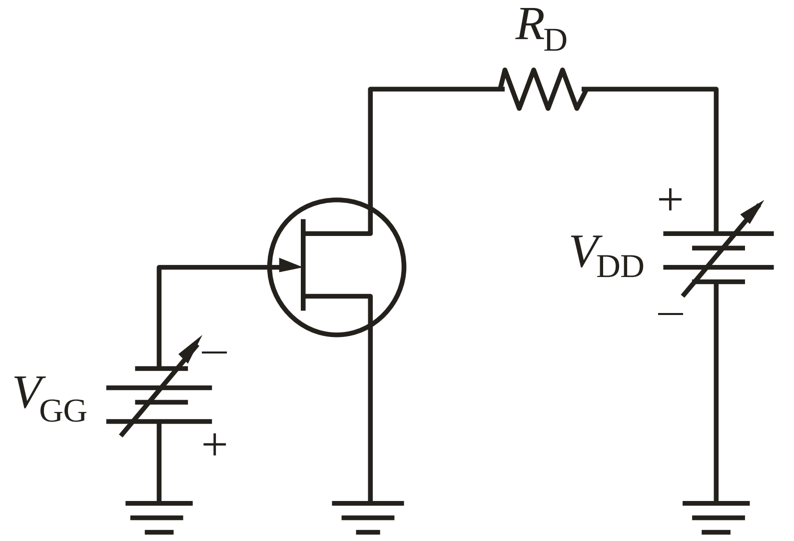


(c) Less V_{GG} widens the channel (between the white areas) which decreases the resistance of the channel and increases I_D.

JFET Circuit Symbol

There are two types of JFETs: *n*-channel and *p*-channel. The dc voltages are opposite polarities for each type.

The symbol for an *n*-channel JFET is shown, along with the proper polarities of the applied dc voltages. For an *n*-channel device, the gate is always operated with a negative (or zero) voltage with respect to the source.



We will focus on n-channel JFET

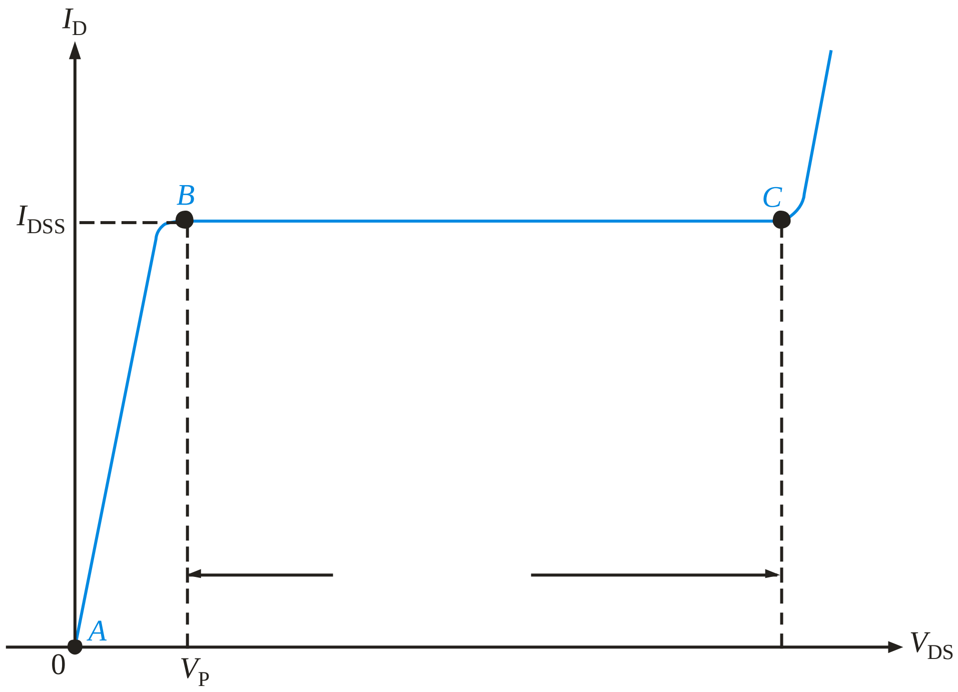
Drain Characteristic Curves

There are three regions as illustrated for the case when $V_{GS} = 0$ V.

Between *A* and *B* is the **Ohmic region**, where current and voltage are related by Ohm's law.

From *B* to *C* is the **active** (or *constant-current*) **region** where current is essentially independent of V_{DS}.

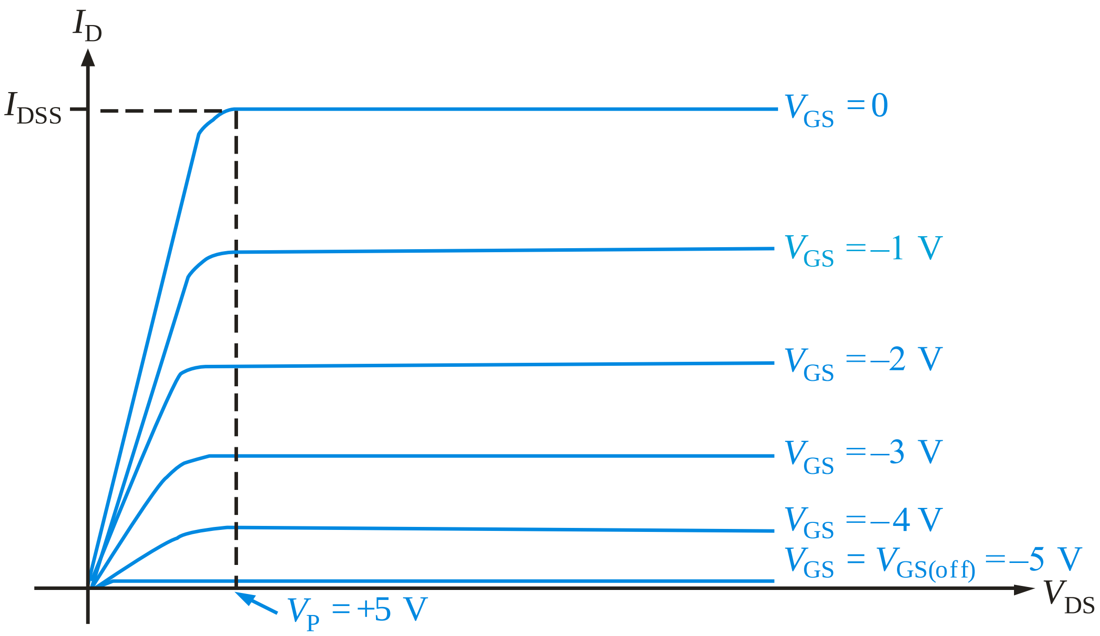
Beyond *C* is the breakdown region. Operation here can damage the FET.



Characteristic Curves (Cont'd)

When V_{GS} is set to different values, the relationship between V_{DS} and I_D develops a family of characteristic curves for the device.

An *n*-channel characteristic is illustrated here. Notice that V_p is positive and has the same magnitude as $V_{GS(off)}$.



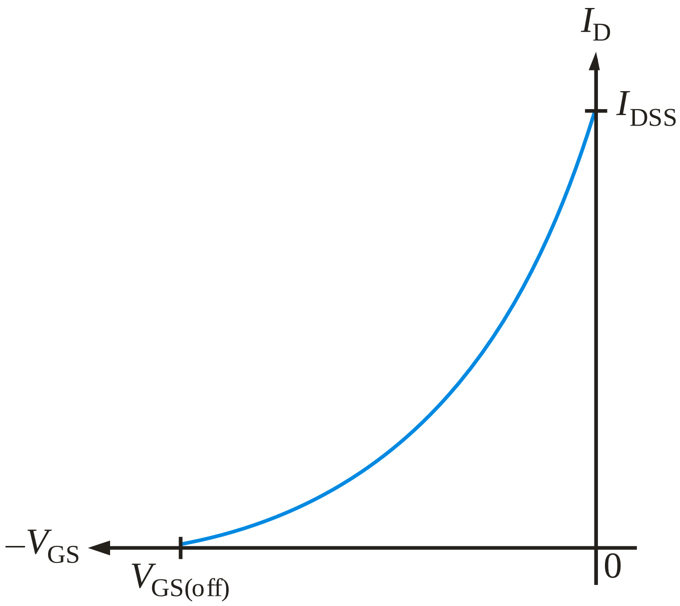
Transconductance Curve

A plot of V_{GS} to I_D is called the transfer or transconductance curve. The transfer curve is a is a plot of the output current (I_D) to the input voltage (V_{GS}).

The transfer curve is based on the equation

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_{GS(off)}}\right)^2$$

By substitution, you can find other points on the curve for plotting the universal curve.



Transconductance

The transconductance is the ratio of a change in output current (ΔI_D) to a change in the input voltage (ΔV_{GS}).

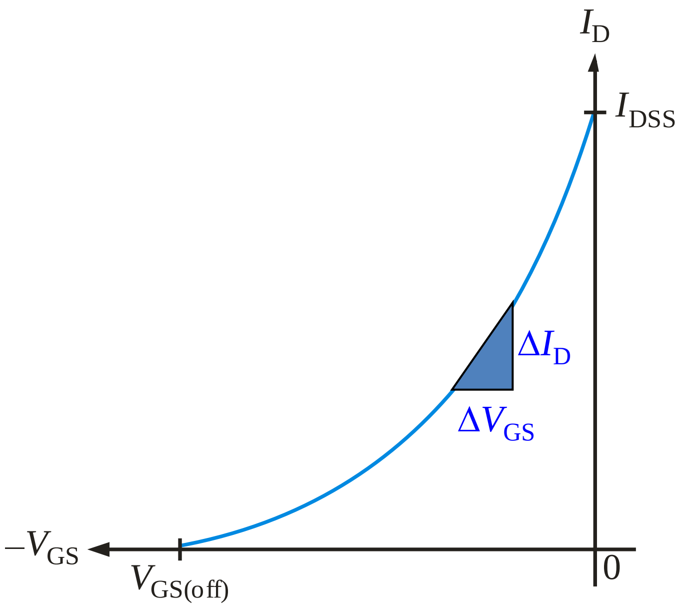
This definition is $g_m = \dfrac{\Delta I_D}{\Delta V_{GS}}$

The following approximate formula is useful for calculating g_m if you know g_{m0}.

$$g_m = g_{m0}\left(1 - \frac{V_{GS}}{V_{GS(off)}}\right)$$

The value of g_{m0} can be found from

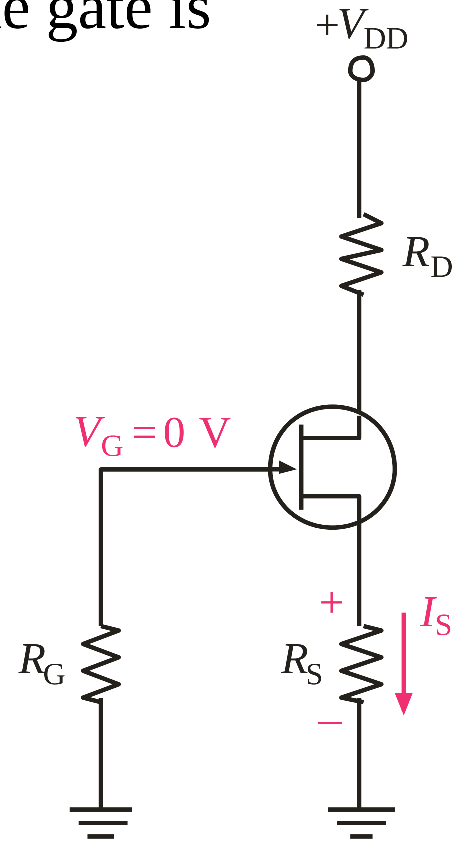
$$g_{m0} = \frac{2I_{DSS}}{\left|V_{GS(off)}\right|}$$



Biasing of a JFET

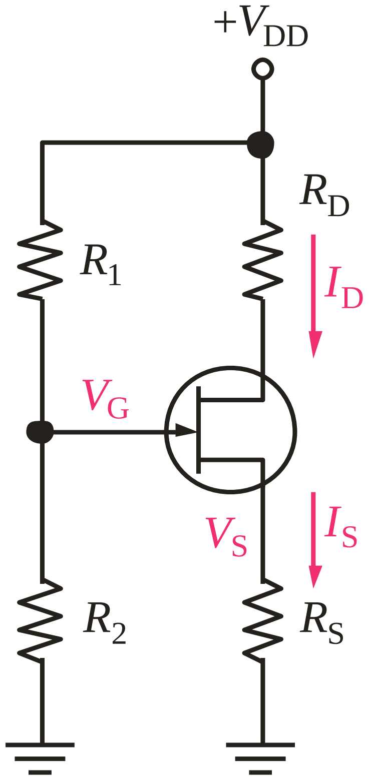
Self-bias is simple and effective, so it is the most common biasing method for JFETs. With self bias, the gate is essentially at 0 V.

An *n*-channel JFET is illustrated. The current in R_S develops the necessary reverse bias that forces the gate to be less than the source.



Voltage Divider Biasing

Voltage-divider biasing is a combination of a voltage-divider and a source resistor to keep the source more positive than the gate.



V_G is set by the voltage-divider and is independent of V_S. V_S must be larger than V_G in order to maintain the gate at a negative voltage with respect to the source.

Voltage-divider bias helps stabilize the bias for variations between transistors.

Current Source Biasing

An even more stable form of bias is current-source bias. The current-source can be either a BJT or another FET. With current-source biasing, the drain current is essentially independent of V_{GS}.

In this circuit Q_2 serves as a current source for Q_1. An advantage to this particular circuit is that the output can be adjusted (using R_{S2}) for 0 V DC.