In your report for this section, carefully explain the theory behind your method. Include plots of any pertinent waveforms.

2. Design of a Time Constant

Design a resistive circuit with 2 or 3 nodes or meshes that includes one 0.1uF capacitor. The design objective is to get the time constant of the voltage waveform across the capacitor to be as close as possible to 0.1mS. Use the resistor values supplied.

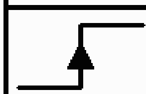
Explain carefully your theoretical analysis for this question. Explain how you arrived at your design. Compare your theoretical analysis with your measured responses. Include relevant waveforms in your report.

3. Square Wave Oscillator Circuit:

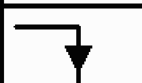
Please note that the 555 timer comes in an 8-pin Dual Inline Package (DIP) IC package. The dot on the top of the package marks pin 1. The remaining pins are numbered sequentially in a counterclockwise direction from pin one.

Refer to the internal block diagram of the 555 timer in Figure 1 on Page 5 (of the 555 timer book).. The blocks labeled '**C1**' and '**C2**' are comparators: whenever the external input exceeds the input connected to the internal voltage divider chain, the output goes high (to Vcc, or +15V). Otherwise the output is low (Ground or 0 volts). Note that the comparators have high impedance inputs, which means that for the most part it is safe to assume that connecting the comparator input to your external circuit won't affect the external circuit. The flip-flop (FF) is a digital logic block with the following properties:

1) If the input B is HIGH and the input A goes from LOW (LO) to HIGH the output goes to HIGH

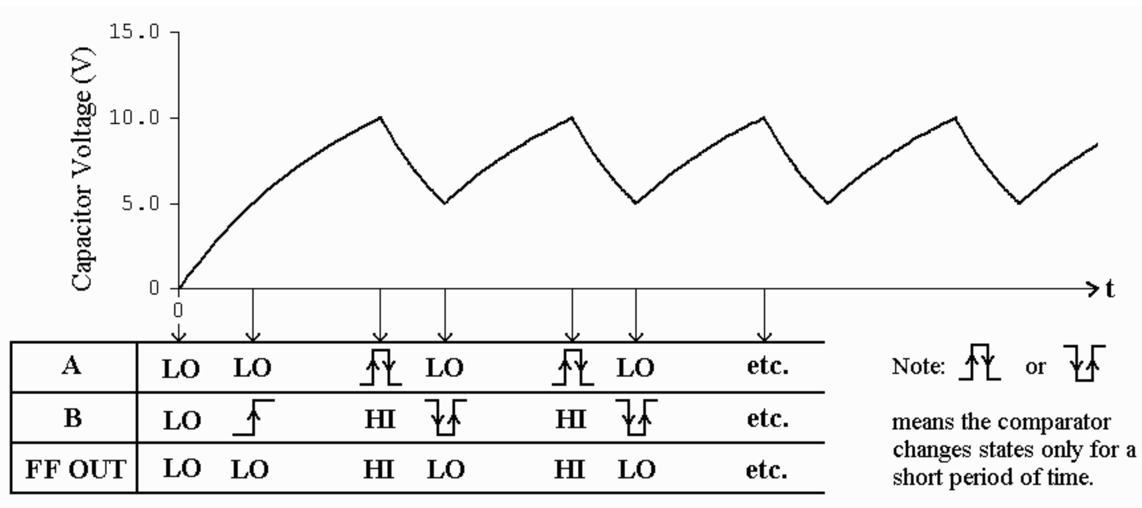
A	B	OUT
	HIGH	HIGH

2) If input A is LOW and the input B goes from HIGH to LOW, then the output goes to LOW

A	B	OUT
LO		LO

When the FF output is HIGH, the output transistor is turned ON. When the transistor is ON, the collector-emitter path has very low resistance. When the transistor is OFF (which is the case when the FF output is LOW), the transistor has very high resistance in its collector-emitter path. Note: In this application the transistor is being used as a **switch**.

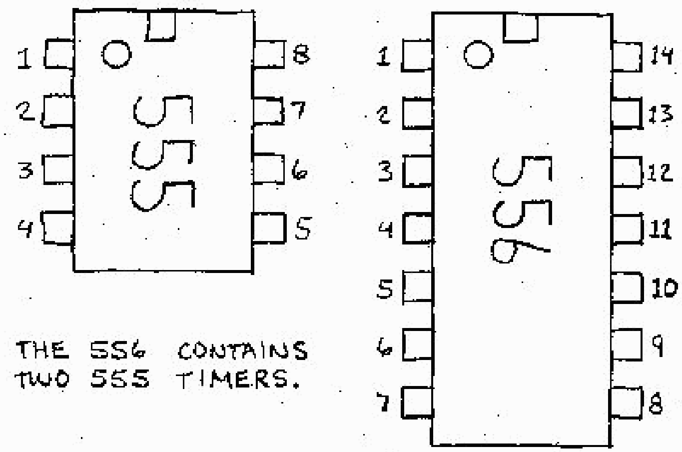
Now refer to the Basic Astable Circuit of Figure 2 on Page 7 (of the 555 timer book). When the power supply is first turned on, the capacitor voltage is zero and the capacitor begins to be charged by the power supply (Vcc) through R1 and R2. At this stage, the FF output is low, and the transistor is OFF, so pin 7 appears as an open circuit. As the capacitor charges, the voltage on pins 2 and 6 rises. It rises to the point where comparator C1 goes HIGH, but this does not affect the output of the flip-flop, which remains LOW. As the capacitor voltage continues to rise, eventually it turns on comparator C2. As a result, condition 1) described above for the FF is satisfied, and the FF output goes to HIGH. Then pin 7 becomes essentially a short circuit to ground. The capacitor then starts to discharge through R2 to ground. Comparator C2 goes to LOW (this does not affect the FF output yet). After the capacitor has sufficiently discharged, comparator C1 will eventually go to LOW, thereby satisfying condition 2). Thus, the FF output goes to LOW, the transistor turns off, and the cycle resumes. An illustration of this entire process is shown in the figure below.



Exercise: Design a circuit using the 555 timer, so that the waveform on output pin 3 is a periodic square wave, which is high for 0.667mS and low for 0.333mS.

Explain carefully your design procedure, using the appropriate formulas. Build your circuit and compare your predicted theoretical response with your measured response. Note: Ideally, the timing values are independent of the supply voltage. However, in practice this is not necessarily so. The use of a 9V power supply is recommended.

555/556 PIN OUTLINES



THE 556 CONTAINS TWO 555 TIMERS.

FUNCTION	555	556 (1)	556 (2)
GROUND	1	7	7
TRIGGER	2	6	8
OUTPUT	3	5	9
RESET	4	4	10
CONTROL V	5	3	11
THRESHOLD	6	2	12
DISCHARGE	7	1	13
V_{cc}	8	14	14

555 SPECIFICATIONS [1]

SUPPLY VOLTAGE (V_{cc})	4.5 TO 15 V
SUPPLY CURRENT (V_{cc} = +5V)	3 TO 6 mA
SUPPLY CURRENT (V_{cc} = +15V)	10 TO 15 mA
OUTPUT CURRENT (MAXIMUM)	200 mA
POWER DISSIPATION	600 mW
OPERATING TEMPERATURE	0 TO 70° C

1 VALUES SHOWN APPLY TO NE555.

ENGINEER'S MINI-NOTEBOOK

555 CIRCUITS

BY
FORREST M. MIMS, III

FIRST EDITION
FIRST PRINTING — 1984

A SILICONCEPTS™ BOOK

PRINTED IN THE UNITED STATES OF AMERICA

PLEASE READ THIS FIRST...

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THANKS IN ADVANCE TO THOSE OF YOU WHO WRITE! BUT PLEASE REMEMBER WE WILL BE UNABLE TO RESPOND PERSONALLY.

CONTENTS

INTRODUCTION

THE 555 TIMER IS ONE OF THE MOST POPULAR AND VERSATILE INTEGRATED CIRCUITS EVER PRODUCED. IT INCLUDES 23 TRANSISTORS, 2 DIODES AND 16 RESISTORS ON A SILICON CHIP INSTALLED IN AN 8-PIN MINI DUAL-IN-LINE PACKAGE (DIP). THE 556 IS A 14-PIN DIP THAT COMBINES TWO 555's ON A SINGLE CHIP. ALSO AVAILABLE ARE ULTRA-LOW POWER VERSIONS OF THE 555. THE 555 HAS TWO PRINCIPLE OPERATING MODES:

MONOSTABLE MODE – IN THIS MODE THE 555 FUNCTIONS AS A "ONE-SHOT." APPLICATIONS INCLUDE TIMERS, MISSING PULSE DETECTION, BOUNCEFREE SWITCHES, TOUCH SWITCHES, ETC.

ASTABLE MODE – THE 555 CAN OPERATE AS AN OSCILLATOR. USES INCLUDE LED AND LAMP FLASHERS, PULSE GENERATION, LOGIC CLOCKS, TONE GENERATION, SECURITY ALARMS, ETC.

CIRCUIT ASSEMBLY TIPS

BUILD TEST VERSIONS OF CIRCUITS ON PLASTIC SOLDERLESS BREADBOARD BEFORE MAKING THEM PERMANENT. IN MONOSTABLE CIRCUITS WHERE FALSE TRIGGERING MIGHT CAUSE PROBLEMS, TIE PIN 5 TO GROUND VIA A 0.1 µF CAPACITOR. IF POWER LEADS ARE LONG OR IF A CIRCUIT SEEMS TO MALFUNCTION, PLACE A 0.1 µF CAPACITOR ACROSS PINS 8 AND 1. A 1 µF CAPACITOR MAY ALSO BE NECESSARY. BE SURE TO EXPERIMENT WITH VALUES OF TIMING RESISTORS AND CAPACITORS. THE BASIC CIRCUITS ON PP. 6-7 EXPLAIN THE ROLE THESE COMPONENTS PLAY. REMEMBER THAT THE 556 REPLACES TWO 555's. LOW-POWER VERSIONS OF THE 555 MAY REQUIRE SOME REVISIONS TO STANDARD 555 CIRCUITS. FOR MORE TIPS, SEE THE RADIO SHACK BOOK "GETTING STARTED IN ELECTRONICS."

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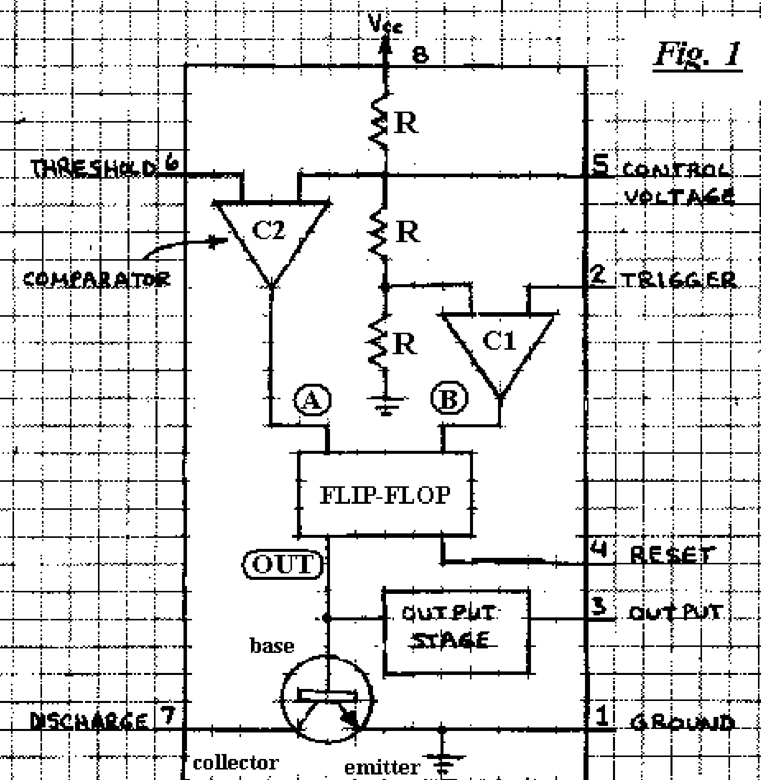
555 SPECIFICATIONS[1]

SUPPLY VOLTAGE (V_{cc})	4.5 TO 15 V
SUPPLY CURRENT (V_{cc} = +5V)[2]	3 TO 6 mA
SUPPLY CURRENT (V_{cc} = +15V)[2]	10 TO 15 mA
OUTPUT CURRENT	200 mA (MAXIMUM)
POWER DISSIPATION	600 mW
OPERATING TEMPERATURE	0 TO 70° C

1 VALUES SHOWN APPLY TO NE555 (8 PIN MINI-DIP).
2 OUTPUT CURRENT = 0.

INTERNAL BLOCK DIAGRAM

Fig. 1



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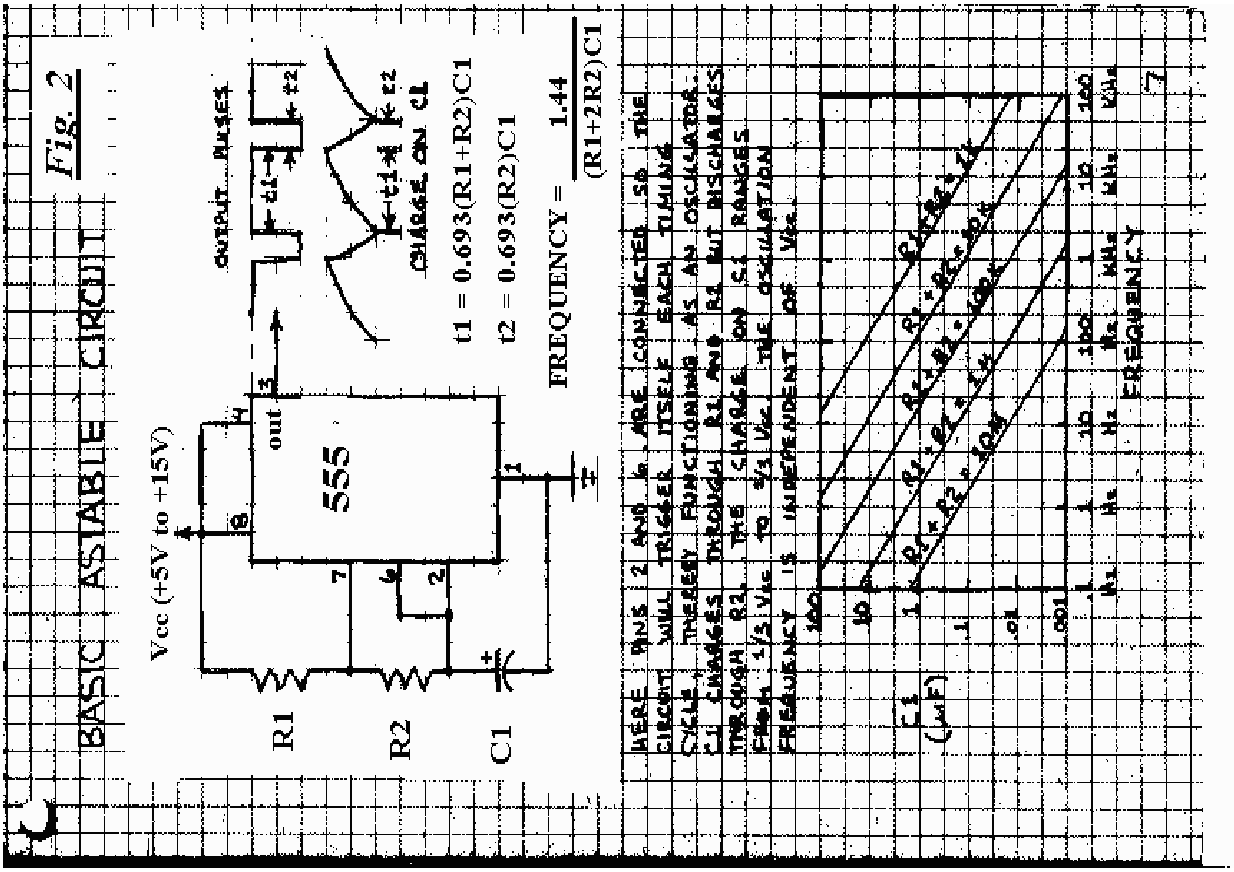
Fig. 2
BASIC ASTABLE CIRCUIT
Vcc (+5V to +15V)
R1
R2
C1
555
out
8
4
7
6
2
1
3
OUTPUT PULSES
t1
t2
CHARGE ON C1
t1 = 0.693(R1+R2)C1
t2 = 0.693(R2)C1
FREQUENCY = 1.44 / (R1+2R2)C1
HERE PINS 2 AND 6 ARE CONNECTED SO THE CIRCUIT WILL TRIGGER ITSELF EACH TIMING CYCLE, THEREBY FUNCTIONING AS AN OSCILLATOR. C1 CHARGES THROUGH R1 AND R2 BUT DISCHARGES THROUGH R2. THE CHARGE ON C1 RANGES FROM 1/3 Vcc TO 2/3 Vcc. THE OSCILLATION FREQUENCY IS INDEPENDENT OF Vcc.
C1 (μF)
100
10
1
.1
.01
.001
R1 + R2 = 1k
R1 + R2 = 10k
R1 + R2 = 100k
R1 + R2 = 1M
R1 + R2 = 10M
.1 Hz
1 Hz
10 Hz
100 Hz
1 kHz
10 kHz
100 kHz
FREQUENCY
7