Lecture #23

from Chapter 7 in Jaeger, Chapter 15 in Spencer

CMOS Logic Design

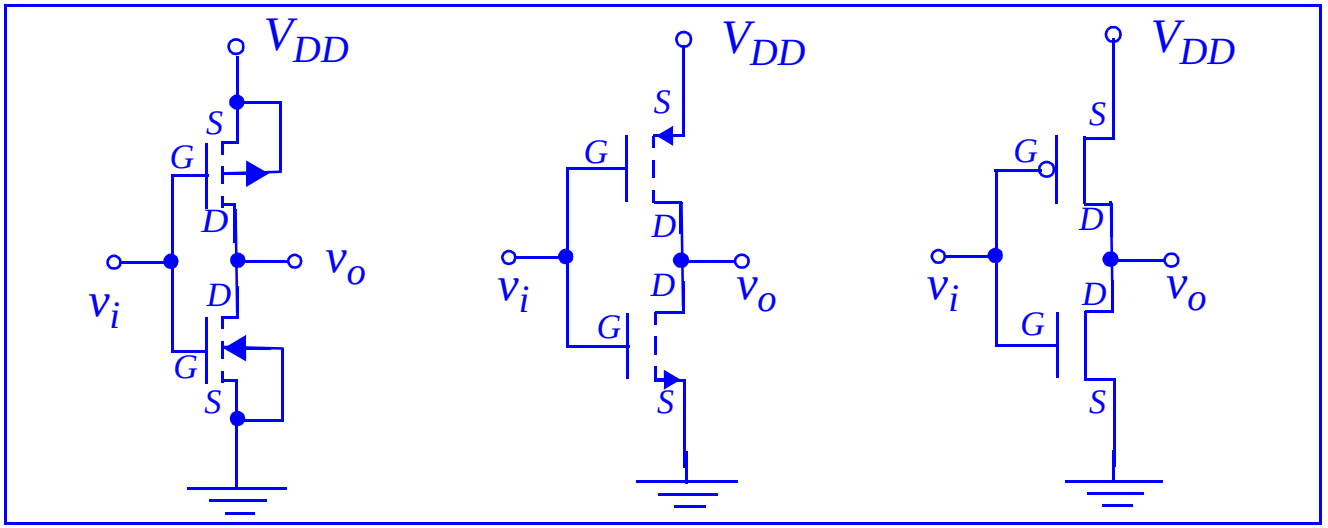
Outline/Learning Objectives:

- Explain the basic function of the primary digital circuit building block -the inverter.
- Describe (static) CMOS logic inverter technology.
- Analyze the (static) CMOS inverter circuit, including its voltage transfer characteristic and static and dynamic power dissipation.

Selected problems:

- 7.8, 7.23, 7.58, 7.60, 7.63

CMOS Inverter



B tied to S in both NMOS and PMOS devices.

V_{TH} NMOS - $$V_{TN} = V_{T0N} + \gamma_N\left(\sqrt{v_{SBN} + 2\phi_{FN}} - \sqrt{2\phi_{FN}}\right) \quad (1)$$

V_{TH} PMOS - $$V_{TP} = V_{T0P} - \gamma_P\left(\sqrt{v_{BSP} + 2\phi_{FP}} - \sqrt{2\phi_{FP}}\right) \quad (2)$$

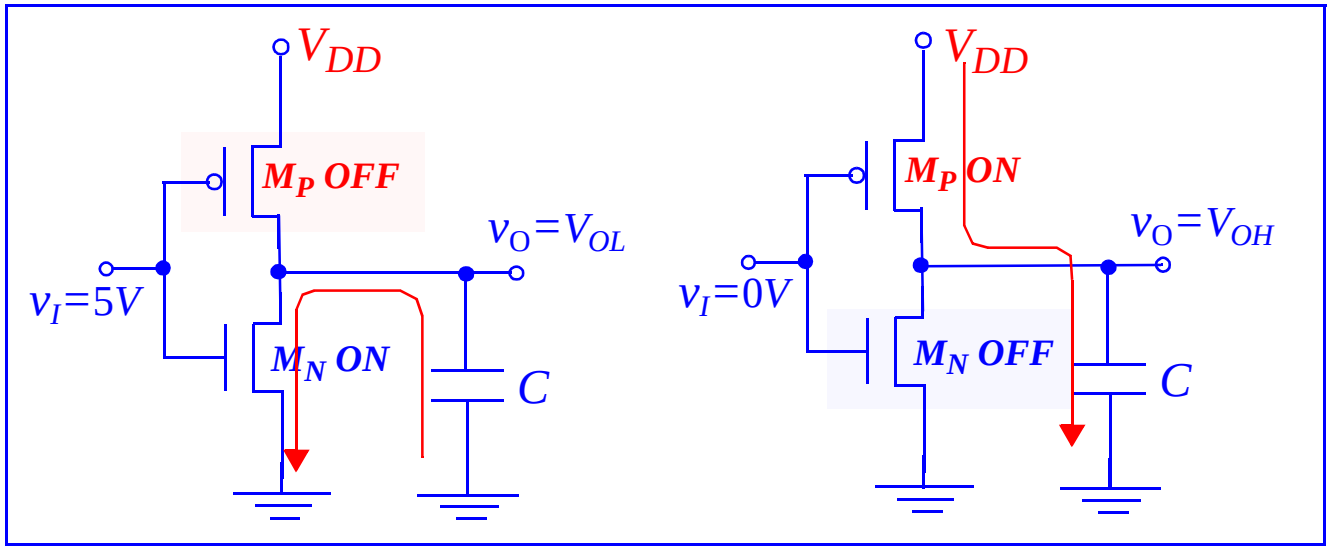
$$\gamma = \frac{\sqrt{2qN_{sub}\varepsilon_s}}{C_{ox}} = \text{body effect parameter } (V^{0.5}) \quad (3)$$

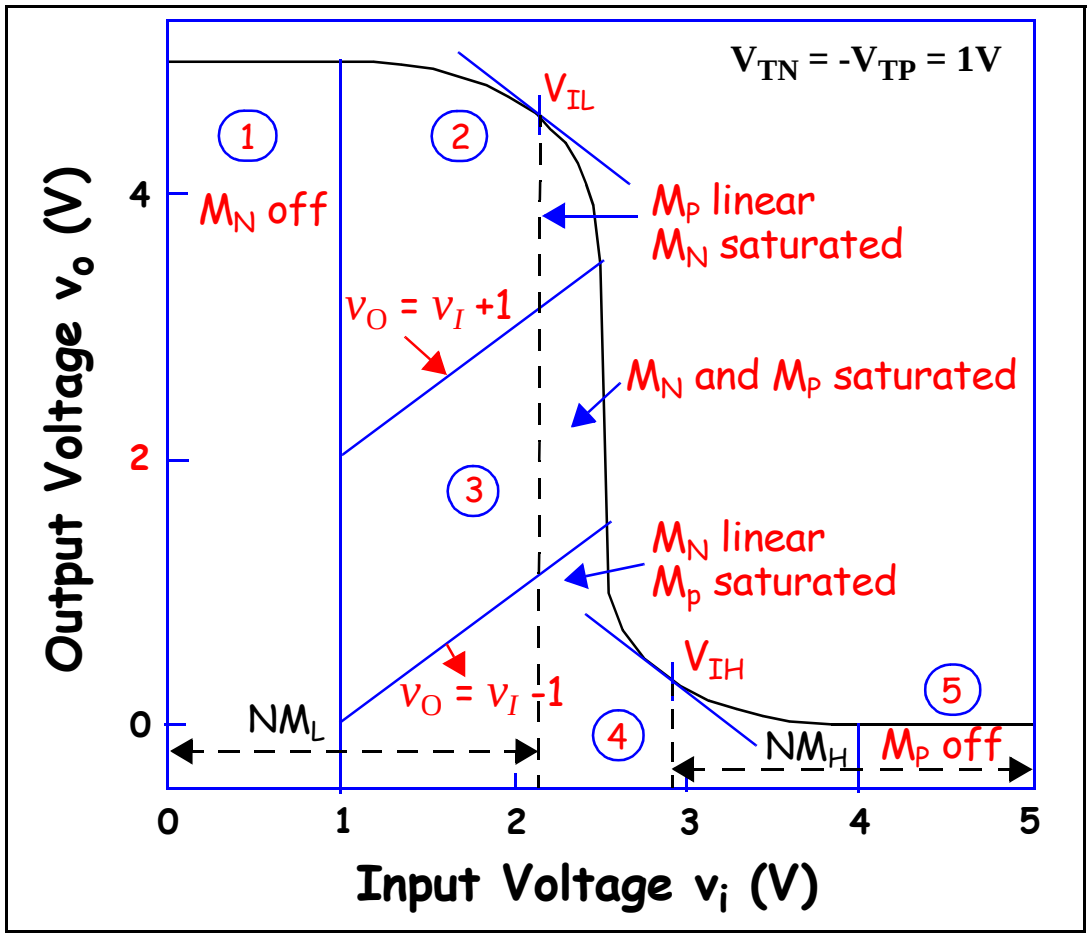
$2\phi_F$ = surface potential parameter $$\phi_F = \frac{kT}{q}\ln\left(\frac{N_{sub}}{n_i}\right) \quad (4)$$

Sample NMOS and PMOS Parameters

Parameter	NMOS	PMOS
V_{TO}	1 V	-1 V
γ	0.5 $V^{1/2}$	0.75 $V^{1/2}$
ϕ_F	0.60 V	0.70 V
K	25 $\mu A/V^2$	10 $\mu A/V^2$
λ	0.02 V^{-1}	0.02 V^{-1}

Static Characteristics of CMOS Inverter





Sat. of PMOS requires $v_{SD} \geq v_{SG} + V_{TP}$ or $\boxed{(5 - v_O) \geq (5 - v_I) - 1 \text{ or } v_O \leq v_I + 1}$ (5)

Sat. of NMOS requires $\boxed{v_{DS} \geq v_{GS} - V_{TN} \text{ or } v_O \geq v_I - 1}$ (6)

Regions of Operation of MOSTs in Symmetrical CMOS Inv.

Region	v_I	v_O	NMOS	PMOS
1	$v_I \le V_{TN}$	$V_{OH} = V_{DD}$	Off	Lin
2	$V_{TN} < v_I \le v_O + V_{TP}$	High	Sat	Lin
3	$v_I \approx V_{DD}/2$	$V_{DD}/2$	Sat	Sat
4	$v_O + V_{TN} < v_I \le V_{DD} - \lvert V_{TP}\rvert$	Low	Lin	Sat
5	$v_I \ge V_{DD} - \lvert V_{TP}\rvert$	$V_{OL} = 0$	Lin	Off

Noise Margins for the CMOS Inverter

High Input - PMOS sat., NMOS lin., so $i_{DSN} = i_{DSP}$

$$K_n\left(v_I - V_{TN} - \frac{v_O}{2}\right)v_O = \frac{K_p}{2}(V_{DD} - v_I + V_{TP})^2 \qquad (7)$$

$$K_R(2v_I - 2V_{TN} - v_O)v_O = (V_{DD} - v_I + V_{TP})^2 \quad \text{Note } \boxed{K_R = K_n/K_p} \qquad (8)$$

$$\boxed{v_O = (v_I - V_{TN}) \pm \sqrt{(v_I - V_{TN})^2 - \frac{(V_{DD} - v_I + V_{TP})^2}{K_R}}} \qquad (9)$$

$$V_{IH} = \frac{2K_R(V_{DD} - V_{TN} + V_{TP})}{(K_R - 1)\sqrt{1 + 3K_R}} - \frac{V_{DD} - K_R V_{TN} + V_{TP}}{K_R - 1} \quad (10)$$

$$NM_H = V_{OH} - V_{IH} = V_{DD} - V_{IH} \; . \quad (11)$$

For $K_R = 1$, $V_{IH} = \frac{5V_{DD} + 3V_{TN} + 5V_{TP}}{8}$ (12)

and $NM_H = \frac{3V_{DD} - 3V_{TN} - 5V_{TP}}{8}$ (13)

Low Input - PMOS lin., NMOS sat., $i_{DSN} = i_{DSP}$

$$K_p\left(V_{DD} - v_I + V_{TP} - \frac{V_{DD} - v_O}{2}\right)(V_{DD} - v_O) = K_n(v_I - V_{TN})^2 \quad (14)$$

$$(V_{DD} - 2v_I + 2V_{TP} - v_O)(V_{DD} - v_O) = K_R(v_I - V_{TN})^2 \quad (15)$$

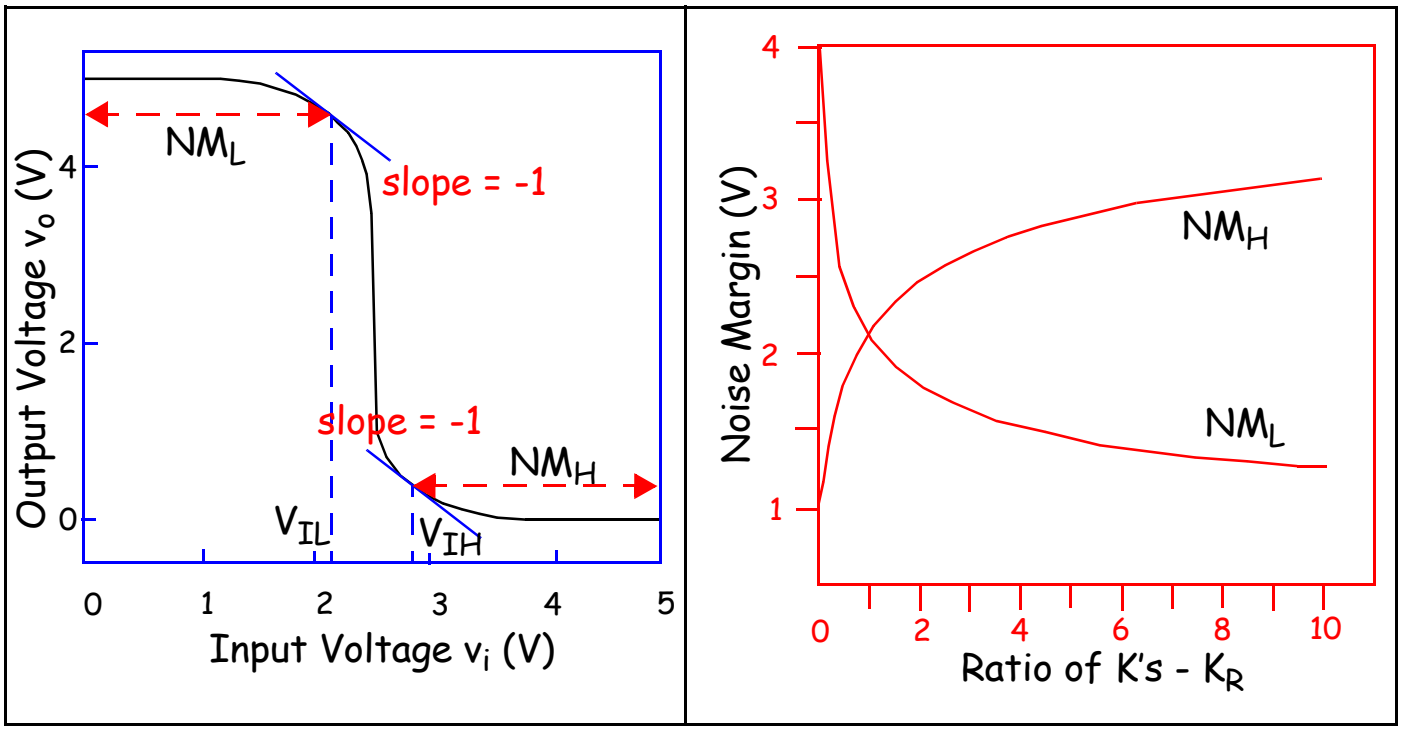
Note $K_R = K_n / K_p$

$$V_{IL} = \frac{2\sqrt{K_R}(V_{DD} - V_{TN} + V_{TP})}{(K_R - 1)\sqrt{K_R + 3}} - \frac{V_{DD} - K_R V_{TN} + V_{TP}}{K_R - 1} \quad (16)$$

$$NM_L = V_{IL} - V_{OL} = V_{IL} - 0 \tag{17}$$

For $K_R = 1$, $$V_{IL} = \frac{3V_{DD} + 5V_{TN} + 3V_{TP}}{8} \tag{18}$$

and $$NM_L = V_{IL} \tag{19}$$



Example: What are the noise margins of a minimum size CMOS inverter in which both W/L ratios are 2/1 with $K_n' = 25\ \mu A/V^2$ and $K_p' = 10\ \mu A/V^2$, $V_{DD} = 5.2\ V$ and $V_{TN} = -V_{TP} = 1\ V$?

$$K_R = \frac{K_n}{K_p} = 2.5$$

$$V_{IH} = \frac{2K_R(V_{DD} - V_{TN} + V_{TP})}{(K_R - 1)\sqrt{1 + 3K_R}} - \frac{V_{DD} - K_R V_{TN} + V_{TP}}{K_R - 1}$$

$$V_{IH} = \frac{2(2.5)(5.2 - 1 - 1)}{(2.5 - 1)(\sqrt{1 + 3(2.5)})} - \frac{5.2 - 2.5(1) - 1}{2.5 - 1} = 2.53V$$

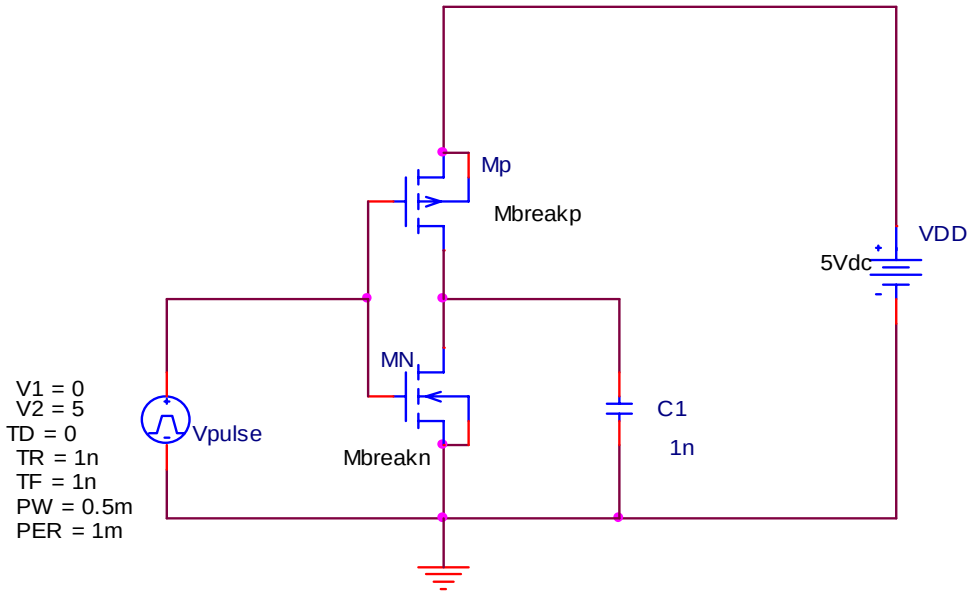
$$\therefore NM_H = V_{DD} - V_{IH} = 5.2 - 2.53 = 2.67V$$

$$V_{IL} = \frac{2\sqrt{K_R}(V_{DD} - V_{TN} + V_{TP})}{(K_R - 1)\sqrt{K_R + 3}} - \frac{V_{DD} - K_R V_{TN} + V_{TP}}{K_R - 1}$$

$$V_{IL} = \frac{2(\sqrt{2.5})(5.2 - 1 - 1)}{(2.5 - 1)(\sqrt{2.5 + 3})} - \frac{5.2 - 2.5(1) - 1}{2.5 - 1} = 1.83V$$

$$\therefore NM_L = V_{IL} = 1.83V$$

PSPICE EXAMPLE




```
*Libraries:

* Local Libraries :

.LIB ".\example9.lib"

* From [PSPICE NETLIST] section of C:\Program Files\OrcadLite\PSpice\PSpice.ini file:

.lib "nom.lib"

*Analysis directives:

.TRAN  0 20ms 0 1u
```

PSPICE EXAMPLE (Cont'd)

```
.PROBE V(*) I(*) W(*) D(*) NOISE(*)

.INC ".\example9-SCHEMATIC1.net"

**** INCLUDING example9-SCHEMATIC1.net ****

* source EXAMPLE9

M_MN          N00163 N00248 0 0 Mbreakn

V_Vpulse          N00248 0

+PULSE 0 5 0 1n 1n 0.5m 1m

V_VDD          N00144 0 5Vdc

M_Mp          N00163 N00248 N00144 N00144 Mbreakp

C_C1          0 N00163  1n

**** RESUMING example9-SCHEMATIC1-Example9.sim.cir ****

.END


 ****     MOSFET MODEL PARAMETERS

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```

PSPICE EXAMPLE (Cont'd)

```
            Mbreakn          Mbreakp
            NMOS             PMOS
            LEVEL    1               1
         L  100.000000E-06  100.000000E-06
         W  100.000000E-06  100.000000E-06
         VTO    1              -1
         KP  500.000000E-06  500.000000E-06
         GAMMA    0               0
         PHI     .6              .6
         LAMBDA    0              0
 ****     INITIAL TRANSIENT SOLUTION       TEMPERATURE =   27.000 DEG C
********************************************************************************
NODE   VOLTAGE     NODE   VOLTAGE     NODE   VOLTAGE     NODE   VOLTAGE
(N00144)    5.0000 (N00163)    5.0000 (N00248)    0.0000
```

PSPICE EXAMPLE (Cont'd)

```
VOLTAGE SOURCE CURRENTS

NAME          CURRENT

V_Vpulse      0.000E+00

V_VDD         -5.010E-12


TOTAL POWER DISSIPATION   2.51E-11  WATTS

JOB CONCLUDED

TOTAL JOB TIME            2.79
```

PSPICE EXAMPLE (Cont'd)