Lecture #24

CMOS Logic Design

- Describe and analyze the dynamic behavior of the CMOS logic inverter.
- Describe and analyze basic CMOS NOR and NAND logic gates.
- Describe and analyze MOS transmission gates and their use in MOS logic circuits.
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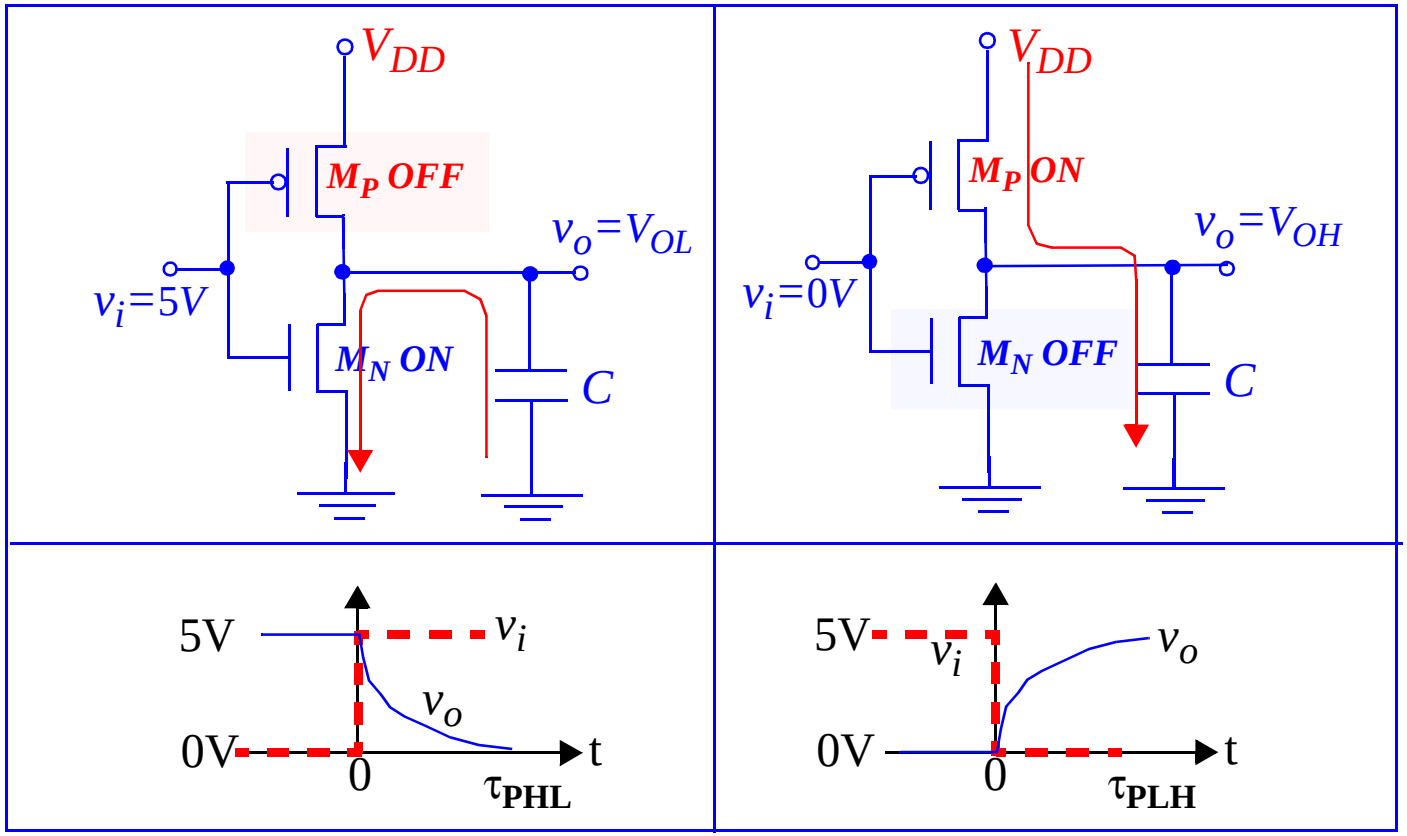
Dynamic Behavior of CMOS Inverter



$$\frac{k_n}{2}(v_{GS} - V_{TN})^2 = -C\frac{dv_o}{dt} \quad \text{for} \quad V_{DD} - V_{TN} \le v_o \le V_{DD}$$

$$k_n\left(v_{GS} - V_{TN} - \frac{v_o}{2}\right)v_o = -C\frac{dv_o}{dt} \quad \text{for} \quad 0.5V_{DD} \le v_o \le V_{DD} - V_{TN}$$

$$\tau_{PHL} = R_{onn}C\left\{\ln\left[4\left(\frac{V_{DD}-V_{TN}}{V_{DD}+V_{OL}}\right)-1\right]+\frac{1}{2}\right\} \quad \text{with} \quad R_{onn} = \frac{1}{K_n(V_{DD}-V_{TN})}$$

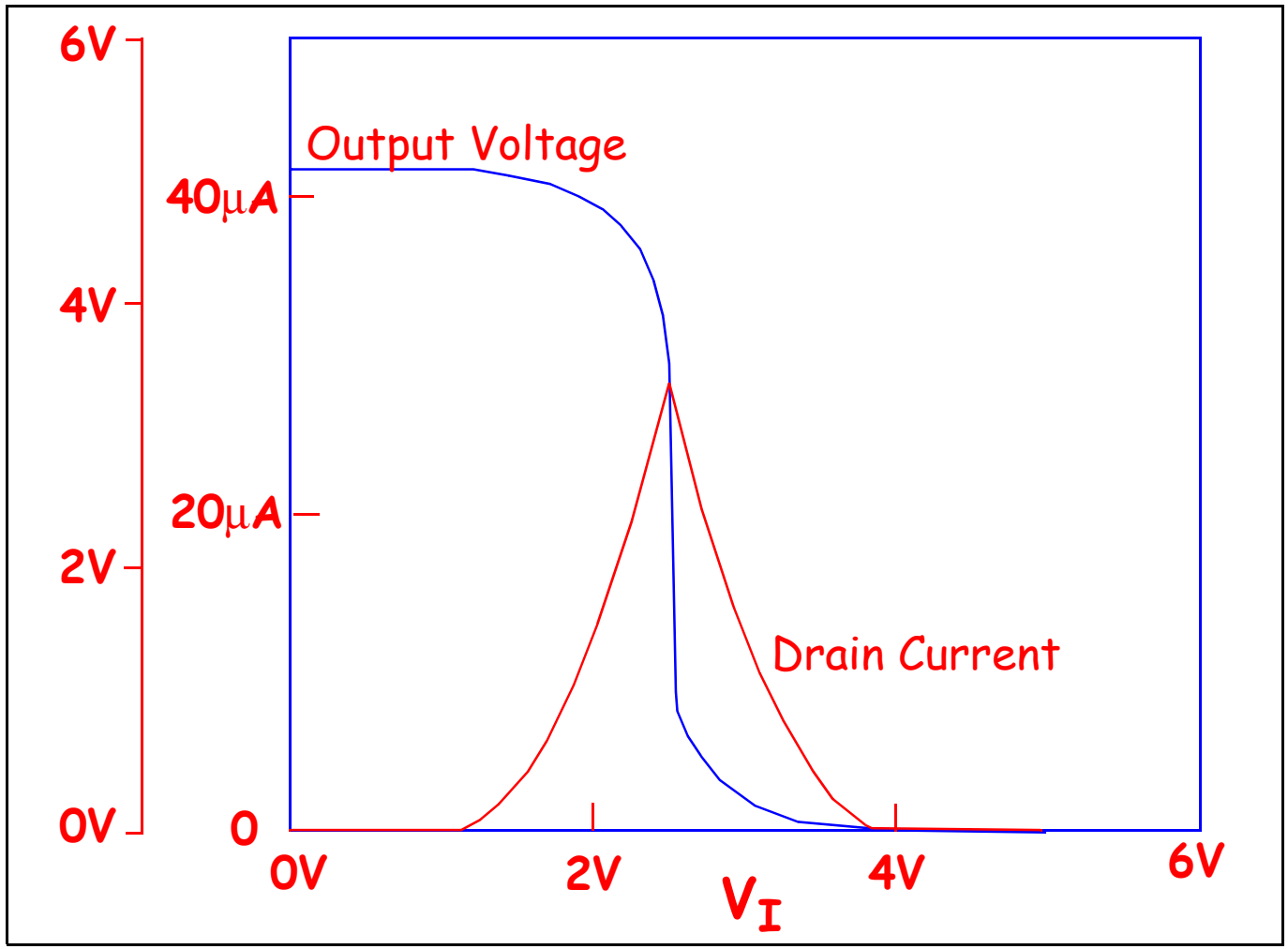
For CMOS inverter with V_{DD} = 5V, V_{TN} = 1V and V_{OL} = 0V.

$$\tau_{PHL} = 1.29R_{onn}C = 0.322\frac{C}{K_n}$$

The L to H propagation delay with V_{DD} = 5V, V_{TP} = -1V and V_{OH} = 5V.

$$\tau_{PLH} = 1.29R_{onp}C = 0.322\frac{C}{K_p} \quad \text{for} \quad R_{onp} = \frac{1}{K_p(V_{DD}+V_{TP})}$$

Static and Dynamic Power Dissipation in CMOS



Output Voltage and Supply Current versus Input Voltage for Symmetrical CMOS Inverter

Dynamic power dissipation is $\boxed{P_D = CV_{DD}^2 f}$

Switching power dissipation - $i_{DS} = 0$ for $v_I \le V_{TN}$ and $v_I > (V_{DD} - |V_{TP}|)$.

For $V_{TN} \le v_I \le (V_{DD} - |V_{TP}|)$, $i_{DS} \neq 0$ and the current peaks when $v_I = v_O = V_{DD}/2$

For high speed CMOS, $\boxed{P_{SW} \sim 0.2 \text{ to } 0.3 \; P_D}$ (24)

Example: A CMOS inverter has $V_{TN} = -V_{TP} = 1V$, $K_n' = 20\mu A/V^2$, $K_p' = 15\mu A/V^2$, $(W/L)_N = (W/L)_P = 20/1$ and $V_{DD} = 4.8V$. What is the peak current in the logic gate and at what input voltage does it occur.

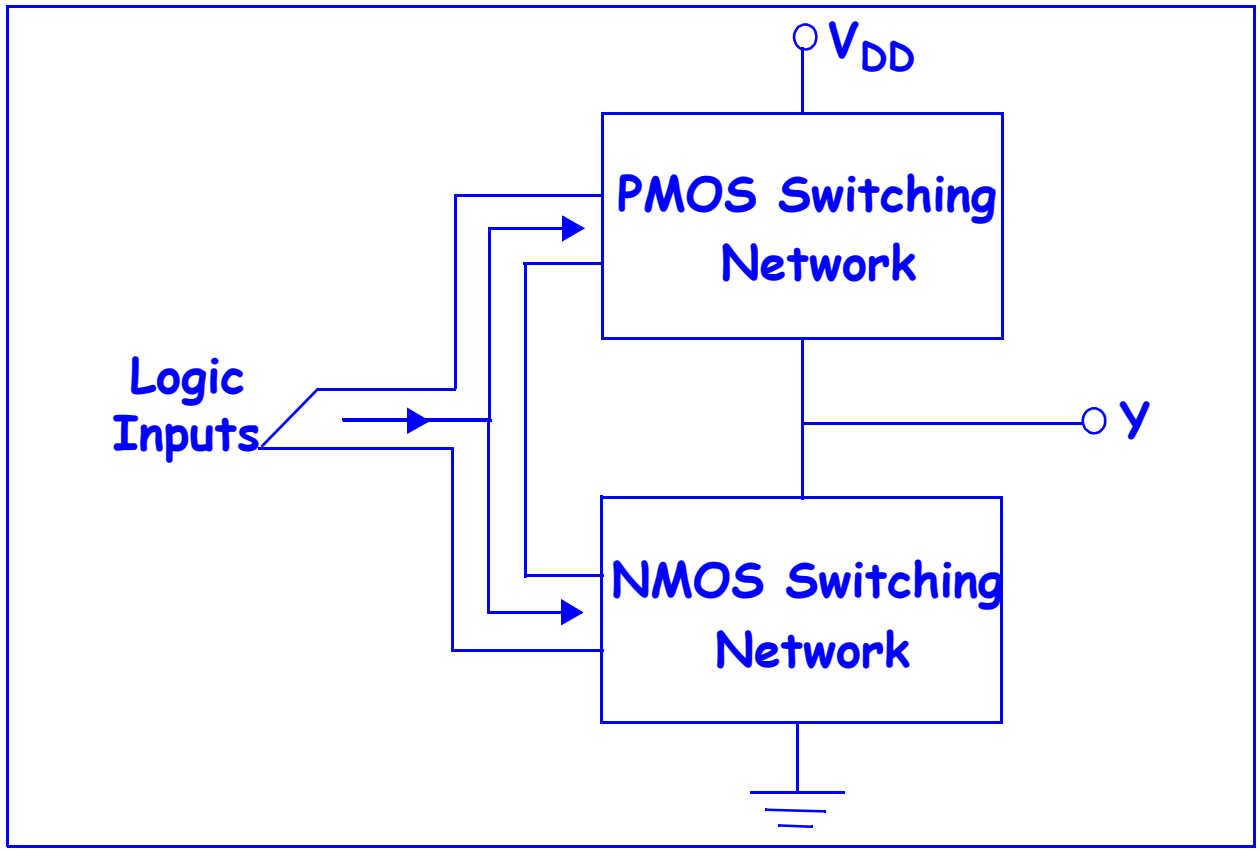
$$\frac{K_n'}{2}\left(\frac{W}{L}\right)_N (v_{GS} - V_{TN})^2 = \frac{K_p'}{2}\left(\frac{W}{L}\right)_P (v_{SG} + V_{TP})^2$$

$$\frac{20\times10^{-6}}{2}\left(\frac{20}{1}\right)(v_I - 1)^2 = \frac{15\times10^{-6}}{2}\left(\frac{20}{1}\right)(4.8 - v_I - 1)^2 \Rightarrow 1.15(v_I - 1) = 3.8 - v_I$$

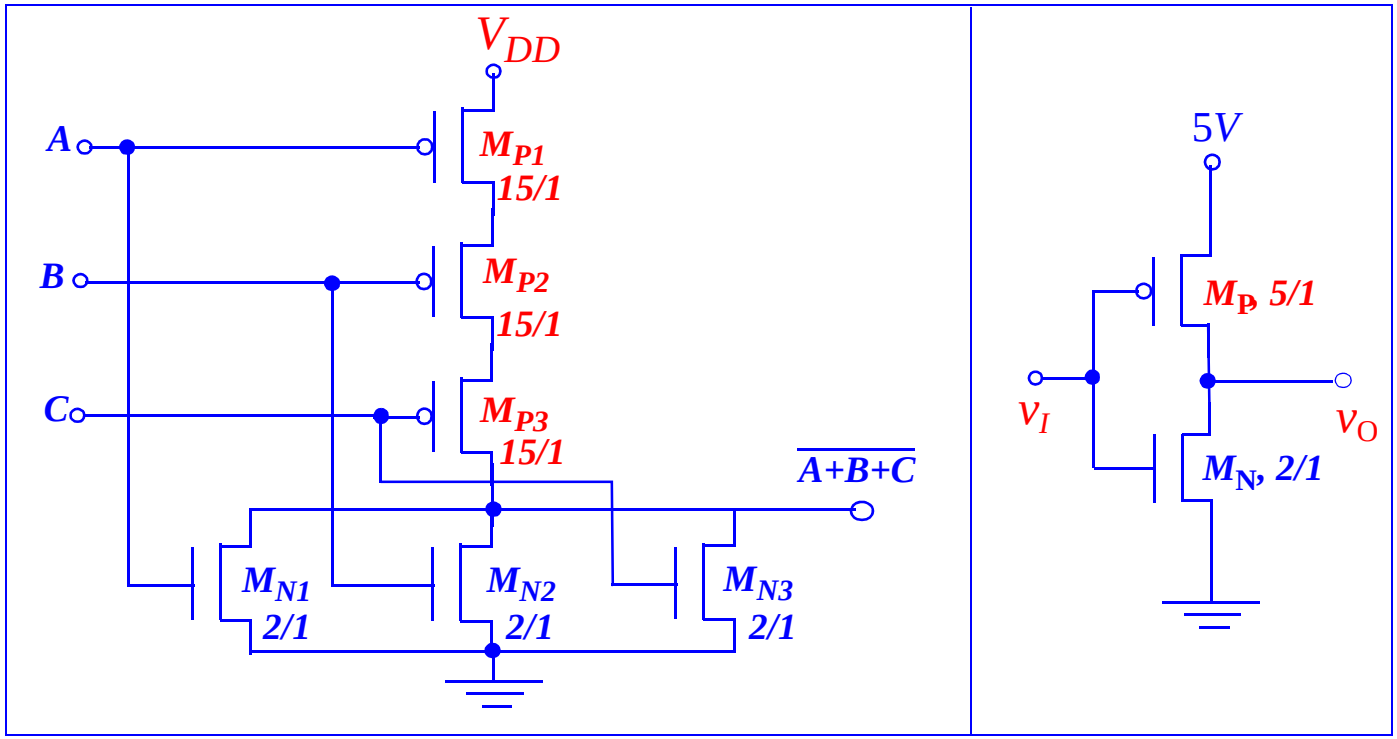
$$\therefore v_I = \frac{3.8 + 1.15}{1.15 + 1} = 2.30V$$

$$\therefore i_{peak} = \frac{20\times10^{-6}}{2}\left(\frac{20}{1}\right)(2.30 - 1)^2 = 338\mu A$$

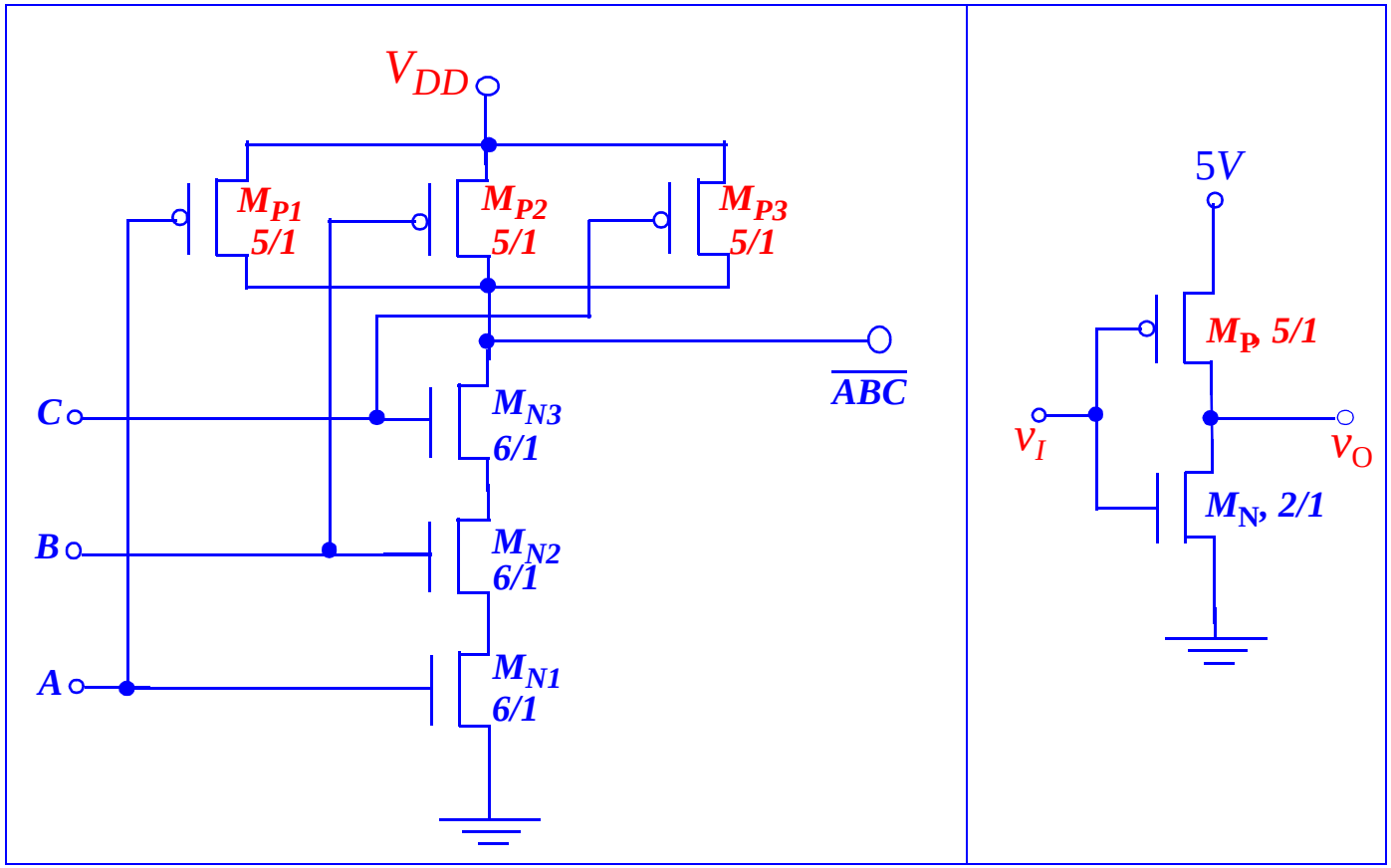
CMOS NOR and NAND Gates



Three Input NOR Gate



Three Input NAND Gate

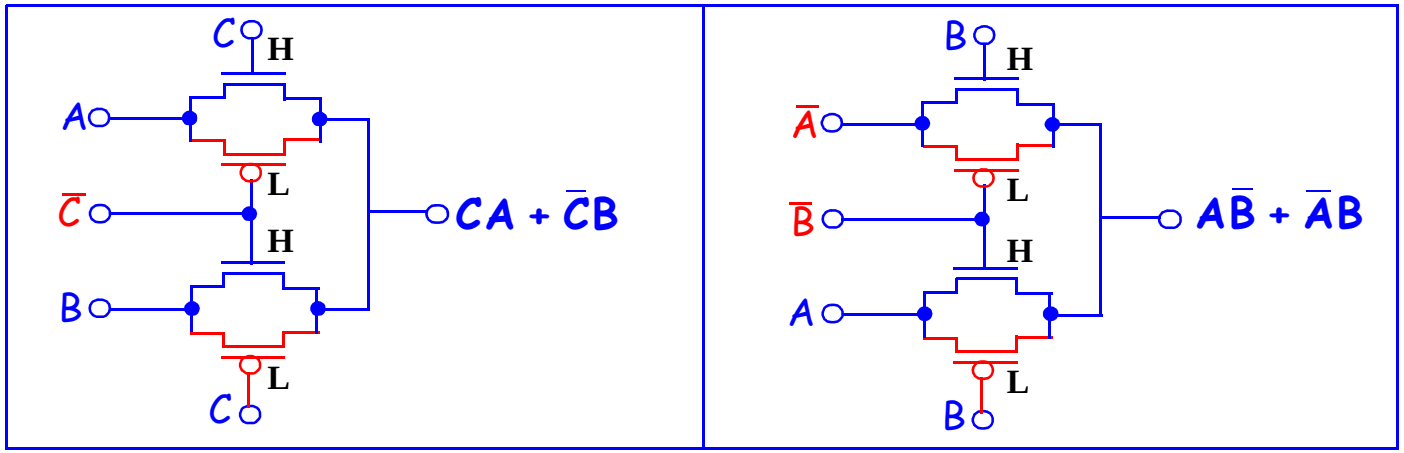


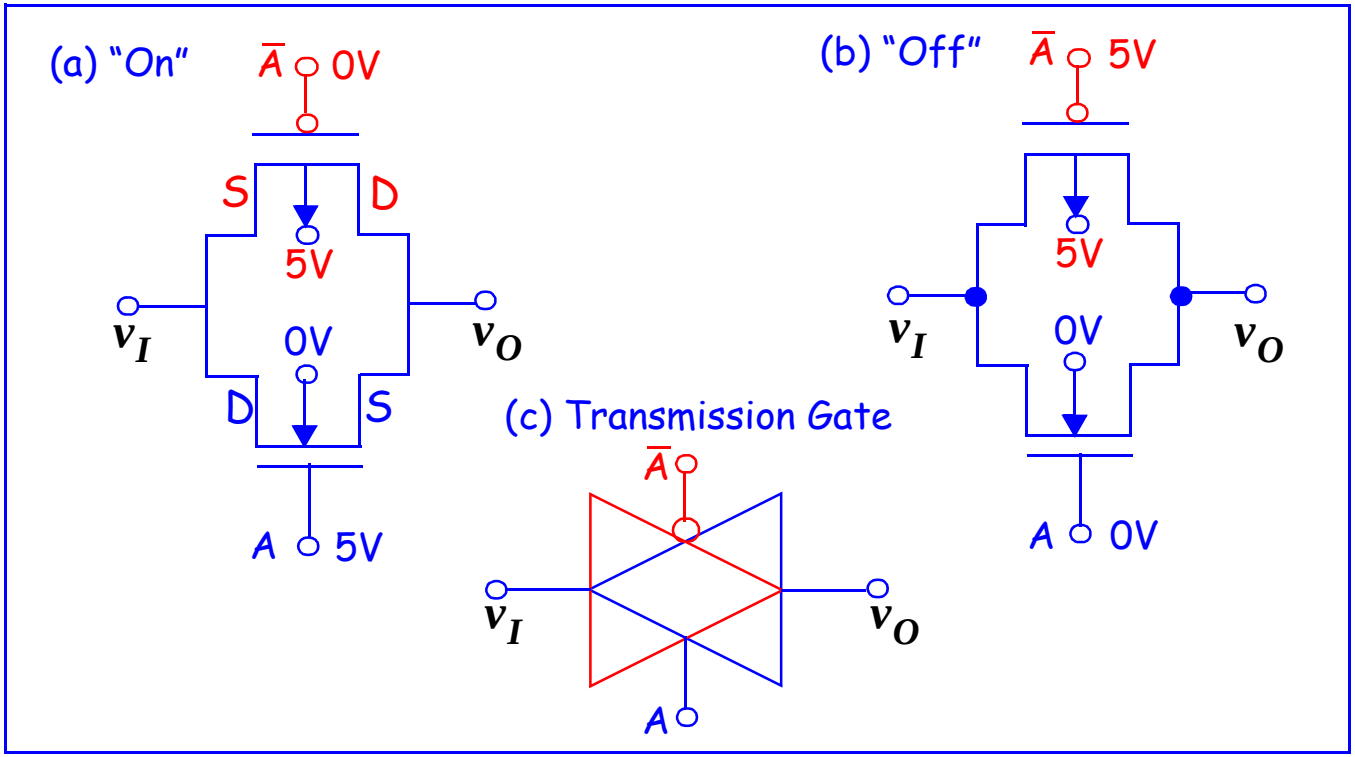
MOS Transmission Gate

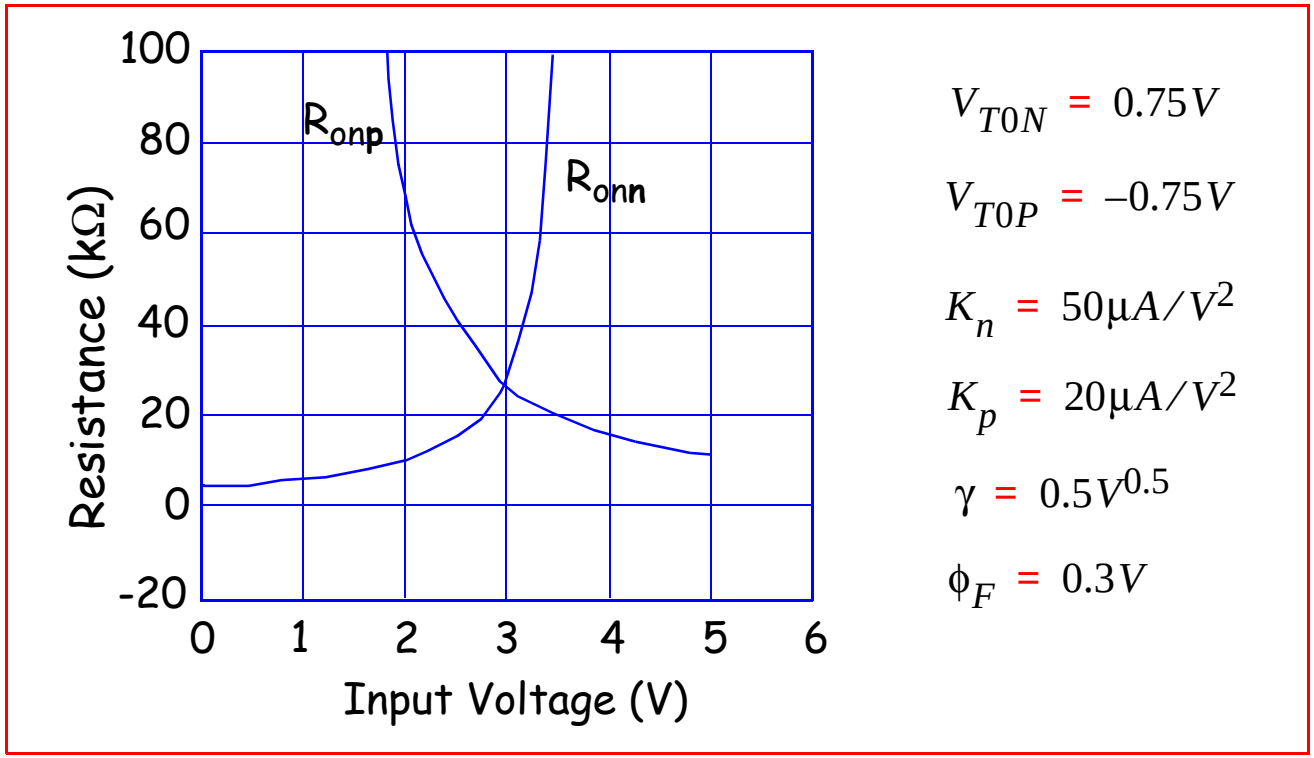
Useful in analog and digital design.

It is a bi-directional resistive connection between v_I and v_O.

The equivalent resistance is $\boxed{R_{EQ} = \dfrac{R_{onp} R_{onn}}{R_{onp} + R_{onn}}}$.


C
H
A
L
C
H
B
L
C
CA + CB
B
H
A
L
B
H
A
L
B
AB + AB


(a) "On"
A 0V
S
D
5V
v_I
0V
v_O
D
S
A 5V
(b) "Off"
A 5V
5V
v_I
0V
v_O
A 0V
(c) Transmission Gate
A
v_I
v_O
A



$V_{T0N} = 0.75V$

$V_{T0P} = -0.75V$

$K_n = 50\mu A/V^2$

$K_p = 20\mu A/V^2$

$\gamma = 0.5V^{0.5}$

$\phi_F = 0.3V$

$R_{onp} = \infty$ for $v_I \leq 1.36V$ PMOS is OFF.

$R_{onn} = \infty$ for $v_I \geq 3.64V$ NMOS is OFF. Can use $R_{on} \propto 1/K$ in design.