

## Design Objectives for Four-Resistor Bias Network

$$V_{EQ} = R_{EQ}I_B + V_{BE} + R_E I_E$$

$$I_E = \frac{V_{EQ} - V_{BE} - R_{EQ}I_B}{R_E} \text{ or}$$

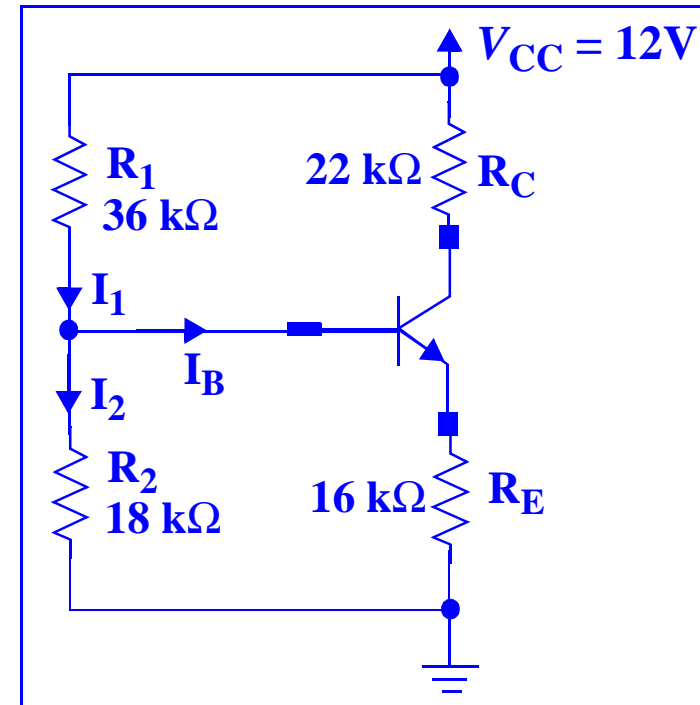
$$I_E \approx \frac{V_{EQ} - V_{BE}}{R_E} \text{ for } R_{EQ}I_B \ll V_{EQ} - V_{BE}$$

$R_{EQ}$  is designed so that its voltage drop is negligible.

In this case,  $I_E$  is determined by  $V_{EQ}$ ,  $V_{BE}$

$$\text{and } R_E. \quad I_E \approx \frac{V_{EQ} - V_{BE}}{R_E} = \frac{4 - 0.7}{16\text{k}} = 206\mu\text{A}.$$

Another constraint is power dissipation. Choose  $I_2 \leq I_C/5$ . Now, power dissipated in  $R_1$  and  $R_2$  is less than 17% of total quiescent power. Also,  $I_2 \gg I_B$  for  $\beta_F \geq 50$ .



## Basic Current Mirror

For  $V_{BE} = 0.7V$ ,  $\beta_F = 100$ ,  $V_A = 0V$  and  $I_S = 1.4 \times 10^{-16}A$  (redundant). Find  $I_{REF}$  and  $I_{C2}$ . Assume that both transistors are matched.

Both transistors operate in forward-active region.

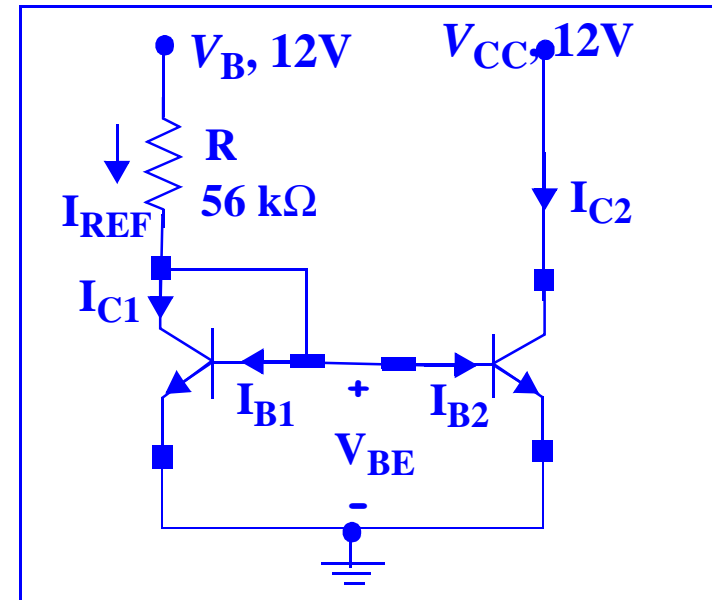
$$I_{REF} = \frac{V_B - V_{C1}}{R} = \frac{12 - 0.7}{56k} = 202\mu A$$

$$I_{REF} = I_{C1} + I_{B1} + I_{B2} \text{ but } \frac{I_{C1}}{\beta_F} = I_{B1} = I_{B2}$$

$$\therefore I_{REF} = I_{B2}(\beta_F + 2) \Rightarrow I_{B2} = 1.98\mu A$$

$$\text{Therefore, } I_{C2} = \beta_F I_{B2} = 198\mu A \approx I_{REF}$$

$$I_S = \frac{I_C}{e^{V_{BE}/V_T}} = \frac{198\mu A}{e^{0.7/0.025}} = 1.37 \times 10^{-16} A$$



## Two-Resistor Bias Circuit

Find the Q-point for the circuit shown if  $\beta_F = 75$  and  $V_{BE} = 0.7V$ .

$$10 = 1.2k(I_C + I_B) + 5kI_B + V_{BE}$$

Assume transistor operates in forward-active region,

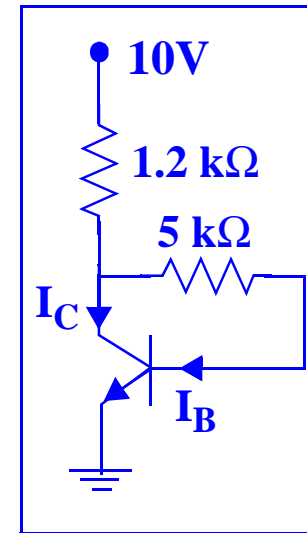
$$I_C = \beta_F I_B \text{ and } 10 = 1.2k(\beta_F I_B + I_B) + 5kI_B + V_{BE}.$$

$$I_B = \frac{10 - V_{BE}}{1.2k(\beta_F + 1) + 5k}$$

$$I_C = \beta_F I_B = \beta_F \left[ \frac{10 - V_{BE}}{1.2k(\beta_F + 1) + 5k} \right] = 75 \left[ \frac{10 - 0.7}{1.2k(75 + 1) + 5k} \right] = 7.25mA$$

$$V_{CE} = 10 - 1.2k(I_C + I_B) = 10 - 1.2k \left( I_C + \frac{I_C}{\beta_F} \right) = 1.18V$$

Since  $V_{CE} > V_{BE} > 0$ , our assumption is correct.



## A PNP Transistor Example

Find the Q-point of the shown circuit

since the emitter is connected to a higher potential than the base we have  $V_{EB} = 0.7V$

The emitter current is found through the loop

$$10 = 0.7 + 2I_E \quad \text{to get} \quad I_E = 4.65mA$$

Assuming forward active region we have  $I_C = \alpha I_E = 4.6mA$

Checking the region of operation by calculating  $V_{CB}$  we get

$$V_{CB} = -10 + I_C \times 1K = -5.4V$$

it follows that the Collector-base junction is reverse-biased and our assumption of forward active region is correct

