Lab #1  Computer-aided Logic Design

Objectives:

- to introduce concepts in the computer-aided design of digital logic circuits
- to gain practical experience with the use of in-circuit programmable CPLDs
- to gain experience with the use of a logic analyzer

Preparation:

1. What is the average value and RMS value of a 0 to 5V square wave?

   Average value = _______________    RMS value = _______________

2. Write a VHDL program for a 4-bit equality detector. That is, a combinational circuit that accepts two 4-bit inputs and generates a single bit output that is HI when the two 4-bit inputs are equal.

3. Review/familiarize yourself with the tutorials in Appendix B of the textbook, specifically, pages 740 to 767 and pages 770 to 779 and pages 781 to 787.

4. Study the circuits given in the graphic design files (.gdf) available on the course web site that implement simple 4-bit counters, one with a synchronous clear and the other with asynchronous clear. You may simulate these before the lab to verify their state behaviour.

5. Review the implementation of a binary-to-BCD look-up table (LUT) in a ROM. Assume BCD numbers are available in the range 00-99 on the 8-bit output of the ROM.

Devices used:

- EPM3032ALC44-10 Programmable Logic Device (CPLD)
- 2732A EPROM (programmed with binary to BCD conversion)
- Agilent 54622DD Mixed-signal oscilloscope
- Max+PLUS 2 Altera design software
- HP (Agilent) 33120A Function/Waveform generator

Introduction and Background:

Modern design techniques for electronic and logic circuits rely heavily on computer-aided systems for synthesis, simulation and realization; a variety of commercial packages are available. We will be using the MAX+plus II package which is marketed by Altera Corp. This is a design environment that includes all the typical components for professional design such as schematic capture, an HDL compiler, simulation, VHDL compilation and CPLD programming.
The devices we will use in this lab are manufactured by Altera and are known as in-circuit programmable parts which means that they can be downloaded with configuration programming while remaining connected in the target circuit. This is done with a simple, serial connection (JTAG) interface to the device. There are families of GALs (eg. GAL22V10) and complex programmable logic devices (CPLDs) of many various configurations. The device we will use is the Altera EPM3032ALC44-10 (or more simply the “3032”) which is a CPLD (member of the 3000 family) packaged in a 44-pin PLCC (plastic-leaded chip carrier) and a 10ns maximum delay specification.

**Experiment:**

**Part 1: 8-bit Counter**

1. Compile your VHDL design for the 4-bit equality detector (comparator) and download to the 3032 device. Test its operation with LED’s and toggle switches. Store the design as a symbol to be used later.

2. Find the 8-bit counter 8COUNT in the megafuctions library (c:\maxplus2\max2lib\mf) and implement in the 3032 device. You will of course have to add input and output nodes using the schematic editor. Test the counter operation with LEDs and toggle switches and verify its proper operation. Use toggle switch 15 on the I/O module as the clock input (switches 15, 14, 13 and 12 are debounced internally). Check the operation of the ripple carry output (COUT) as well as the up/down control (DNUP), the synchronous Load (LDN) and asynchronous clear (CLRN).

3. Check the output of the function generator using analog channel 1 of the 54622D ’scope (use Auto-scale button on front panel). Using the automated measurement features (use Quick Meas button on front panel), verify the clock frequency, period, rise times, duty cycle and voltages as requested below. Explain any discrepancies from the ideal case and the values you obtained in the preparation for this lab.

<table>
<thead>
<tr>
<th>Freq: ________</th>
<th>Period: __________</th>
<th>Rise time: __________</th>
<th>Fall time: __________</th>
</tr>
</thead>
<tbody>
<tr>
<td>Max voltage: __________</td>
<td>Min voltage: _________</td>
<td>Peak-to-peak voltage: __________</td>
<td></td>
</tr>
<tr>
<td>Avg voltage: __________</td>
<td>RMS voltage: __________</td>
<td>Duty cycle: __________</td>
<td></td>
</tr>
</tbody>
</table>

*Verify that you have a 0-5V, 1 MHz square wave from the function generator before you proceed to the next section. Ask for help if your function generator does not produce this waveform by default.*

4. Now connect the free running 1 MHz clock to the counter (display on ’scope channel 1), display COUT on channel 2, and connect digital channels D7-D0 of the logic analyzer to the 8 output bits of the counter. On the front panel of the ’scope, turn on the display of digital channels D7-D0 (using the D7 Thru D0 button), turn off display of digital channels D15-D8 (using the D15 Thru D8 button), and turn both analog channels 2 and 1 on. You should now have 8 digital and 2 analog displays on the screen. Adjust the vertical size using the 3rd “soft key” for the digital channels and the vertical sensitivity knobs for the analog channels to allow display of all ten channels simultaneously. Be sure that the threshold is set to TTL using the 4th “softkey”.


PLEASE BE CAREFUL WITH LOGIC ANALYZER LEADS - THEY ARE DELICATE and EXPENSIVE TO REPLACE !! DO NOT MOVE THEM FROM THE BREADBOARD!

5. Set up the scope to trigger when the bit pattern 00000000 appears on channels D7-D0. This is done using the “Trigger” controls section of the 'scope front panel. Using the Pattern button, set the trigger to XXXX XXXX LLLL LLLL. Each bit is selected using the rotary entry knob and its value (either X, L or H) is chosen with the softkey. Try changing the trigger bit pattern and verify that the waveforms that are displayed start at the corresponding position.

6. Using the features of the 'scope, completely verify the operation and timing of the counter including the COUT pulse. Note carefully where it occurs and its width for the 1MHz counter clock:

COUT pulse width = _________ COUT frequency = ___________ COUT duty cycle = ___________

7. Connect the lowest 8-bits of the EPROM address to the counter and use the logic analyzer to verify its contents (binary to BCD look-up table). Ground the /OE, /CS and address bits A8 to A11 of the EPROM. Connect inputs D15-D8 of the logic analyzer to the data outputs of the EPROM and verify the contents of the LUT. Turn on the display of D15-D8 and check several locations such as EPROM address inputs 00, 10H, 20H, 63H and 64H. (Hint: trigger on the desired input bit pattern)

Part 2: Design using VHDL and Schematics

Circuit designs may be described as VHDL source files, schematics, test vectors or a combination of all of these. You designed a simple combinational circuit using VHDL earlier. The objective of this part of the lab is to practice with the schematic capture facility and to use it to implement a simple circuit that incorporates the comparator and a counter as components.

1. Program the 3032 with the 4-bit asynchronous counter and verify its operation. (use the logic analyzer to observe its state behaviour)

2. Add the NAND gate as shown in Figure 1 to detect the binary output 1XX1 from the counter to provide a reset signal. What is the state behaviour of this circuit ? (use the logic analyzer to observe)

3. Replace the counter in the circuit with the synchronous counter. How does the state behaviour compare to that in part 2 above ? (use the logic analyzer to observe)

4. Program the 3032 with the circuit in Figure 2 (using the synchronous counter) and your comparator that you stored as a symbol at the beginning of this lab. After compiling and programming the 3032 device, observe the operation of this circuit on the logic analyzer and note where the terminal count pulse appears for various values set on the toggle switches.

5. Modify the circuit in part 4 by connecting the terminal count output to the clear input of the counter and show that you now have a mod-(N+1) counter where N is the 4-bit binary number set on the toggle switches. Explain the operation for the case N=0.
Figure 1:

Figure 2