

4DM4 - Computer Architecture

September – December, 2009

Lectures: Mon, Thursday : 12:30 – 1:20, BSB-136
 Tuesday : 1:30 – 2:20, BSB-136
Tutorials : Tuesday 12:30 - 1:20, JHE-326H
Labs: Wed, Thurs - 2:30 - 5:20, ITB-157
Prof's Office Hours: To be Announced.

Instructor:

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(All emails to the Prof should begin with 4DM4 in the subject to be recognized as valid by spam filtering programs)

Teaching Assistants (Tentative):

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Web Site:

<http://mail.ece.mcmaster.ca/faculty/teds/COURSES>

Course Objective: Upon completion of this 4DM4 course, you should have considerable expertise in the topics on computer architecture listed below. You should have a thorough understanding of pipelined superscalar microprocessors, including the Intel and AMD IA-32 Pentium architectures, the Intel/HP IA-64 Itanium architectures, and the ARM microprocessor HDL ‘core’. You should have thorough expertise on the development of pipelined microprocessor “cores” in the VHDL hardware description language. You will be well prepared for a career in which you will likely encounter microprocessors and HDL cores on a regular basis. You will also have a solid basis for a continuation of your studies in graduate school if you chose this option.

Audience: Computer Architecture 4DM4 is a senior level course suitable for students with previous exposure to computer architecture and digital systems.

TextBook: "*Computer Organization and Design, The Hardware/Software Interface*", Fourth Edition, David Patterson and John Hennessy, Elsevier Publishers (Morgan-Kaufmann), 2009, ISBN 978-0-12-374493-7 (paperback)

The same authors have a graduate level textbook, which is an excellent reference of the same material but in more depth. Copies of this reference book will be made available in the library.

Reference Textbook: "*Computer Architecture: A Quantitative Approach*", Third Edition, 2002, David Patterson and John Hennessy, Morgan-Kaufmann, 2002, ISBN 1-55860-596-7.

The textbooks by Patterson and Hennessey are considered to be among the most comprehensive books on computer architecture available today. I chose the new book for a few reasons: (1) it is relatively new (3-td

edition published in 2005, 40-th edition published in 2009) and covers the Intel IA-32 Pentium and IA-64 Itanium architectures, (2) it supports both hardware and software streams, and (3) it includes a CD with additional reference materials, including a Verilog-HDL microprocessor “core”. This book is also used in COE-3DJ4 and 3DR4 in past years. These courses did not venture too much into the more complex material in chapters 6 and 7, such as pipelining, advanced pipelining and memory hierarchies and caching.

The textbook supports 2 streams, the software and hardware streams. 4DM4 will follow the hardware stream, focusing most of our time on the last few chapters (Ch. 6, 7). My 4DM4 notes will have additional material on ‘Advanced Pipelining and Parallelism’, taken from the reference textbook above. My 4DM4 notes will be made available electronically on the web. The tentative course outline follows:

<u>Outline of Topics:</u>	(weight)
Fundamentals of VHDL (VHDL constructs, RISC CPU in VHDL)	1 week
Ch. 1. Fundamentals of Computer Design (performance trends, silicon VLSI)	very brief review
Ch. 2. Instruction Set Principles (focusing on the hardware side)	very brief review
Ch. 4. CPU Performance Analysis (Amdahl’s law, SPEC benchmarks)	brief review
Ch. 5. Unpipelined Processor Architecture (multi-cycle operation)	brief review
Ch. 6A Basic Pipelining (pipelining, hazards, stalls, forwarding branch delays, branch prediction, exceptions, hardware structures, VHDL cache unit, IF unit, ID unit)	thorough coverage, 3 weeks
Ch. 6B Advanced Pipelining (multiple issue, Superscalar, EPIC/VLIW, Intel IA-32 Pentium, IA-64 Itanium, dynamic scheduling, Tomasulo’s algorithm, VHDL ID unit)	thorough coverage, 3 weeks
Ch. 7. Memory Hierarchy (caches, cache performance, Virtual Memory, paging, address translation VHDL, various cache designs)	thorough coverage, 3 weeks
Ch. 8. Storage Systems (RAID disk architecture)	brief review, time permitting

Tentative Marking Scheme:

Assignments (approx. 4 or 5)	approx. 10 %
Laboratories (approx. 5)	approx. 15 %

'2 pop quizzes	approx. 5 %	(at instructor's discretion)
1 Scheduled Midterm Test	approx. 20 %	
1 Final Exam	approx. 50 %	

Weights may be shifted by $\pm 10\%$ between the above components to reflect the work involved, at the instructor's discretion.

To achieve an A+ in this course, a student must achieve an A+ in the exam and midterm.

To pass this course, a student must pass the final exam.

Pop Quizzes: The "pop" quizzes are unscheduled, and may be given on 2 surprise days at the instructor's discretion. The purpose of these quizzes is that the marks reflect class attendance and ability to follow material, so please plan to attend most lectures. These marks are firm: if you miss a pop quiz, your grade will count unless there is a medical note.

Laboratories: The laboratories will involve the design of a pipelined microprocessor "core" in the VHDL hardware description language. All students should have previous exposure to VHDL in the 3rd year 3DQ4 Digital Systems Design course.

Feedback to the Instructor: The prof wants to make this course as exciting as possible for you. The lectures and labs have been carefully prepared and we will try to present a lot of examples in class. If you have feedback for the prof, please drop by during office hours or right after the class and let us know.

Other Resources:

VHDL: You can obtain a student edition of the Altera MAX+Plus II CAD software at this web-site:

<http://www.altera.com/support/licensing/lic-university.html>

"Getting Started" Manual for Altera's MAX+Plus II system is available at:

<http://www.altera.com/support/software/sof-maxplus2.html>

Altera Application Notes: Available at

<http://www.altera.com/literature/lit-an.html>

Calculator requirement for tests and examinations: *the McMaster Standard Calculator (Casio fx991)*

Policy Reminders: *(include the following on all course outlines)*

Senate and the Faculty of Engineering require all course outlines to include the following reminders:

"The Faculty of Engineering is concerned with ensuring an environment that is free of all adverse discrimination. If there is a problem, that cannot be resolved by discussion among the persons concerned, individuals are reminded that they should contact the Department Chair, the Sexual Harassment Officer or the Human Rights Consultant, as soon as possible."

“Students are reminded that they should read and comply with the Statement on Academic Ethics and the Senate Resolutions on Academic Dishonesty as found in the Senate Policy Statements distributed at registration and available in the Senate Office.”

"Academic dishonesty consists of misrepresentation by deception or by other fraudulent means and can result in serious consequences, e.g. the grade of zero on an assignment, loss of credit with a notation on the transcript (notation reads: "Grade of F assigned for academic dishonesty"), and/or suspension or expulsion from the university. It is your responsibility to understand what constitutes academic dishonesty. For information on the various kinds of academic dishonesty please refer to the Academic Integrity Policy, specifically Appendix 3, located at http://www.mcmaster.ca/senate/academic/ac_integrity.htm

The following illustrates only three forms of academic dishonesty:

- 1 Plagiarism, e.g. the submission of work that is not one's own or for which other credit has been obtained. (*Insert specific course information, e.g. style guide*)
- 2 Improper collaboration in group work. (*Insert specific course information*)
- 3 Copying or using unauthorized aids in tests and examinations.

(If applicable) In this course we will be using a software package designed to reveal plagiarism. Students will be required to submit their work electronically and in hard copy so that it can be checked for academic dishonesty."