LOW POWER HIGH SPEED I/O INTERFACES IN 0.18um CMOS

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ABSTRACT

The design and implementation of a low power high speed differential signaling input/output (I/O) interface in 0.18um CMOS technology is presented. The motivations for smaller signal swings in transmission are discussed. The prototype chip supports 4 Gbps data rate with less than 10mA current at 1.8V supply according to Cadence Spectre post-layout simulations. Performance comparisons between the proposed device and other signaling technologies reported recently are given.

1. INTRODUCTION

Recent developments in high speed serial I/O are pushing the off-chip data rate into multi-Gbps range on a single pin/wire [1],[2]. Along with the increasing data rate, other major concerns of high performance I/Os are reductions in circuit power and chip area, which enable very high levels of silicon integration [3].

Currently, popular approaches in high performance transmission include signaling with the incident wave from the transmitter rather than ringing up the line [2][3][4]. To achieve incident-wave signaling, the high speed I/O circuits drive a point-to-point interconnect over a terminated transmission line while the receiver termination absorbs the incident wave preventing any reflection [4]. To assure signal quality which is prone to deteriorate by process conditions, differential signaling is often used to reject common mode noise, to minimize electro magnetic interference (EMI), and to double the slew rate [3]. *Boni* describes a differential positive emitter coupled logic (PECL) - I/O interface in 0.35um CMOS technique tested up to 1.2 Gb/s [5].

A more effective solution to multi-giga-bit transmission is low voltage swing signaling which possesses significant advantages such as faster data rate and better energy efficiency by means of reducing signal swing on the wire, ie see [6] which applies to on-chip signaling. Low Voltage Differential Signaling (LVDS) [7] supports data rate up to 2 Gbps in asynchronous mode transmission using 0.35um CMOS [8] and up to 2.5 Gbps on 0.25um CMOS technique [9]. However, it should be noted that LVDS standards (*ANSI/TIA/EIA-644-A*) define stringent specifications on signal swings and signal levels. For off-chip I/O, the LVDS standards define the swing and common mode voltage as [7]:

$$250mV \leq V_{OD} \leq 450mV \qquad (1)$$

$$1.125V \leq V_{CM} \leq 1.375V \qquad (2)$$

Where V_{OD} and V_{CM} are the differential output voltage and common-mode voltage of transmitter output, respectively.

This paper presents the design and implementation of a pair of low power high speed I/O interfaces using 0.18 um CMOS. By decreasing input/output voltage swings from the LVDS standard ranges in Equ. (1) to 80mV as well as optimizing circuit designs, an I/O interface is achieved which supports transmission at data rates up to 4 Gbps and exhibits average currents of 2.87mA on the transmitter and 6.9mA on the receiver using a 1.8V supply according to Cadence Spectre simulations. The silicon area of a transceiver I/O pad is approximate 0.011 mm^2. A comparison with other I/O schemes is also provided.

2. TRANSMITTER

2.1. Circuits

Typical differential mode signals may be driven by either switched-voltage sources or switched-current sources [5]. The differential signals flow through transmission line pairs to receiver terminals. In the current-driving mode, the transmitter output stage drives a differential signal current into a terminated line and an output voltage swing level appears across a termination resistor which provides optimum line matching [8]. The proposed transmitter works in current driving mode with lower output swing levels. Fig.1 shows the functional blocks of an LVDS transmitter. The phase splitter is implemented to acquire differential signals with 180° phase shift from a single-ended input. The differential output currents are provided by the switch current unit. A bias voltage from a reference unit controls process, supply, temperature (PVT) variations.
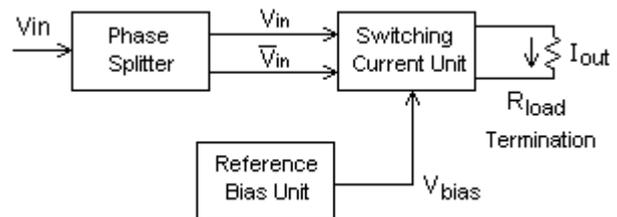
Figure 1. Function block diagram of an LVDS transmitter [8]

The schematic of the proposed switching current unit is shown in Fig. 2, which is modified from [8]. The switched output current flows across a load resistance R_{load} establishing a correct differential voltage swing which would be sensed by the receiver. In Fig. 2, the unit includes two sub-circuits: the current bridge (left) and voltage feedback control (right).
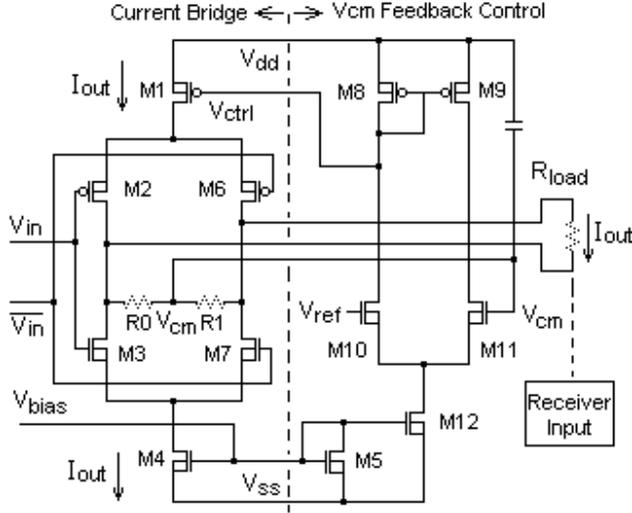
Figure 2. Schematic of switching current unit in transmitter

In Fig. 2, CMOS transistors M_2, M_3, M_6, and M_7 are configured in a full bridge differential arrangement whose working current is supplied by current source M_1 and current sink M_4. According to differential input signals $V_{in}/\overline{V}_{in}$ from the phase splitter unit in Fig. 1, M_2/M_7 and M_3/M_6 are switched on or off together to generate two different current paths from M_1 down to M_4. These two current paths affect the polarity of the current I_{out} on the termination resistor R_{load}.

To achieve higher control of the output current and to reduce the transistor count, the feedback control used in [8] was replaced by the circuit shown on the right side of Fig. 2. V_{cm} is determined over a high resistance voltage divider R_0 and R_1 (10k ohms) between two inner bridge nodes, and compared with a reference V_{ref}. Depending on difference $(V_{cm}-V_{ref})$, the differential amplifier (M_8, M_9, M_{10}, M_{11}) adjusts the control signal V_{ctrl} to affect the supply current of the current bridge from M_1 to minimize the difference between V_{cm} and V_{ref}.

2.2. Average power analysis

For the power dissipation of I/O interface, what we care about mainly is its average power, which is consumed in 3 parts: transmitter, terminal / interconnect, and receiver. For a conventional transmitter based on Fig. 1, the majority of the power benefit is consumed by the switching current unit, while the power in phase splitter unit and reference bias unit are rarely affected by output swing changes and can be designed around 1mW.

To demonstrate theoretically the average static power variety of transmitter in different output swings, let's consider the schematics of switching current unit in Fig. 2,

where the power consumption is mainly from current bridge as shown on left side of Fig. 2, because the feedback control unit can be designed with minimal power (< 0.5mW).

2.2.1. 250mV swing

When the output voltage swing on the load resistance R (termination resistor, *100* ohms) is an *250* mV square wave, the corresponding current on resistor, I_{out}, is:

$$I_{out} = \frac{V_{swing}}{R} = \frac{250mV}{100\Omega} = 2.5mA \qquad (3)$$

Known from the current path (M_1 down to M_4) of Fig. 2, the load current I_{out} is the working current of the bridge, which flows between drain and source node of M_1 and M_4. The average power of current bridge P_{brdg}, and of termination resistor P_R can be approximately written as:

$$P_{brdg} = V_{dd} \times I_{out} = 1.8 \times 2.5 = 4.5mW \qquad (4)$$

$$P_R = I_{out}^2 \times R = 2.5^2 \times 100 = 0.625mW \qquad (5)$$

Therefore, the power of the switching current unit in transmitter (assuming the power designed in feedback control part, *0.5*mW), *P*, is:

$$P \approx 4.5 + 0.625 + 0.5 = 5.625mW \qquad (6)$$

The total power consumption of transmitter in 250mV swing can be approximated by considering the average power of phase splitter unit and reference bias unit in Fig. 1 (1.5mW) as:

$$P_{250mV} \approx 5.625 + 1.5 = 7.125mW \qquad (7)$$

Note that, the use of a larger CMOS technology (i.e. 0.25um CMOS) or higher supply voltage (ie. V_{dd} = 2.5V) will only increase the power consumption.

2.2.2. 80mV swing

In the proposed transmitter circuits the output differential swing is reduced to 80mV and common mode voltage is reduced to 350mV. Therefore, the corresponding output current over load resistor, I_{out} is:

$$I_{out} = \frac{V_{swing}}{R} = \frac{80mV}{100\Omega} = 0.8mA \qquad (8)$$

The average power consumption of current bridge P_{brdg} and termination resistor P_R are approximately:

$$P_{brdg} = V_{dd} \times I_{out} = 1.8 \times 0.8 = 1.44mW \qquad (9)$$

$$P_R = I_{out}^2 \times R = 0.8^2 \times 100 = 0.064mW \qquad (10)$$

The total power of switching current unit of proposed transmitter (including the power designed in feedback control part, *0.5*mW) is:

$$P \approx 1.44 + 0.064 + 0.5 = 2.0mW \qquad (11)$$

For total power consumption of transmitter with 80mV output swing, considering the average power of designed phase splitter unit and reference bias unit in Fig. 1 (*1.5*mW), the approximate value is:

$$P_{80mV} \approx 2.0 + 1.5 = 3.5mW \qquad (12)$$

From above static power analysis results, Equ. (7) and (12), the change in output swing from 250mV to 80mV reduces the transmitter power by approximately a factor of 2.

To simplify the analysis, the power benefit of interconnect from smaller swings is ignored here. For the power benefits of smaller swings (80mV) in receiver, the proposed receiver designs can support different swings with almost same output response, or in other words, no other extra amplifiers needed in receiver to restore smaller swing to its normal value. Therefore there is no significant difference between power consumptions of receiver while I/O interface swings at 250mV or 80mV level.

3. RECEIVER

In the proposed receiver, the differential current signals are converted into corresponding voltage swings over a termination resistor. The voltage swing level is reduced to 80mV. To detect these low voltage signals, the receiver sensitivity/gain is critical. Additionally, a wide range of common mode voltage should be admissible to maintain a large dynamic response in the receiver.

Fig. 4 shows a 3-stage serially linked amplifier structure in the receiver, modified from [9] to create a single-ended (non-differential) signal output at the end. Fig.5 shows the schematics of the proposed circuit stages.
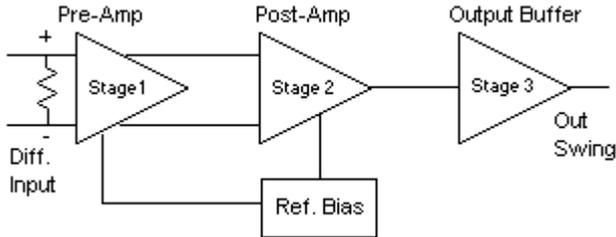
Figure 4. Structure of receiver circuits
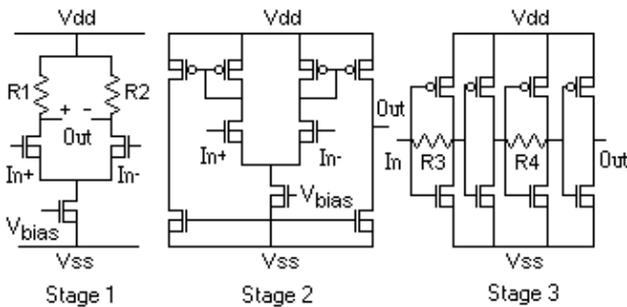
Figure 5. Schematics of receiver circuits

To ensure a sufficient voltage gain in the receiver when common mode voltage is very low, a rail-to-rail pre-amplifier (Stage 1 shown in Fig. 5) from [11] was used. The load resistors of the pre-amplifier, R_1 and R_2, are optimized for the required voltage gain, and to produce the correct common-mode voltage for following amplifier stage.

Since the input swing to the receiver is a voltage signal and the output concerned is current drive ability, an operational transconductance amplifier (OTA) is used in the second stage amplifier of the receiver. The advantage of OTA is that circuit transconductance can be adjusted and kept optimized by bias current [11]. Therefore the reference circuit is carefully designed (not shown in Fig. 5) to supply ideal bias voltage to the current source of the OTA amplifier.

In the final stage, a 4-level inverter chain works as an output buffer amplifier for gain adjustment. The inverter in the chain detects signal output from stage 2 (OTA), and works as a linear amplifier to meet the gain requirement. Feedback resistors R_3 and R_4 are attached between the input and output nodes of first and third inverters to reduce waveform clipping in high-speed operation, at the expense of voltage gain [9].

With optimized parameters, the proposed receiver performs satisfactorily at 2 GHz (equivalent to 4 Gbps) sine-wave input with differential input swings at 80mV, receiver output is 994mV, the average working current is 6.9mA according to Cadence Spectre simulations, while receiver silicon area in prototype chip is approximate 0.004 mm^2.

4. EXPERIMENTAL RESULTS

The transmitter and receiver circuits of proposed low power I/O interface are integrated in a prototype chip being fabricated by Canada Microelectronic Corporation (CMC) in TSMC 0.18um 1P6M CMOS technology. The real silicon area of circuits in chip is approximate 0.011 mm^2. Fig. 6 shows the layout diagram of the prototype chip.
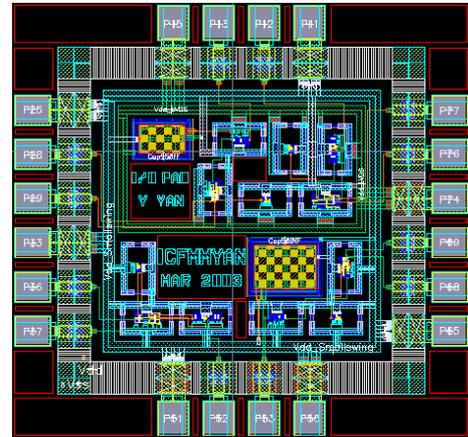
Figure 6. Layout diagram of test chip

The post-layout simulations by Cadence Spectre of test chip confirm the reasonability of new I/O circuit designs and high performance on data rate and power consumption. When input frequency is 2 GHz (4 Gbps), temperature is 27℃ and power supply is 1.8V, the response waveforms of proposed transmitter and receiver are shown in Fig. 7 and Fig. 8, respectively. The LRC models of bond wire, pad and chip package (CMC 80-pin CFP80) are included in simulations as well as ESD protections. The simulation of transmitter output is based on a pair of 100cm-long, 50ohms characteristic resistance

PCB traces and 100 ohms termination resistor.
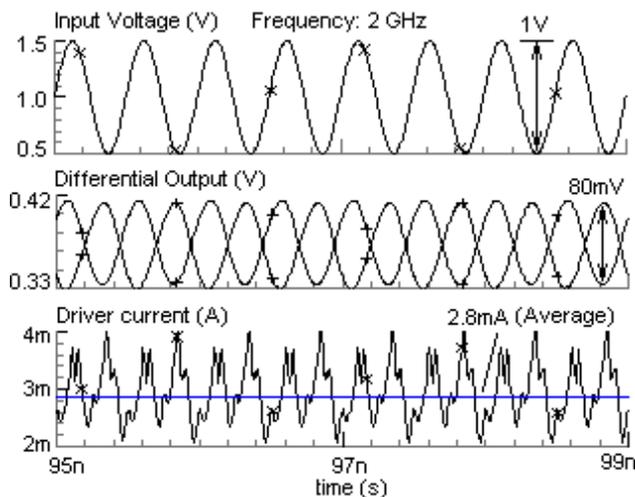
Figure 7. Post-layout simulation of transmitter by Cadence Spectre
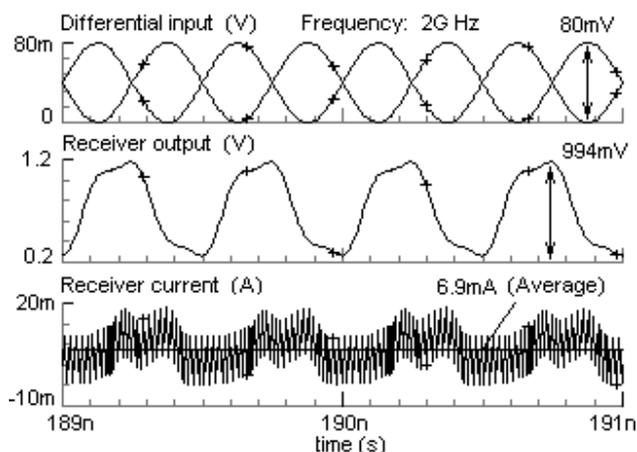
Figure 8. Post-layout simulation of receiver by Cadence Spectre

Table 1 summarizes the performance comparisons on data rate and power consumption between the proposed I/O interface and other signaling methods in recent reports

Chips	Swing (mV)	Power(mW)/current(mA)		Data rate (Gbps)	CMOS (um)
		Transmitter	Receiver		
Designed here	80	5.16 (2.8)	12.4 (6.9)	4	0.18
Designed here	250	13.3 (7.4)	15.6 (8.7)	4	0.18
Jamasb,[12]	212	23 (12.5)	---	1.2	0.18
Velio Co.[10]	Program.	1900 (VC1003)*		3.125	0.18
Dally[3]	100	20 (--)	18 (--)	4	0.25
LVDS[9]	100-400	50 (20)	51 (20.4)	2.5	0.25
Boni PECL[5]	930	115 (35)	23 (7)	1.2	0.35
Boni LVDS[8]	250	43 (13)	33 (10)	2	0.35

Table 1. Comparisons of present I/O chip technology
*: VC1003 transceiver, 8 lanes, 238mW per lane.

5. SUMMARY

In summary, a low power high speed I/O interface has been designed and the prototype chip is being fabricated in TSMC 0.18um 1P6M CMOS technology. By reducing signal voltage swings, the transceiver can achieve high data rates up to 4 Gbps in I/O interface with power consumption of 17.56mW (sum of transmitter and receiver).

The proposed transmitter utilizes a modified closed loop switching current circuit to maintain reliable signal current levels and controlled common-mode voltage levels with a reduced output swing. The receiver uses dual-gain amplifiers and out-buffer with feedback to achieve optimized gain performance for low differential input swing, while reducing power consumption.

The post-layout simulation results not only demonstrate the feasibility of smaller swings in I/O devices, but show significant improvements on performance of data rate and power consumption, due to low voltage swings.

6. ACKNOWLEDGMENTS

7. REFERENCE

[1] W. J. Dally and J. Poulton, "Transmitter Equalized 4Gbps CMOS Signaling," *IEEE Micro,* pp.48-56, Jan. – Feb. 1997.

[2] H. Wilson *et al.*, "A Six-Port 30-Gb/s Nonblocking Router Component Using Point-to-Point Simultaneous Bidirectional Signaling for High-bandwidth Interconnect" *IEEE Journal of Solid-State Circuits*, Vol.36, No.12, pp. 1954-1963 Dec. 2001

[3] M. J. E. Lee, W. J. Dall*y,* and P. Chiang, "Low-Power Area-Efficient High-Speed I/O Circuit Technique". *IEEE Journal of Solid-State Circuits*, Vol. 35, No.11, pp. 1591-1599, Nov. 2000

[4] W. J. Dally, *et al.*, "High-Performance Electrical Signaling", *Massively Parallel Processing, 1998. Proceedings. Fifth International Conference on*, pp. 11–16, 1998

[5] A. Boni,. **"**1.2-Gb/s true PECL 100K compatible I/O interface in 0.35 um CMOS" *Solid-State Circuits, IEEE Journal of*, Vol. 36 Issue: 6, pp. 979 – 987, June 2001

[6] H. Zhang,, V. George, J.M. Rabaey, " Low-swing on-chip signaling techniques: effectiveness and robustness" *Very Large Scale Integration (VLSI) Systems, IEEE Transactions on*, Vol. 8 Issue: 3, pp. 264 – 272, June 2000

[7] ANSI/TIA/EIA-644-A LVDS Standards

[8] A. Boni, A. Pierazzi, D. Vecchi, "LVDS I/O interface for Gb/s-per-pin operation in 0.35-um CMOS" *Solid-State Circuits, IEEE Journal of*, Vol. 36 Issue: 4, pp. 706 –711, April 2001

[9] J. Lee *et al.*, "Design and implementation of CMOS LVDS 2.5 Gb/s transmitter and 1.3 Gbps receiver for optical interconnections" *Circuits and Systems, 2001. The 2001 IEEE International Symposium on,* Vol. 4, pp. 702 -705, 2001

[10] VC1003, 2.72-3.125 Gbps Eight-Lane CMOS Serializer / Deserializer, *Product Summary, Velio,* Mar 13, 2002

[11] R. J. Baker, H. W. Li *et al.*, *CMOS Circuit Design, Layout and simulation*, IEEE, Inc., New York, 1998

[12] S. Jamasb, *et al.*, "A 622MHz stand-alone LVDS transmitter pad in 0.18um CMOS" *MWSCAS 2001. Proceedings of the 44th IEEE 2001 Midwest Symposium on Circuits and Systems*, Vol. 2, pp: 610 – 613, 2001