Performance of a 12GHz Monolithic Microwave Distributed Oscillator in 1.2V 0.18µm CMOS with a New Simple Design Technique for Frequency Changing

Kalyan Bhattacharyya and Ted H. Szymanski

Dept. of Electrical & Computer Engineering, McMaster University, Hamilton, ON, Canada L8S 4K1

Abstract **—** A monolithic distributed oscillator (DO) is designed and fabricated using an n-FET-based Traveling Wave Amplifier (TWA) [1], but with coplanar waveguides (CPW) and a proposed coplanar structure called a 'folded CPW'. Experimental measurements are reported for the first time using a standard 0.18µm CMOS technology, with a bias of 1.8V. The oscillator operates at 12.0GHz with 5.77dbm gain as shown in Fig. 2 and will be called as OSC-1. The measured phase noise is –115dBc/Hz at 1MHz offset. The signal power in the harmonics is very low, -34dBm in the 2nd harmonic. The frequency of oscillation can be increased for this oscillator by 170MHz by varying the dc bias. The reported power includes a 2.6dB loss associated with the measurement system.

The 'folded CPW' of Fig. 3 is proposed, fabricated and measured with a probing system and vector network analyzer with S-G (signal-ground) probes for signal-ground pads, rather than the G-S-G probes used for measurements as in [2], [3]. The measured loss S_{21} (dB) versus frequency of the coplanar test structure of Fig. 3 is shown in Fig. 4 before pad de-embedding, with 1.259dB loss at 10GHz. Measurements of 'folded CPW' is de-embedded for the pads with the previously measured s-parameter data of ground-signal-ground pads, which won't be very different as the substrate is similarly grounded. This test structure exhibits 0.8dB loss at 10GHz after pad de-embedding. For previously characterized coplanar waveguides reported in [2], [3], the measured loss was 0.64dB/mm at 10GHz for straight design. The CPW in [2], [3] did not have a 180 degree bend. The proposed 'folded CPW' would have only 0.67dB/mm loss at 10GHz if bends were removed [2], [3]. By adopting two 45 degree bends in the test structure, the extra loss is only 0.13dB. From the loss point of view, two 45 degree bends are preferable to arbitrary angle bends such as 30 or 60 degrees, which give more reflection losses. All angle bends necessarily incur losses and may need non-standard fabrication process. The measured spectrum of the input and output reflections S_{11}(dB) and S_{22}(dB) before pad deembedding are S_{11}= -24.6dB and S_{22}= -24dB at 12GHz.

The amplitude of the DO of Fig. 1 (without C_c) has fallen significantly at the lower bias of 1.2V. A design modification is proposed by incorporating C_c in the feedback path (Fig. 1), similar to [4], to overcome this drop of amplitude and simulated results are reported. This design is simulated in ADS Harmonic Balance simulator with TSMC n-FET model of 0.18µm technology. The DO of Fig. 1 is now has the capacitor C_c for ac coupling while retaining the independent control of dc voltage in gate and drain lines. By increasing the drain voltage by 0.2V from 1.8V while keeping gate voltage constant at 1.2V, the frequency is increased by 60MHz with a 1dBm increase in output power. By decreasing the gate voltage by 0.2V while keeping the drain voltage constant at 1.8V, the frequency is increased by 60MHz with a 1.3dBm decrease in output power. We observe that this incorporation of C_c results in a high oscillation frequency with VCO-like operation.

An optimized four stage DO design using n-FET cascode in gain cells is proposed, similar to that we reported first in [3] with five stages and will be mentioned as OSC-2 shown in Fig. 5. The measured results of the five stage oscillator of Fig. 1 (without C_c) is compared with simulated results of this four stage DO having C_c incorporated from the beginning. This OSC-2 uses n-FET of 50µm width in n-FET cascode cells. ADS simulations indicate a frequency increase of 230MHz from a fundamental of 12.67GHz with less than 2dBm change in output power (from a base power of 3dBm) by increasing the drain voltage by 0.2V from 1.8V while keeping gate voltage constant at 1.2V. However, the ADS simulator underestimates the loss of the CPWs, so that fabricated oscillators will exhibit somewhat lower frequencies than simulations.

We now propose a new simple design technique to change the oscillation frequency. Previous TWAs have used inductive elements of values L between gain stages and L/2 at the beginning and end-ports. This trend has been valid for 20 years, since it was first reported in [3].

Values of Inductive Termination	OSC-2 Freq: (GHz)	Values of Inductive Termination	OSC-2 Freq: (GHz)
L_{D1}=3L/2	12.05	L_{D2}=3L/2	11.0
L_{D1}=L	12.35	L_{D2}=L	11.75
L_{G1}=3L/2	11.0	L_{G2}=3L/2	12.63
L_{G1}=L	11.75	L_{G2}=L	12.42
L_{D1}=L_{G1}=3L/2	10.55	L_{D2}=L_{G2}=3L/2	11.0
L_{D1} =L_{G1}=L	11.75	L_{D2}=L_{G2}=L	11.75

We explore the use of L values from L/2 to 3L/2 (maximum) for using before or after the gain stages in drain and gate transmission lines (please see Fig. 5) formed by coplanar waveguides [3]. For changing the $L_{D1/2}$ and $L_{G1/2}$ up to 3L/2 from L/2 in steps of L/2, the simulated results are reported in the table above for the OSC-2 (otherwise the values are L/2). The table above showing 2.12GHz frequency variation in same design for

the optimized four stage n-FET cascode cell oscillator (Fig. 5).

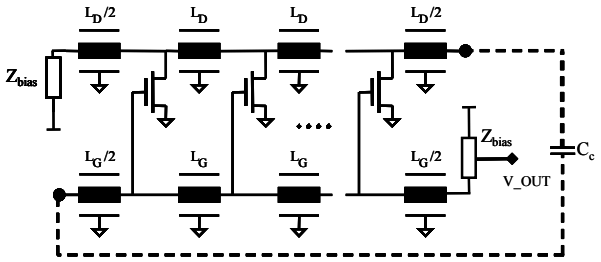

Fig. 1. Schematic of the distributed oscillator with coupling capacitor C_c incorporated in simulation after measurements.

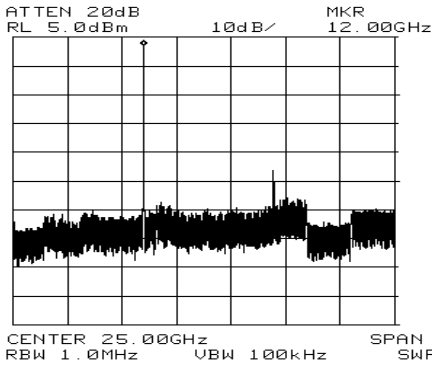

Fig. 2. Measured power spectrum of the Osc-1 with marker showing that the fundamental is at 12.00GHz, +5.77dBm (after adding the loss of 2.6dB).

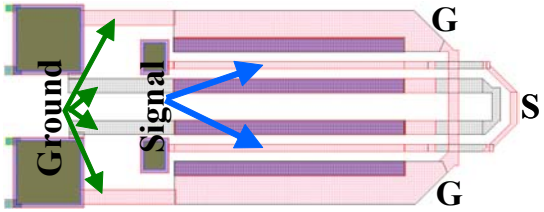

Fig. 3. Layout of the coplanar test structure (top view) used in the bend path of the gate line.

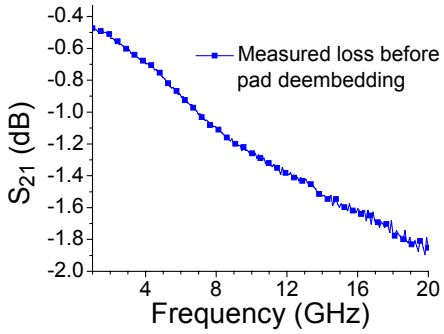

Fig. 4. Measured loss S_{21} (dB) versus frequency of the coplanar test structure of Fig. 3.

The measured phase noise of the DO of Fig. 1 (without C_c) is compared with previously published work on silicon distributed oscillators [1], [4] showing (Fig. 6) this work has the best phase noise figure. The normalized carrier-to-noise ratio (which is also Figure of Merit) has been calculated according to [6] is 176.25dBc/Hz.

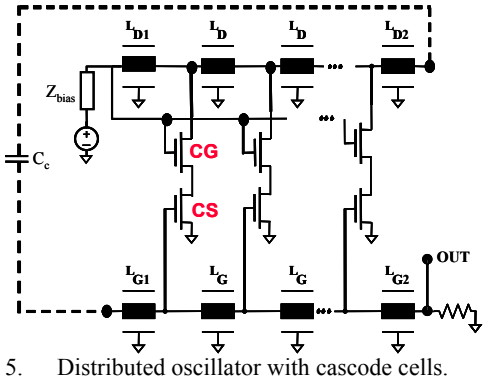

Fig. 5. Distributed oscillator with cascode cells.

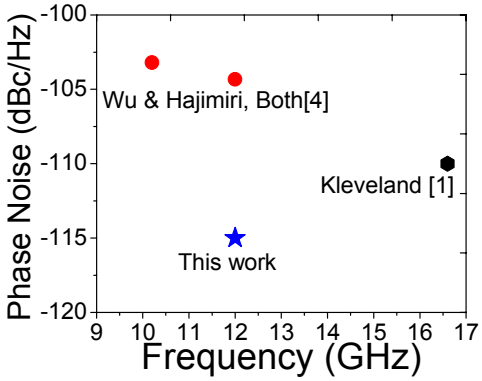

Fig. 6 Comparison of measured phase noise figures.

REFERENCES

[1] B. Kleveland, "CMOS interconnects beyond 10 GHz," *PhD thesis*, Stanford University, August 2000.

[2] Kalyan Bhattacharyya and M. Jamal Deen, "Microwave CMOS traveling wave amplifiers – performance and temperature effects," *IEEE Microwave and Wireless Components Letters*, vol. 14, No. 1, pp. 16-18, January 2004.

[3] Kalyan Bhattacharyya and Ted Szymanski, "1.2V CMOS 1-10GHz Traveling Wave Amplifiers Using Coplanar Waveguides as On-Chip Inductors," *IEEE Radio and Wireless Conference (RAWCON)*, Atlanta, Georgia, USA, pp. 219-222, September 19-22, 2004.

[4] H. Wu and A. Hajimiri, "Silicon-Based Voltage-Controlled Oscillators," *IEEE Journal of Solid-State Circuits*, vol. 36, No. 3, pp. 493-502, March 2001.

[5] James.B.Beyer et al, "MESFET distributed amplifier design guidelines," *IEEE Transactions on Microwave Theory and Technique*, vol. MTT-32, No 3, pp 268-275, March 1984.

[6] A. Leelasantitham and B. Srisuchinwong, "A low-power, high-frequency, all-NMOS all-current-mirror sinusoidal quadrature oscillator,"*Microelectronics Journal,* Vol. 35, Issue. 9, September 2004.