Abstract. A Field Programmable Gate Array (FPGA) with optical I/O is described. FPGAs with optical I/O can have their functionality specified in the field by downloading a control bit stream, and can be used in a wide range of applications, such as optical signal processing and optical interconnects. Our device implements six state-of-the-art Programmable Logic Arrays (PLAs) on a 2x2 mm die. The device was fabricated through the 1997 Lucent/ARPA/COOP workshop using a 0.5 micron CMOS/SEED technology. All devices are fully functional, and the electronic datapaths have been verified at 200 Mhz. The device has been programmed to implement a 2-stage optical switching network with six 4x4 crossbar switches, which can realize over 190 million unique programmable input-output permutations. The same 0.5 micron device scaled to a 1 cm² substrate could support 4 thousand optical I/O, 1 Terabit/sec of optical I/O bandwidth, and offer fully programmable digital functionality with \( \approx 110,000 \) programmable logic gates.

1. Introduction

Conventional electronic ICs have a limited electronic I/O bandwidth. In contrast, an FPGA with optical I/O \([1,2]\) can offer very high optical I/O bandwidths, ranging from 100s of Gigabits/sec to Terabits/sec. FPGAs with optical I/O can also eliminate the need for the custom design and fabrication of application-specific optoelectronic devices, just as FPGAs have largely eliminated the need for custom design and fabrication of application-specific VLSI integrated circuits, except in the most demanding applications.

A first-generation programmable logic device with integrated optical I/O was fabricated in the 1995 Lucent/ARPA/COOP workshop, and is described in \([1,2]\). It used multiple Look-Up Tables (LUTs) to implement the programmable logic on a 2x2 mm die. This device established the feasibility of field programmable integrated optoelectronic devices. This paper describes a second-generation device fabricated in the 1997 Lucent/ARPA/COOP workshop, and demonstrates "Moore's Law" of exponential gains in performance. Our latest device uses an array of state-of-the-art PLAs internally, uses tens of thousands of transistors, and requires approx. 1K bits of configuration. Our second generation design is very fast, highly functional and competitive to commercially available FPGAs. Some related research is described in \([3,4,5]\).

2. Architectural Model

Our FPGA consists of an array of "Finite State Machines" (FSMs) on a CMOS substrate. Each FSM has several electronic connections to neighboring FSM cells. Each FSM has several optical and electrical I/O, a combinational Programmable Logic Array (PLA), along with memory. Each FSM also has a global clock and reset inputs.

The core of the FSM is the PLA. The PLA consists of a logical AND array followed by a logical OR array, as shown in fig. 1a. The input signals enter from the lower left. The complemented and uncomplemented values of each input signal are fed into the AND array on the vertical lines. Every horizontal line in the AND array represents a "product" term, i.e., the logical AND of all the inputs connected to it through a closed connection (ie. bold dot). In the OR array, every vertical line represents a "sum" term, i.e., the logical OR of all product terms connected to it through a closed connection.
Conventional PLAs are not dynamically programmable [6]. To make these PLA structures dynamically programmable, a "programmable connection" must be inserted at each intersection of a horizontal and vertical line. Each programmable connection has 2 states, "opened" and "closed", and can be controlled by one bit of control memory. Such PLAs are used in commercial devices such as the Altera 7000 Family of programmable logic devices, and are often called "Complex Programmable Logic Devices" (CPLDs) in the literature. Hence, our device can also be called a CPLD with optical I/O.

Each of our FSMs contains up to 4 electrical or optical inputs, up to 4 electrical or optical outputs, and 1 Flip-Flop, i.e., our PLAs have 5 inputs, 6 outputs and 10 product terms as shown in fig. 1a. Each PLA requires $10 \times 10 = 100$ programmable connections in the AND array, and $10 \times 6 = 60$ programmable connections in the OR array, for a total of 160 programmable connections. Each programmable connection uses a dense 6 transistor Static RAM cell. Each FSM buffers its inputs, outputs and product terms, for a total of 21 additional DFFs.

The programmability of our devices is computed as follows. Each horizontal line in the AND array can realize a 5 input AND gate with up to 5 inverters. Each vertical line in the OR array can realize a 10 input OR gate. FPGA complexity is usually expressed in terms of equivalent binary (two input) logic gates. Each AND array product term is equivalent to $\approx 6$ binary AND gates, and each OR array sum term $\approx 9$ binary OR gates. Therefore, each PLA offers $\approx 114$ programmable binary logic gates. Each PLA uses 160 bits of configuration memory, for an average of about 1.4 bits of control memory per programmable gate. Our entire chip supports 6 FSMs, and requires 960 bits of control memory.

3. VLSI Design

The device was fabricated on a 2x2 mm die using a 0.5 micron CMOS process, shown in fig. 1b. Each PLA requires approx. $300 \times 400$ microns. The die also contains some custom smart pixels for an intelligent optical backplane under development in Canada, which will be described elsewhere.

Four differential optical receivers provided by Lucent technology [7] were implemented on the chip, including the BL_trnew3_packb, BL_trnew3_packa, BL_rc5g, and BL_trnew3_packc receiver standard cells. The electronic outputs of the chip used the buffered output pads from the Tanner Research standard cell library. According to our SPICE simulations, these electronic pads are rated at 80/60/30 MHz clock rates with 20/40/80 pF capacitive loads respectively. The devices were packaged in the standard Kyocera 84-pin PGA packages used by the workshop. The electronic output pads have limited clock rates, whereas the optical I/O have very high clock rates. Hence, the optical I/O bandwidth of the device will be considerably larger than the electrical I/O bandwidth.
4. Electrical Testing

We have completed the electrical testing. An Altera 81500 FPGA connected to an IBM PC was used to program our device. Each test configuration requires specifying and downloading all 960 control bits. We have programmed the device to implement several different logic functions. Each programmable connection in the device was tested, and verified with 100% functionality.

In our most complex test, the device was programmed to implement a 12x12 switching matrix. The switching matrix is similar to a 2-stage Banyan network built with 4x4 crossbar switches, and is also similar to the first 2 stages of a 3-stage radix 4 Clos network [8]. The network has 2 stages each with three 4x4 crossbar switches. Each crossbar can be programmed to realize 4! = 24 different programmable permutations, and the entire switching network can be programmed to realize (24)^6 = 190 million unique input-to-output permutations. The device can also be programmed to realize all multicasting and broadcasting patterns. This test was fully functional, with a 200 Mhz clock rate. This test illustrates the power of programmable optoelectronic logic devices, as they are competitive with custom designed optoelectronic devices [8].

The output waveforms from the oscilloscope are shown in Fig. 2b. The 200 Mhz clock has a small voltage swing (2v - 3v). One input rising edge is shown, followed by an output rising edge. A Hewlett Packard oscilloscope model HP 54610B, with two channels and with a 500 Mhz peak bandwidth, was used. We are currently testing the internal datapaths at 250 Mhz clock rates.

5. Extrapolation to a 1x1 cm Die Size

Each FSM requires about 300x400 microns. In a 1x1 cm die using 0.5 micron technology, we can fit ≈ 32x32 array of FSMs. Each FSM offers about 114 programmable gates, so this chip will offer a peak of ≈ 114,000 programmable logic gates. With an optical clock rate of 250 Mhz, the optical I/O bandwidth will be ≈ 1 Terabit per sec. The device could also use standardized optical I/O packaging and standardized electronic chip packaging mechanisms. Hence, such a chip could be used in a wide range of applications, and could eliminate the need for custom VLSI design of optoelectronic chips.

The use of programmable logic with VCSEL technology promises even higher optical I/O bandwidths and simpler optical packaging. Such devices could for example be used to realize ATM switching over optical...
backplanes, optical image processing, optical pattern matching and correlators, and various other complex optical digital logic processing tasks.

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7. References.


