MOSFET Modeling for Low Noise, RF Circuit Design

M. Jamal Deen and Chih-Hung Chen
Department of Electrical and Computer Engineering, McMaster University, Hamilton, ON, Canada

Yuhua Cheng
Conexant Systems, Newport Beach, CA 92660, USA

ABSTRACT
In this paper, high frequency (HF) AC and noise modeling of MOSFETs for low noise, radio frequency (RF) integrated circuit (IC) design are discussed. Scalable parasitic model and the Non-Quasi-Static (NQS) model are discussed and verified with the measured data. For the noise modeling, extracted noise sources of MOSFETs in 0.18 µm CMOS process and from RF noise measurements are presented. Finally, the design consideration including selection of device size, bias condition and design of the device geometry are discussed.

I. INTRODUCTION
In addition to the high level of integration offered by CMOS process for digital circuit design, MOSFETs have become attractive for RF applications due to the very high unity-gain frequencies of tens of GHz [1],[2]. However, one of the challenges for the MOSFET-based RF circuit design is the prediction of the RF performance of the devices with low power consumption. In addition, when working at high frequencies with low power consumption, the noise generated within the device itself will play an increasing important role in the overall system characteristics, especially for front-end receivers. Therefore understanding the RF and noise characteristics of MOSFETs is crucial for low noise, RF circuit designs.

In this paper, three main issues - AC modeling, noise modeling and design strategies for low noise RF circuits will be addressed. In the first part, we discuss the modeling of the parasitic components, and present a simple sub-circuit MOSFET model for RF applications. The model is accurate in y-parameters (up to the ½ fT frequency range) for RF ICs. In addition, the non-quasi-static (NQS) behavior of the model will also be discussed and verified with measurements. In the second part, the HF noise sources of MOSFETs extracted directly from the measured data are examined. Finally, based on the noise knowledge obtained from measurements, some strategies for the design of low noise, RFICs are presented.

II. AC SMALL SIGNAL MODELING
A. Modeling of Intrinsic and Parasitic Components

Compared with the MOSFET modeling for digital and low frequency analog applications, the HF modeling of MOSFETs is more challenging. All of the requirements for a MOSFET model in low frequency application, such as continuity, accuracy and scaleability of the DC and capacitance models should be maintained in a RF model. In addition, there are further important requirements of the RF models in describing HF small signal and nonlinear behavior as well as noise behavior of the device.

To achieve the above, the model for the intrinsic device should be derived with the inclusions of most (if not all) important physical effects in a modern MOSFET. Also, the continuities of small signal parameters such as transconductance g_m, channel conductance g_dS, and the intrinsic transcapacitances must be modeled properly. Further, (1) the gate resistance should be modeled; (2) the extrinsic source and drain resistances should be modeled as real external resistors, instead of only a correction to the drain current with a virtual component; (3) substrate coupling in a MOSFET, that is, the contribution of substrate resistance, needs to be modeled physically and accurately; (4) an accurate overlap capacitance model, describing the parasitic capacitive contributions between the gate and drain/source/bulk, needs to be included; and (5) the models for these parasitic components should be physics-based and linked to process and geometry information to ensure the scalability and prediction capabilities of the model. Also, simple sub-circuits are preferred to reduce the simulation time and to make parameter extraction easier. Fig.1 shows a typical subcircuit model of a MOSFET for RF applications.

![Fig. 1: A subcircuit that can be implemented in a circuit simulator.](image)

At DC and low frequency, the gate resistance consists mainly of the poly silicon sheet resistance. At HF, however, two additional physical effects appear. One is the distributed transmission line effect on the gate, and the other one is the distributed effect or Non-Quasi-Static (NQS) effect in the channel [3],[4]. For the devices with NQS effects, additional bias and geometry dependences of the gate resistance are needed to account for the NQS effect, as shown in figs. 2 and
3, based on which, an optimized width-per-finger should be used in the design to reduce the effective $R_G$ [3],[5].

In figs. 4 and 5, the capacitances $C_{GDP}$ and $C_{GSP}$, where $C_{GDP} = C_{GD_{total\_extracted}} - C_{GD_{intrinsic\_simulated}}$, and $C_{GSP} = C_{GS_{total\_extracted}} - C_{GS_{intrinsic\_simulated}}$, obtained from the total capacitances extracted from the measured s-parameters and the intrinsic capacitances simulated with the above RF model are shown. According to the definition of $C_{GDP}$ and $C_{GSP}$, these capacitances can be considered as overlap capacitances if the intrinsic capacitance model is accurate enough. However, in some cases, $C_{GDP}$ and $C_{GSP}$ should not be considered as overlap capacitances since they may contain the correction to the intrinsic capacitances if the intrinsic capacitances are not properly modeled. It is clear that $C_{GDP}$ and $C_{GSP}$ have strong bias dependences that cannot be fitted by a constant overlap capacitance model.

The substrate capacitance is another extrinsic capacitance that should be considered in a subcircuit model for ultra HF applications. In the above substrate RC network, the contribution of the substrate capacitance was not included. It does not influence the model accuracy to fit the measured data up to 10 GHz. However, the substrate capacitance component may be necessary in a subcircuit model when the device operates at frequencies much higher than 10 GHz.
B. Non-Quasi-Static (NQS) Modeling Issues

As discussed above, the NQS effect should be included for a RF model to accurately describe the HF characteristics of devices if the devices themselves exhibit this effect at the operating frequency. When the device cannot respond to the signal immediately, the distributed effect in the channel or NQS effect will cause an increase in the effective gate resistance, as demonstrated in figs. 2 and 3.

It is also known that the NQS effect will equivalently introduce a transcapacitance between the drain and gate. The displacement current from this additional capacitance (referred as $C_{nqs}$) can cancel partially the output current, which is equivalent to an increased delay to the signal. $C_{nqs}$ is negative relative to the positive gate-to-source, gate-to-drain, and gate-to-bulk capacitances $C_{GS}$, $C_{GD}$, and $C_{GB}$ so the effective $C_{GG}$ with NQS (the sum of $C_{GS}$, $C_{GD}$, $C_{GB}$ and $C_{nqs}$) is less than that without NQS (the sum of $C_{GS}$, $C_{GD}$, and $C_{GB}$ only). In devices with longer $L_f$, the NQS effect is stronger so $|C_{nqs}|$ is larger and hence $C_{GG}$ is smaller. Also, as the frequency increases, the NQS effect in the device is stronger so $|C_{nqs}|$ increases and $C_{GG}$ decreases, as shown in fig. 6.

$g_m$ is considered as the contribution of NQS effect even though it may be partially caused by the increased signal "feed-through" via $C_{GG}$ at HF. Fig. 7 shows a real($Y_{21}$) roll-off caused by the NQS effect as the frequency increases.

The modeling of the frequency dependent components caused by the NQS effect is challenging in compact models for circuit simulation. Due to the existence of the NQS effect, a MOSFET model based on the quasi-static approximation may not accurately describe the HF device behavior.

In figs. 8 and 9, the simulation results obtained by using the models with and without considering the NQS effect are shown. It is clear that the model without the NQS effect cannot predict correctly the device behavior in both $Y_{11}$ and $Y_{21}$. By including the NQS effect, the RF model with BSIM3v3 as the core model can predict the measured data very well in both of the real and imaginary parts of $Y_{21}$. However, the model needs to be improved for fitting $Y_{11}$. Further investigation of the model including the implementation is needed to improve the accuracy of the BSIM NQS model. The inclusion of the NQS effect would be a desirable feature for a RF model even though it remains a question whether the devices in RF circuits for small-signal applications will operate in the frequency region at which the devices show significant NQS effects.

III. NOISE MODEL FOR RF CIRCUIT DESIGNS

RF noise model of MOSFETs consists of two parts - a.c. lumped elements and noise sources. Fig. 10 shows RF noise
model of an intrinsic MOSFET that is suitable for high-frequency circuit applications. For the noise sources in fig. 10, $i_d^2$ is the channel noise caused by the mobile carriers in the channel, $i_s^2$ and $i_b^2$ are the noise current sources caused by the source ($R_S$) and drain ($R_D$) resistances, $i_G^2$ is the noise current source caused by the polysilicon gate resistance ($R_G$), and $i_{DB}^2$, $i_{SB}^2$, and $i_{DSB}^2$ is the noise current source caused by the substrate resistance $R_{DB}$, $R_{SB}$ and $R_{DSB}$, respectively. When transistors operate in the GHz range, the random potential fluctuations in the channel resulting in the channel noise will be coupled to the gate terminal through the gate oxide capacitance and cause the induced gate noise $i_G^2$, which is usually correlated with the channel noise. The noise sources $- i_s^2$, $i_b^2$, $i_G^2$ and $i_{DSB}^2$ are thermal noise with spectral density $4kT/R$ and will be determined as long as their corresponding resistance $R$ is obtained through with either DC or a.c. measurements. The noise sources needed to be characterized are the channel noise, $i_s^2$, induced gate noise $i_G^2$, and their correlation $i_{GS}i_{GD}^*$. The term $i_{GS}^2$ consists of the thermal noise (white noise) and the flicker noise. The flicker noise mainly affects the performance of the device at low frequencies and can be ignored at high frequencies, except for some RF circuits such as mixers or oscillators in which the low frequency noise will be up-converted to the frequencies around the carrier and deteriorate the phase noise and signal-to-noise ratio.

**A. Channel Noise**

The first task in the characterization of the dominant noise source - channel noise is to obtain the noise currents directly from RF noise measurements. Several different extraction methods [11]-[13] have been published in the literature and only the one in [13] can extract the channel noise, induced gate noise and their correlation simultaneously. Figs. 11 and 12 show the extracted channel noise versus frequency and $V_{GS}$ characteristics for n-type MOSFETs with different channel lengths biased at $V_{DS} = 1.0$ V [13].

It is shown that the channel noise, in general, is frequency independent and increases when the channel length is decreased or the $V_{GS}$ is increased. This is because of the higher output conductance in both cases.

After having the direct targets for the channel noise, the next step is to derive a physics-based analytical model. The approach used to calculate the channel noise is based on the model in which the channel of a MOSFET is divided into two regions - a gradual channel region with length $L_{elec}$ and a velocity saturation region with length $\Delta L$ [17],[18] when the device is saturated, the normal operating mode for RFICs.

![Fig. 13: Cross section of a MOSFET channel divided into a gradual channel region (I) and a velocity saturation region (II).](image)

In region I, the channel exhibits near ohmic conductivity and the gradual channel approximation holds. In region II, the carriers travel at their saturated velocity and ohmic’s law fails. Because the carriers in region II will not respond to any a.c. voltage fluctuation and produce zero noise current at the drain...
terminal, it is assumed that no noise current will be contributed from region II. Based on the noise model derived in [18] for region I, the spectral density of the channel noise can be obtained by

\[ S_{i_d} = \frac{4kT \Delta f \mu_{\text{eff}}}{L_{\text{elec}}^2} \left| -Q_{\text{inv}} \right| + 8\frac{kT I_D \Delta f}{L_{\text{elec}} E_{\text{crit}}^2 V_{DS}} \]

(1)

where \( k \) is the Boltzmann constant, \( T_0 \) is the lattice temperature (K), \( \mu_{\text{eff}} \) is the effective mobility, \( E_{\text{crit}} \) is the critical electrical field, \( I_D \) is the DC current, \( Q_{\text{inv}} \) is the inversion charge in the gradual channel region and \( V_{DS} \) is the voltage between the drain and the source terminals. If the device works in the saturation region, \( V_{DS}\text{Sat} \) instead of \( V_{DS} \) will be used in equation (1). The second term in equation (1) is used to model the hot electron effect [15]. Because equation (1) is obtained based on the thermal noise theory which is only true in the gradual channel region, \( L_{\text{elec}} \) instead of \( L_{\text{eff}} \) will be used in equation (1) in order to model the channel length modulation (CLM) effects.

Fig. 14 shows the extracted (symbols) and simulated (lines) channel noise \( \overline{i_d} \) versus \( V_{GS} \) characteristics for the n-type MOSFETs with channel width \( W = 10 \times 6 \) µm and channel lengths \( L = 0.97 \) µm, 0.42 µm and 0.18 µm, respectively biased at \( V_{DS} = 1.5 \) V without hot electron effects (\( \delta = 0 \)). The solid lines are obtained using \( L_{\text{elec}} \) in equation (1) and the dashed lines are obtained using \( L_{\text{eff}} \). It seems that the hot electron effect does not have strong impact on the channel noise [20]. In addition, it is shown that the CLM effect begins to have some impact on the channel noise when the channel length of the device is smaller than 0.5 µm and the exclusion of the CLM effect will predict lower channel noise.

Fig. 14: Measured (symbols) and simulated (lines) channel noise \( \overline{i_d} \) versus bias \( V_{GS} \) characteristics of n-type MOSFETs.

For the \( V_{DS} \) dependence of the channel noise, fig. 15 shows extracted (symbols) and calculated (lines) channel noise versus \( V_{DS} \) characteristics for the n-type MOSFETs with channel width \( W = 10 \times 6 \) µm and channel lengths \( L = 0.97 \) µm, 0.42 µm and 0.18 µm, respectively biased at \( V_{GS} = 1.0 \) V with \( \delta = 0 \). The solid lines are obtained using \( L_{\text{elec}} \) in equation (1) and the dashed lines are obtained using \( L_{\text{eff}} \) in the noise calculation. It is shown that the calculated channel noise using \( L_{\text{eff}} \) predicts lower channel noise and cannot mimic the increasing trend of the extracted channel noise caused by the CLM effect for the deep sub-micron devices.

Fig. 15: Measured (symbols) and simulated (lines) channel noise \( \overline{i_d} \) versus drain bias \( V_{DS} \) characteristics of n-type MOSFETs.

Sometimes, the spectral density of the channel noise \( \overline{i_d} \) will be expressed by

\[ \overline{i_d} = \gamma \cdot 4kT \rho_{\text{so}} \]

(2)

where \( g_{\text{so}} \) is the output conductance at zero drain bias (i.e. \( V_{DS} = 0 \)) [15]. For long-channel devices, the value of \( \gamma \) is between 1 (in the linear region with \( V_{DS} = 0 \)) and 2/3 (in the saturation region) [15,16]. However, for short-channel devices, the value of \( \gamma \) will become greater than 2/3 in saturation [20] and this is caused mainly by the CLM effect. Fig. 16 shows the measured (symbols) and simulated (lines) \( \gamma \) versus gate bias \( V_{GS} \) characteristics of an n-type MOSFET with channel length \( L = 0.18 \) µm and width \( W = 10 \times 6 \) µm biased at \( V_{DS} = 1.5 \) V without including the hot electron effect and the noise contributed from the velocity saturation region. It is shown that for the deep-submicron MOSFETs, the \( \gamma \) value will be increased from 2/3 to 1.2 or 1.8 (depending on the \( V_{GS} \) bias) when the channel length is reduced. In addition, at a fixed \( V_{DS} \) bias, the \( \gamma \) value will be decreased when the \( V_{GS} \) value is increased [19]. However, if the \( L_{\text{eff}} \) is used in the calculation of channel noise (dashed line in fig. 16), the \( \gamma \) factor increases towards unity when \( V_{GS} \) is increased which is the opposite trend of the extracted channel noise.

Fig. 16: Measured (symbols) and simulated (lines) \( \gamma \) versus gate bias \( V_{GS} \) characteristics of n-type MOSFETs.
B. Induced Gate Noise and Correlation Noise

The concept of the induced gate noise has been introduced about three decades ago [21]. But many researchers are studying how to model it correctly [15], [22]. Figs. 17 and 18 show the extracted induced gate noise $i_{ig}$ and the correlation noise $i_{ic}^2$ versus frequency characteristics for the n-type MOSFETs with channel width $W = 10 \times 6 \mu m$ (10 fingers of width 6 $\mu m$) and lengths $L = 0.97 \mu m$, 0.64 $\mu m$, 0.42 $\mu m$, 0.27 $\mu m$ and 0.18 $\mu m$, respectively, biased at $V_{DS} = 1.0 V$ and $V_{GS} = 1.2 V$ [13]. It is shown that the induced gate noise and the correlation term are proportional to $f^2$ and $f$, respectively where $f$ is the operating frequency (solid lines in the figures). In addition, when channel length decreases, both the induced gate noise and the correlation term also decrease because of the decrease of $C_{GS}$.

For the bias dependence of the extracted noise sources, figs. 19 and 20 show the extracted induced gate noise $i_{ig}$ and its correlation noise with the channel noise $i_{ic}^2$ versus bias characteristics for the n-type MOSFETs with channel width $W = 10 \times 6 \mu m$ and lengths $L = 0.97 \mu m$, 0.64 $\mu m$, 0.42 $\mu m$, 0.27 $\mu m$ and 0.18 $\mu m$, respectively, biased at $V_{DS} = 1.0 V$. It is shown that the induced gate noise has a weak $V_{GS}$ dependence because it is mainly determined by the gate-to-source capacitance instead of the voltage or current fluctuation within the channel. On the other hand, for the correlation noise, it increases then tends to saturate when $V_{GS}$ increases. This follows the $V_{GS}$ dependence of the channel noise. However, the correlation noise decreases when the channel length is reduced and this follows the channel length dependence of the induced gate noise.

IV. DESIGN OF LOW NOISE CIRCUITS

After understanding the physics of the noise sources in MOSFETs, the most general questions being asked by the circuit designers are how to properly choose the device size, select the bias conditions ($V_{GS}$ and $V_{DS}$), and design the device geometries to achieve the best noise performance for RFICs. In this section, the noise behavior of MOSFETs will be explained qualitatively based on the extracted noise sources [13] and noise parameters, and this leads to the proper selection of the device size and the determination of the bias conditions.

A. Selection of Bias Conditions

In general, as shown in fig. 21, the minimum noise figure $NF_{min}$ decreases when $V_{GS}$ increases at low $V_{GS}$ region, and it increases at high $V_{GS}$ region. This can be understood by comparing the measured transconductance $g_m$ (shown in fig. 22) and the extracted channel noise $i_{ic}^2$ (shown in fig. 12) versus $V_{GS}$ characteristics. Basically, $NF_{min}$ is mainly determined by these two factors - $g_m$ and $i_{ic}^2$. In the low $V_{GS}$ region, the increasing rate of $g_m$ (or the first order derivative of $g_m$...
with respect to $V_{GS}$) is greater than that of $g_d$ and therefore it causes the drop of $NF_{\text{min}}$. However, in the high $V_{GS}$ region, since $g_m$ decreases but $g_d$ keeps increasing, this causes $NF_{\text{min}}$ to increase.

There are two observations that can be made from this explanation. First, as shown in fig. 21, the $V_{GS}$ value for the lowest $NF_{\text{min}}$ becomes lower when the channel length is reduced, and this is because of the faster increase of $g_m$ for the short channel devices. Second, from fig. 21 and fig. 22, it is shown that the lowest $NF_{\text{min}}$ actually happens before the peak $g_m$ instead of at the peak $g_m$. This is because the derivative of $g_m$ with respect to $V_{GS}$ is zero at the peak $g_m$.

As for the selection of the device size, as shown in fig. 21, the smallest devices will not always guarantee the best noise performance (i.e. the smallest devices is higher than that of 0.27 $\mu$m devices) and how to select the device size will depend on the selection of the bias conditions.

For the $V_{DS}$ dependence, figs. 23 to 25 show the measured intrinsic transconductive $g_m$, minimum noise figure $NF_{\text{min}}$ at 2 GHz and equivalent noise resistance $R_n$ at 2 GHz versus $V_{GS}$ characteristics for the n-type MOSFETs with channel width $W = 10 \times 6 \mu$m and lengths $L = 0.97 \mu$m biased at $V_{DS} = 1.0$ V, 1.5 V and 2.0 V, respectively. It is shown that, at higher $V_{DS}$, because of the increase of $g_m$ at high $V_{GS}$ region and this causes $NF_{\text{min}}$ and $R_n$ drop at high $V_{GS}$ region. Therefore, higher $V_{DS}$ bias will make the noise performance of the transistor to be less sensitive to the $V_{GS}$ variation at the price of higher power consumption. However, the $V_{DS}$ bias does not modify the $V_{GS}$ bias where the lowest $NF_{\text{min}}$ and $R_n$ occur.

**B. Consideration of Device Geometry**

The second dominant noise sources in MOSFETs at RF regions is the noise from the gate resistance $R_G$. In general, the gate resistance can be modelled by

$$R_G = \frac{R_{GSH} \cdot W}{3 \cdot M \cdot n^2 \cdot L}$$  

(3)
where $R_{GSH}$ is the gate sheet resistance, $W$ and $L$ are the channel width and length, respectively, $M$ is 1 or 4 depending on the gate connected at one end or both ends, and $n$ is number of fingers. From equation (3), we can find that by using the multi-finger design and connecting the input signal to both ends of the gate will reduce the gate resistance to a very small value. Fig. 26 shows the measured $NF_{\text{min}}$ (symbols) of a 60 $\mu$m transistor and a multi-finger gate design in which there are six 10 $\mu$m wide transistors connected in parallel. It is shown that the multi-finger gate design improves 1.2 dB $NF_{\text{min}}$ by decreasing the gate resistance $R_G$.

![Fig. 26: Measured $NF_{\text{min}}$ of a single 60 $\mu$m transistor (squares) and a multi-finger gate design (circles) with six 10 $\mu$m wide transistors.](image)

**V. CONCLUSIONS**

In this paper, we have discussed AC and NQS modeling of MOSFETs for RF applications. An accurate RF MOSFET model with a simple substrate network is presented. The model has been verified with high frequency measurements. The developed RF MOSFET model can be a basis of a predictive and statistical modeling approach for RF applications. The multi-finger RF MOSFET model has been verified with high frequency measurements. An accurate RF MOSFET model with a simple substrate network is presented. The authors would like to thank the support from Canadian Microelectronics Corporation (CMC), Conexant Systems Inc., Micronet, a federal network center of excellence in microelectronics, and the Natural Sciences and Engineering Research Council (NSERC) of Canada.

**ACKNOWLEDGEMENTS**

The authors would like to thank the support from Canadian Microelectronics Corporation (CMC), Conexant Systems Inc., Micronet, a federal network center of excellence in microelectronics, and the Natural Sciences and Engineering Research Council (NSERC) of Canada.

**REFERENCES**


