Surface activated bonding of copper through silicon vias and gold stud bumps at room temperature

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A comprehensive investigation of the surfaces of copper through silicon vias (Cu-TSVs) and gold stud bumps is presented. These vias and stud bumps were bonded at room temperature using a nanobonding and interconnection equipment. The influence of heating on the bonded interface was also studied. In order to achieve an intimate contact between the Au-stud bumps and Cu-TSVs, the stud bumps were flattened under an external force of 20 N before bonding. The surface roughness of the flattened area was improved due to deformation of the bumps. Specimens with high deformation provided better alignment accuracy than those with low deformation. The Cu-TSV surface showed inhomogeneous behavior due to the influence of electroplating and chemical mechanical polishing. Tensile pulling test of the bonded interfaces showed three fractures modes in the bulk of the Au bump and the Au pad. The electrical resistance of the bonded interface was dependent on the surface morphology of the bumps and TSVs, the distance between the bumps and TSVs, the locations of the bumps and TSV with respect to the argon fast atom beams, and the distribution of external force during bonding. Heating at 200 °C for 60 h in air increased the electrical resistance of the bonded interface. This investigation shows that the vertical integration of Au/Cu at room temperature and low bonding force can be applied to three-dimensional interconnections for low cost miniaturized systems.
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I. INTRODUCTION

High-density interconnection at low temperature is a key focus area of research for systems miniaturization.[1] The low temperature integration is important in avoiding artifacts such as changing of dopant profile in transistors or performance degradation of temperature-sensitive devices during high temperature bonding. An example of a miniaturized system is the noninvasive wireless imaging capsule for early detection of defective cells in human organs, such as the gastrointestinal tract.[2,3] Such miniaturized systems require high speed with enhanced performance. The bonding quality of the interconnection, such as low electrical resistance and high bonding strength associated with their stability, is critical in miniaturized systems.

As a room temperature bonding method, surface activated bonding (SAB) provides the bonded interface with (a) high bond strength, (b) low contact resistance, and (c) high microstructural stability.[4,5] In the SAB method, two smooth surfaces, each with root mean square roughness less than 1 nm, bond at room temperature due to atomic scale adhesion of surface atoms.[6] In fact, for many practical applications, either the surfaces are not as smooth as required for the SAB method, or the shape and size of the surfaces are not compatible with SAB. For example, stud bumps have been utilized in microelectronics packaging[7,8] for a long time. A stud bump consists of a bump with a wire. This wire is placed on top of the bump using ultrasonic bonding. Thus, the shape of the top surface of the remaining wire on the bumps (i.e., stud bumps) after cutting causes difficulty in making this surface polished and smooth, an important requirement for SAB. A low cost solution is to flatten the top surface of the stud bumps by applying an external force on this surface. After flattening, even though the surface roughness is higher than that required in SAB, the rough surfaces of gold stud bumps (Au-SBs) can still be bonded at room temperature using SAB.

Currently, copper through silicon vias (Cu-TSVs) is considered as the best candidate for microelectronics packaging of devices such as image sensors. This is because Cu has higher conductivity and better electromigration stability than all the other interconnect materials.[9] Thus, the bonding between Au-SBs and Cu-TSVs is highly desirable for high-density interconnections. This provides three-dimensional (3D) integration with reduced interconnection length and, thus, reduces the signal delay problem.[10] At present, the 3D integration is mainly accomplished using thermosonic compression bonding,[7,8] compressive force at room temperature,[11] and thermocompression bonding at 250–300 °C.[12,13] The challenge in implementing these

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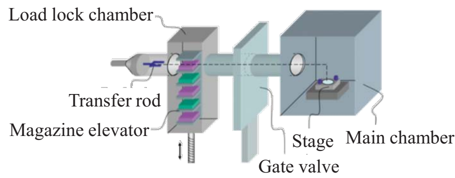


FIG. 1. (Color online) Schematic of NBIS.

methods for integration with the miniaturized TSVs is the requirement that the bonding is done using a high bonding force and at high temperature. To alleviate these requirements and achieve high quality bonding between the Au-SBs and Cu-TSVs at room temperature with low bonding force, a number of challenges such as surface morphology control must be addressed. Surface morphologies of both the stud bumps and the Cu-TSV control the quality of the bonding and performance of the bonding process. This performance includes alignment accuracy, mechanical strength, and electrical conductivity of the bonded interface.

This article reports a comprehensive analysis of the surfaces of Au-SBs and Cu-TSVs and the mechanical and electrical behaviors of the bonded interface in order to achieve the high quality bonded interface. The vertical integration of Au-SBs and Cu-TSVs using the SAB at room temperature and low bonding force has been used for the emerging systems' applications at low cost.

II. EXPERIMENT

Standard Au-SBs and Cu-TSVs were used for the bonding experiments. The Au-SBs were fabricated by ultrasonic bonding of Au wires to Au bumps on silicon. The formation of the two-step shape on the Au-stud bumps was due to pushing of the ultrasonic bonder nozzle on to the Au bumps during bonding, before cutting the Au wire. The base and height of the Au-stud bump were 50 and 37 μm, respectively. The height and diameter of the Cu-TSVs were 150 and 55 μm, respectively. 1 μm thick silicon dioxide was grown in the vias before Cu filling. For Cu-TSVs, the vias in silicon were filled with Cu using electroplating technique followed by removal of excess Cu on the silicon surface using chemical mechanical polishing (CMP). Following, the other side of Cu-TSVs was thinned down using backgrinding of silicon and polished using CMP. This step reduced Cu-TSV heights to 150 μm. The Cu-TSVs and Au-SBs were bonded using the nanobonding and interconnection system (NBIS) shown in Fig. 1. The NBIS consists of a load lock chamber and a bonding chamber that are separated by a gate valve. The bonding chamber is equipped with a high precision alignment system, two argon fast atom beam (Ar-FAB) sources, and a bonding head. The pressure in the bonding chamber was 1.0×10^{-7} Pa. The background pressure during surface activation was 2.4×10^{-2} Pa. Before bonding, the surfaces were activated using a 1.5 keV Ar-FAB with a current of 48 mA for 300 s. The top and bottom chips were simultaneously activated using two Ar-FAB sources positioned at 45° with respect to the chips. The specimens were

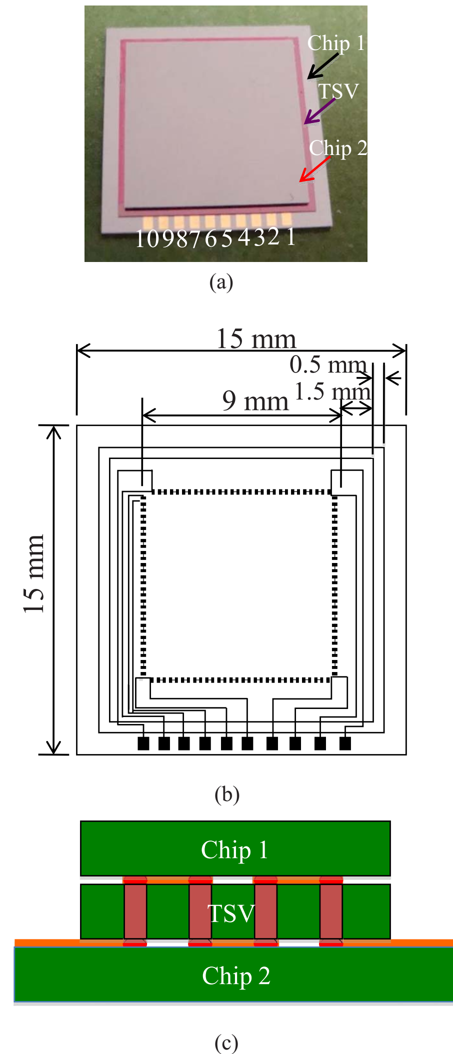


FIG. 2. (Color online) (a) Optical image, (b) schematic of the vertically integrated system with locations of Au-stud bumps and TSVs, and (c) cross-sectional view of the vertical integration. The Au-stud bumps of chip 1, and Au-stud bumps with probe electrodes of chip 2 are bonded on the top and bottom of TSVs' chip.

aligned first by optical and then by infrared transmission techniques. Finally the specimens were contacted under the bonding head with external forces of 0.08–0.16 N (8–16 g) per bump at room temperature for 3 min to achieve strong bonding strength.

Figure 2 shows the optical image and schematics of the vertically integrated system in which the Cu-TSVs are sandwiched between chips 1 and 2. This also indicates that the Au-SBs are vertically placed on the top and bottom of the Cu-TSVs. The dimensions of chip 1, TSV, and chip 2 were 15×15, 13×13, and 12×12 mm^2, respectively, as shown in Fig. 2(b). The Au-SBs and TSVs were located 4.5 mm from the center of the chips. The total numbers of TSVs were 120 [Fig. 2(b)]. Each TSV has two contacts after bonding [Figs. 2(b) and 2(c)]. Each Cu-TSV was bonded with top and bottom Au-SBs.

Surface roughness is a major concern for room temperature bonding. Here, the surface roughness of Au-SBs was

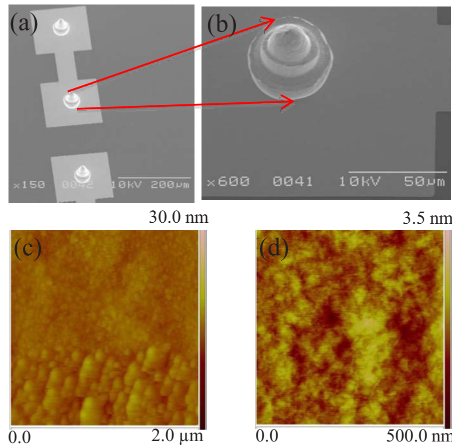


FIG. 3. (Color online) SEM images of Au-stud bumps with (a) low and (b) high resolutions. AFM images of Au-stud bump surfaces with scan areas of (c) 2×2 and (d) 0.5×0.5 μm^2 before deformation.

investigated before deformation (i.e., before applying the external bonding force) and after deformation. Due to flatness of Cu-TSV surface, no deformation experiment was done with Cu-TSVs. To gain insight into the surface morphology of Cu-TSVs and Au-SBs, an atomic force microscope (AFM) (Veeco Dimension Icon, Micro- and Nano-Systems Laboratory, McMaster University) was used for surface roughness measurements. For bonding strength measurements, the bonded specimens were glued with copper jigs using a tensile pulling tester (Instron, McMaster Univeristy). After vertical integration of the Au-SBs and the Cu-TSVs, the electrical resistance of the interface was measured using a semiconductor parameter analyzer (HP-4145B).

III. RESULTS AND DISCUSSION

Figure 3 shows the scanning electron microscope (SEM) images of Au-SBs with (a) low and (b) high resolutions, and AFM images of Au-SBs surfaces with scan areas of (c) 2 $\times2$ μm^2 and (d) 500×500 nm^2 before deformation. The SEM image in Fig. 3(b) shows elliptical shape of the bump, which restricts the surfaces' roughness measurement over large scan areas. The measured surface roughnesses of the Au-SBs were 1.01 and 0.34 nm for 2×2 μm^2 and 500 $\times500$ nm^2 scan areas, respectively. The surface inhomogeneity of the area in contact and the shape of the Au-SBs do not allow bonding with Cu-TSVs using SAB. Therefore, the top surface of the Au-SBs was flattened using an external force that smoothed the surface roughness as well.

Figure 4 compares the surface morphology of Au-SBs after deformation with external forces of 10 [(a)–(d)] and 20 N [(e)–(h)] applied over the whole area of chip 2. The external force dependent deformation behavior was observed. The higher external force produced a wider area of deformation. Deformed and nondeformed areas are observed [Figs. 4(b) and 4(f)]. The surface roughness of the deformed area was smoother compared with the nondeformed area. For the chip deformed with 10 N, the surface roughnesses of the deformed (over 10×10 μm^2) and nondeformed (over 10 $\times10$ μm^2) areas were 27.2 and 35 nm, respectively. On the other hand, when 20 N force was used, the surface roughnesses of the deformed (over 10×10 μm^2) and nondeformed (over 10×10 μm^2) areas were 9.6 and 36.1 nm, respectively. This indicates that the surface roughness of the deformed area with a higher external force (i.e., 20 N) was considerably lower than that with the lower external force (i.e., 10 N). In fact, while the deformation under 10 N reduced the heights of Au-stud bumps by 19%, it was reduced 30% under 20 N (Table I).

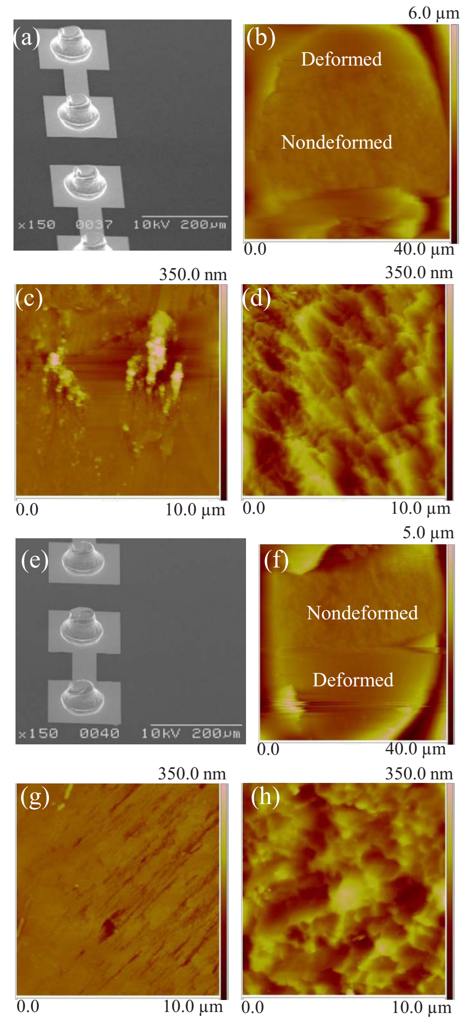


FIG. 4. (Color online) Comparative analysis of surface morphology of Au-stud bumps after deformation with external forces of 10 N. (a) SEM image of three bumps with pads and the AFM images of surface over (b) 40 $\times40$ μm^2, (c) 10×10 μm^2 of deformed area, and (d) 10×10 μm^2 of nondeformed area of a bump, and 20 N, (e) SEM images of three bumps with pads and the AFM images of surface over (f) 40×40 μm^2, (g) 10 $\times10$ μm^2 of deformed area, and (h) 10×10 μm^2 of nondeformed area of a bump.

Figure 5 shows the optical images of Cu-TSVs with low (top) and high (bottom) resolutions after CMP. Four types of TSV surfaces were observed. The dark areas {center and whole black area in Fig. 5 [both top and bottom (a)–(c)]} were deeper than the brighter areas surrounding the circle. This may be due to the chemical reaction between the Cu surface and the chemicals used for CMP. Another possible

TABLE I. Alignment accuracy of before bonding and after bonding, and Au-bump height under different bonding forces.

Specimens	Alignment accuracy before bonding (μm,°)			Alignment accuracy after bonding (μm,°)			Bonding force (N)	Bump height (in μm) with force (N)		
	X	Y	θ	X	Y	θ		0	10	20
Chip 1/TSV	0.14	0.15	0.002	2	2	0.005	10	37 ± 3	30 ± 2	26 ± 1.5
Chip 2/TSV	0.1	0.18	−0.001	4	4	0.2				
Chip 1/TSV	0.09	0.02	0.0007	−2	2	−0.0005	20			
Chip 2/TSV	0	−0.29	−0.0001	−1.29	−0.99	−0.00076				

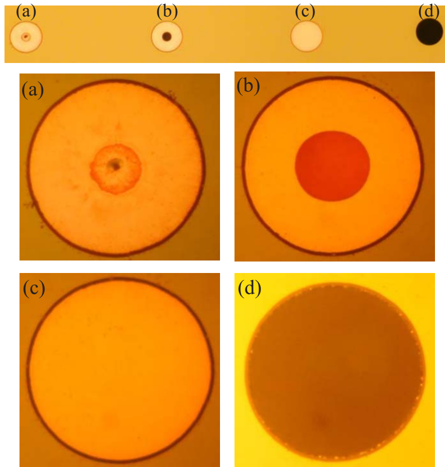


FIG. 5. (Color online) Optical images of Cu-TSVs with (a) low (top) and high (bottom) resolutions after CMP. Four types of surfaces, (a) type I, (b) type II, (c) type III, and (d) type IV, were observed. The size of the Cu-TSV was 55 μm.

reason is the imperfect Cu filling in the TSVs at the time of electroplating. However, more investigation is needed to clarify this issue.

Due to the concave shape of the top surface of the TSV with dark (black) area, the height of the cantilever tip used in the AFM was lower than that of the TSV at the center. Therefore, surface roughness measurements of the TSV, as shown in Figs. 5(b) and 5(d), were not successful. The surface morphology of the partially defective TSV [Fig. 5(a)] and the perfect TSV [Fig. 5(c)] is given in Figs. 6 and 7, respectively. Figure 6 shows an optical image [Fig. 6(a)], which was analyzed using AFM images at the red circle region over 20×20 μm^2 [Fig. 6(b)], dark area at the center over 2×2 μm^2 [Fig. 6(c)], silicon (outside TSV) [Fig. 6(d)] over 2×2 μm^2, brighter area near the center over 2×2 μm^2 [Fig. 6(e)], and ring area near the center over 2×2 μm^2 [Fig. 6(f)]. Both the optical and AFM images [Figs. 6(a) and 6(b)] showed that there was a 29 nm deep hole at the center. This is caused either by CMP or imperfect Cu filling in the TSVs at the time of electroplating. The surface roughnesses over the areas indicated in Fig. 6(a) were 29.4, 4.62, and 7.31 nm, respectively. The images shown in Figs. 6(c), 6(e), and 6(f) indicate that the bright area is smooth. Note that this smooth surface was rougher than the silicon surface, which was 0.2 nm, as shown in Fig. 6(d). On the other hand, the

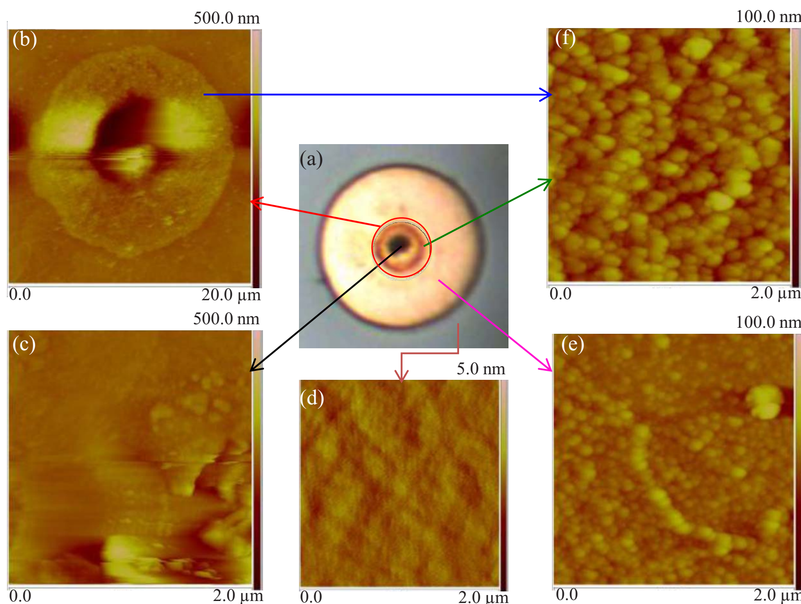


FIG. 6. (Color online) (a) Optical image, and AFM images at the (b) red circle region over 20×20 μm^2, (c) dark area at the center over 2×2 μm^2, (d) silicon (outside TSV) over 2×2 μm^2, (e) brighter area near the center over 2×2 μm^2, and (f) ring area near the center over 2×2 μm^2 of the type I surface of Cu-TSV.

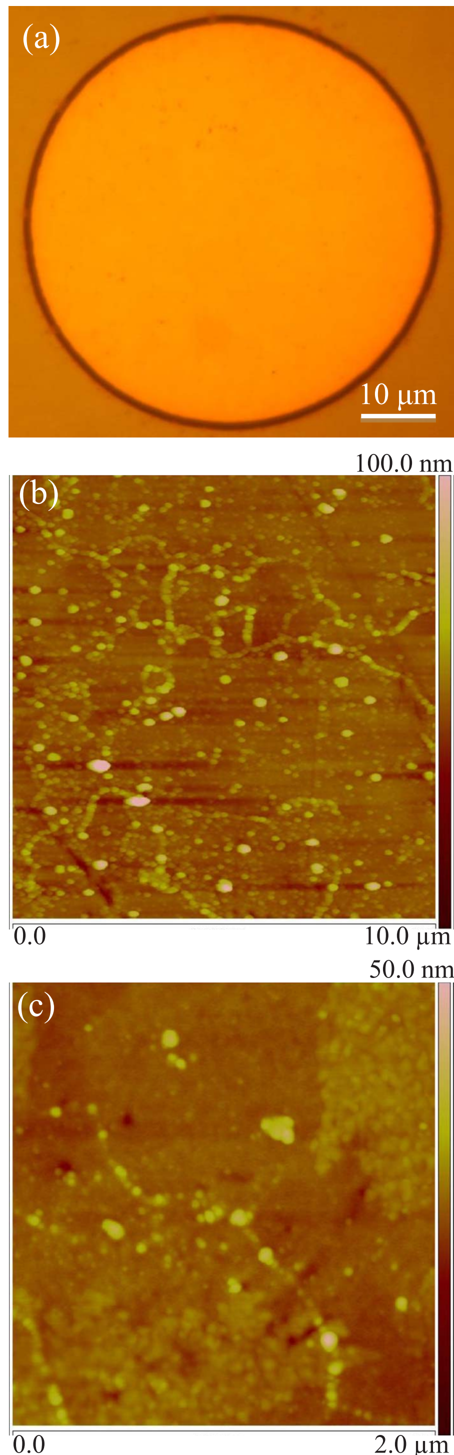


FIG. 7. (Color online) (a) Optical image, and AFM images over (b) $10 \times 10\ \mu m^2$ and (c) $2 \times 2\ \mu m^2$ of the type III surface of Cu-TSV.

surface roughnesses of the perfect TSV over areas of 10×10 and $2 \times 2\ \mu m^2$ were 6.0 and 2.4 nm, respectively (Fig. 7).

Table I shows the alignment accuracy between Au-SBs and Cu-TSVs before and after bonding under bonding forces of 10 and 20 N. Alignment accuracy was determined through reading positions of Au alignment marks on the chip and substrate using an infrared transmission camera. Details of the alignment procedure are given in Ref. 14. A correlation of the deformation with the alignment accuracy and contact resistance was observed. The alignment accuracy between the specimens with high deformation was higher than that with low deformation. Figures 8(a) and 8(b) show the optical images of the cross-sectional view of the bonded interface between the Au-SBs on chip 2 and Cu-TSVs bonded with external bonding forces of 10 and 20 N, respectively. In Fig. 8(a), the width of Au-SBs was 44 μm. The base of the Au-SBs was 64 μm. The contact length of the bonding interface between Cu-TSV and Au-stud bump was about 15.6 μm. The rest of the Au-stud bump (i.e., 27.4 μm) was bonded with Si. The alignment accuracy achieved between the stud bump and the TSV was lower than that observed between the alignment marks after bonding. In Fig. 8(b), there was no significant misalignment between the bumps and TSVs throughout the whole bonding area. A conical shape defect at the bottom side of TSV was also observed after debonding between the Au-SBs on chip 1 and Cu-TSVs. As previously mentioned, there were four types of TSV surfaces observed before bonding. The defect observed as dark areas in the optical image in Fig. 5(b) was corresponded to the conical shape defect in Fig. 8(b). Figure 8(c) shows an example of the optical image of the vertically integrated system in which the Cu-TSVs are sandwiched between Au-SBs on chips 1 and 2 with an external bonding force of 20 N. The alignment accuracies for both the chips with TSV were nearly identical to that of the chip and TSV (Table I).

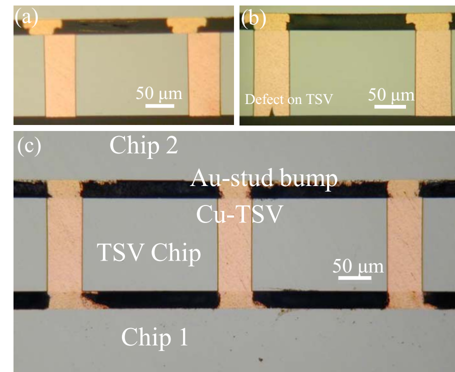


FIG. 8. (Color online) Optical image of cross-sectional view of the bonded interface between the Au-stud bump on chip 1 and Cu-TSV with external bonding forces of (a) 10 and (b) 20 N, and (c) optical image of cross-sectional view of vertically integrated system between Au-stud bumps and Cu-TSVs with the external bonding force of 20 N.

Figure 9 shows the fracture images of Au-SB and Cu-TSV surfaces after tensile pulling test of the bonded interface between Au-SBs and Cu-TSVs. Three fracture modes were observed. Figures 9(a) and 9(b) show that Au-stud bump was removed from Au-pad and remained on Cu-TSV; Figs. 9(c) and 9(d) show that Au-stud bump was broken in the middle and remained on Cu-TSV; Figs. 9(e) and 9(f) show that Au-stud bump was broken partially and remained on Cu-TSV. The bulk fracture was observed in Au, as shown in Figs. 9(c)–9(f). The bulk fracture of Au was due to the high bonding strength of the bonded interface between Au-SB and Cu-

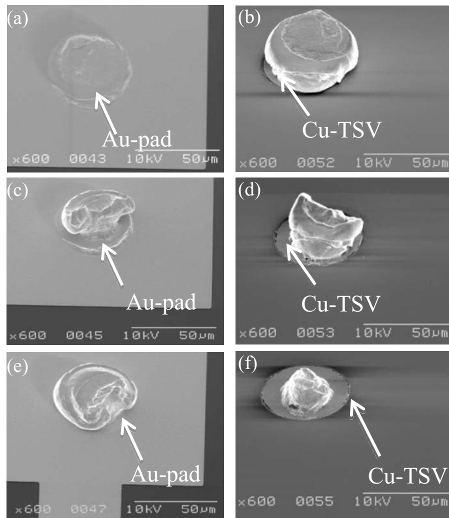
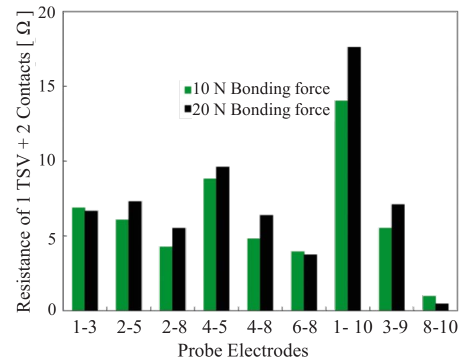
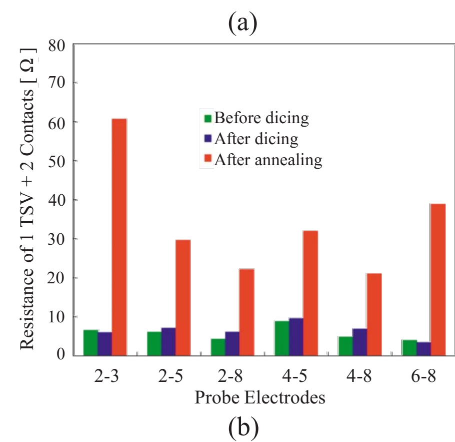


FIG. 9. Fracture images of Au-SBs/Cu-TSVs' interfaces created under an external force of 20 N after tensile pulling test. Three types of fractures, [(a) and (b)] bump removed from the pad and fully remained on TSV, [(c) and (d)] bump broken in the middle and remained on TSV, and [(e) and (f)] bump broken partially and remained on TSV, were observed.





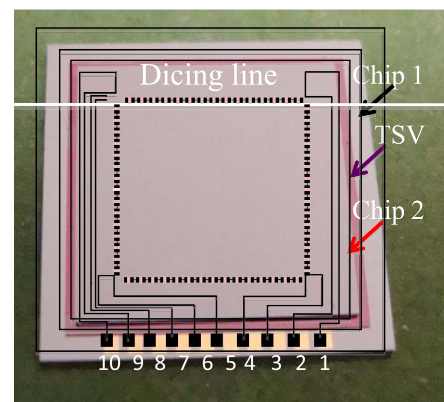


FIG. 10. (Color online) (a) Electrical resistance per contact measured between different probe electrodes at bonding forces of 10 and 20 N at room temperature. (b) Electrical resistance per contact measured between different probe electrodes at bonding force of 10 N before dicing, after dicing, and after annealing at 200 °C for 60 h in air. (c) Schematic of the vertically integrated system with the dicing location.

TSV. The high bonding strength between the Au microbumps and Cu-TSV is very important for miniaturized interconnects required for the 3D systems' integration.

Figure 10(a) shows the electrical resistance of a single TSV and two contacts (interfaces between Cu-TSV and Au-SB) measured between different probe electrodes at bonding forces of 10 and 20 N at room temperature. The electrical resistance of the single TSV and two contacts was estimated from the total resistance between the relevant probe electrodes after subtracting the relevant line resistance of Au. Table II shows the number of contacts between the probe electrodes. The resistance varied as a function of the probe electrode. The resistance was higher in the integrated chips under higher bonding force. Also, the resistance decreased with improving alignment accuracy [compare between Table I and Fig. 10]. The probe electrodes connected to the integrated stud bumps with TSV at different locations. The resistance of the single TSV and two contacts in both the 10 and 20 N integrated chips varied depending on the locations. For example, the resistance of the contacts and TSV between probes 1 and 3 is lower than that between probes 1 and 10. Another example is the resistance between probes 8 and 10. This resistance (between probes 8 and 10) is the lowest among the probes. In fact, the resistance between these probes should be higher than that of other probes. This is because there are 120 contacts between probes 8 and 10. While the average contact resistance in the individual measurement was 37.6 Ω, it became 0.5 Ω measured directly between probes 8 and 10. This is due to the current flow between the shortest distance of the two lines connecting to the pads with the bumps. Therefore, the differences in the resistance between different probes were caused by the discrepancies in (a) the surface morphology of the bumps and TSVs, (b) the distance between the bumps and TSVs, (c) the locations of the bumps and TSV with respect to the Ar-FABs, and (d) the distribution of external force during bonding.

Figure 10(b) shows the average resistance of a single TSV and two contacts (interfaces between Cu-TSV and Au-SB) of the 10 N integrated chip before dicing, after dicing and after annealing. The annealing temperature was 200 °C. The dicing location is about 300 μm below the upper TSVs, as shown in Fig. 10(c). Before the dicing, the contact resistance was lowest compared with that after dicing and after annealing. The increase in resistance after dicing is due to artifacts caused by the external forces during dicing. The resistance of

TABLE II. Number of contacts for different probe electrodes after bonding.

Probe electrodes	No. of contacts
1–3	30
2–5	60
2–8	90
4–5	30
4–8	60
6–8	30
1–10	30
3–9	60
8–10	120
7–8	0

contacts near the dicing location was higher than that of other locations. This implies significant impact of the amount of force acting on the bonded interface during dicing. After annealing, the contact resistance was significantly increased, but there was no relationship in the resistance of the contacts' locations. Further investigation is planned to find the cause of the increase in the contact resistance after heating.

IV. CONCLUSIONS

Cu-TSVs have been vertically bonded between Au-SBs at room temperature after surface activation using a 1.5 keV Ar-FAB for 300 s in vacuum at 10^{-7} Pa under external forces of 10 and 20 N. The surface morphology of the Au-SBs and Cu-TSVs was investigated to explain the mechanical and electrical behaviors of the bonded interface. Before bonding, the Au-SBs were flattened using external force. The external force controlled the surface morphology and deformation of the bumps. We observed that higher deformation resulted in higher alignment accuracy. Cu-TSV surfaces were inhomogeneous due to electroplating and chemical mechanical polishing. The electrical resistance of the interface depended on the surface morphology of the bumps and TSVs, the distance between the bumps and TSVs, the locations of the bumps and TSV with respect to the Ar-FABs, and the distribution of external force during bonding. After heating the bonded interface at 200 °C for 60 h in air, the electrical resistance was increased. This investigation shows that the vertical integration of Au-SBs/Cu-TSVs at room temperature and low bonding force can be applied to three-dimensional interconnections for low cost miniaturized systems.

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