COE2DI4 Logic Design
Fall 2010

Instructor: Dr. Shahram Shirani
Rooms: ITB-A320
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Office Hours: Tuesdays and Thursdays 10:30-11:20 in ITB/A320
Schedule of Lectures: Tuesdays, Thursdays and Fridays 11:30-12:20 in JHE 376
Tutorials: Tuesdays 12:30-13:20 in T13/127 or Tuesdays 13:30-14:20 in T13/127

Course Objective: To understand the fundamentals of logic design and their relation to computer organization.

Outline of Major Topics:
Binary Numbers
Unsigned binary numbers, base conversions, representation of negative numbers, binary arithmetic
Boolean Algebra, Digital Logic and Electrical Properties of Logic Gates
Introduction to Boolean algebra, truth tables and logic gates
Propagation delay, signal levels, noise margins, fan-in, fan-out, glitches
Combinational Circuit Design
Circuit simplification using K-maps, ripple carry adders, carry look-ahead adders
Design of basic building blocks such as decoders, multiplexers, encoders, comparators
Implementation technology and programmable logic
Complementary metal-oxide semiconductors (CMOS) technology
Programmable logic arrays (PLA), field programmable gate arrays (FPGA), read only memories (ROM)
Introduction to hardware description languages (VHDL)
Sequential Circuit Design
Latches, flip-flops, counters, shift registers, state diagrams and tables
Control logic implementation using finite state machines (FSM)
Introduction to Computer Organization
Central processing unit (CPU), arithmetic and logic unit (ALU), register files
Register transfer logic; microoperations and microprograms

Format:
There is a course Web site accessible via links on the ECE department home page or directly from:
http://www.ece.mcmaster.ca/~shirani/2di4/2di4.html

This Web site will be the primary source for course-related information. You should check this site frequently for updates including lab descriptions and schedule, manufacturers' data sheets, problem sets and solutions, course announcements, etc.
Laboratories:
Laboratories are designed to enhance and supplement the lecture material. ***ATTENDANCE AT ALL LAB SESSIONS IS REQUIRED.*** The laboratory is located in ITB/143 and will be available for your use on one afternoon from 14:30 until 17:20 on alternate weeks. For the exact dates please check the lab schedule, which is posted on the course website. You will work in groups of 2. The five lab sessions are:

1. Logic Gates
2. Combinational Logic Design
3. Programmable Logic
4. Sequential Logic Design
5. Design of a Register File and Datapath

Labs will start in the week of September 20. The lab material and the lab schedule will be available on the course website. If you have not been assigned a lab section by the Office of the Registrar, then you should email the tutorial TA Michael Kinsner (kinsnemh@mcmaster.ca) between September 10th and 16th and provide him a list of three preferred lab sections where you wish to be assigned. In order to change your lab section you must bring to the instructor some formal documentation in the week of September 13 (after the class on Tuesday September 14, Thursday September 16, or Friday September 17). The documentation must prove why you need to change your lab section (e.g., letter from an employer, proof of conflict with other courses, letter from a medical doctor, ...). Only after your documentation has been verified by the instructor you should contact Michael Kinsner and follow the same procedure as outlined above.

Textbook:
"Fundamentals of Digital Logic with VHDL Design, third edition", **by Brown & Vranesic.**

Tests: In addition to the final exam, there will be ***two compulsory*** midterm tests on October 14 and November 9 (dates are subject to change). *Students who miss the midterms, and who have a valid excuse, will be accommodated. Those who do not have a valid excuse will be assessed zero for the midterm components of the final grade.*
Assessment:
Labs **10** %
Midterm Test #1 **20** %
Midterm Test #2 **20%**
Final Examination **50** %

Conversion from percentage to letter grade will be by way of the standard scale used in the Office of the Registrar. To pass the course you must obtain at least 50% on the final examination, attend all laboratory sessions and obtain at least 8 of the 10 points allocated to labs. Statistical adjustments (such as bell curving) will not normally be used.

Calculators:
"**NO** calculators will be allowed during tests and examinations"

Announcements:
The instructor reserves the right to choose the format (i.e. written or oral) of any deferred midterm or exam in this course.
Please note that announcements concerning any type of graded material may be in any format (e.g., announcements may be made only in class). Students are responsible for completing the graded material regardless of whether they received the announcement or not. What this means is that if you skip class and an announcement for a quiz, lab, test etc. is made in that class, then you are still responsible for that material. If you miss it, then you get zero.

Plagarism
Academic dishonesty will be taken very seriously. Any copying of labs etc. will be reported to the Office of Academic Integrity. Both the copyee and the copyor will be reported. On the first offence, the standard penalty is a zero on the work in question. Subsequent offences are much

more serious: the student is typically assigned an F in the course, with a transcript notation indicating the F is for academic dishonesty.

Policy Reminders
"The instructor and university reserve the right to modify elements of the course during the term. The university may change the dates and deadlines for any or all courses in extreme circumstances. If either type of modification becomes necessary, reasonable notice and communication with the students will be given with explanation and the opportunity to comment on changes. It is the responsibility of the student to check their McMaster email and course websites weekly during the term and to note any changes."

 "The Faculty of Engineering is concerned with ensuring an environment that is free of all adverse discrimination. If there is a problem, that cannot be resolved by discussion among the persons concerned, individuals are reminded they should contact the Departmental Chair, the Sexual Harassment Officer or the Human Rights Consultant, as soon as possible."
"Students are reminded that they should read and comply with the Statement on Academic Ethics and the Senate Resolutions on Academic Dishonesty as found in the Senate Policy Statements distributed at registration and available at the senate office."
"Academic dishonesty consists of misrepresentation by deception or by other fraudulent means and can result in serious consequences, e.g. the grade of zero on an assignment, loss of credit with a notation on the transcript (notation reads: "Grade of F assigned for academic dishonesty"), and/or suspension or expulsion from the university. It is your responsibility to understand what constitutes academic dishonesty. For information on the various kinds of academic dishonesty please refer to the Academic Integrity Policy, specifically Appendix 3, located at
http://www.mcmaster.ca/senate/academic/ac_integrity.htm
The following illustrates only three forms of academic dishonesty:
1. Plagiarism, e.g. the submission of work that is not one's own or for which other credit has been obtained
2. Improper collaboration in group work. (E.g., using previous year's lab reports).
3. Copying or using unauthorized aids in tests and examinations.