Serial Adder

- If speed is not of great importance, a cost-effective option is to use a serial adder
- Serial adder: bits are added a pair at a time (in one clock cycle)
- $A=a_{n-1}a_{n-2}\ldots a_0$, $B=b_{n-1}b_{n-2}\ldots b_0$

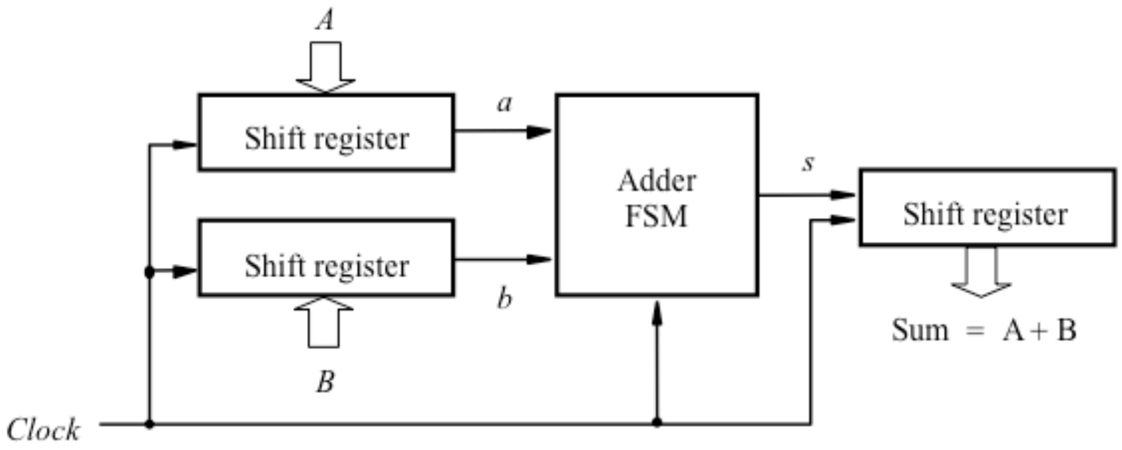


Figure 8.39. Block diagram for the serial adder.

Serial Adder

- G: state that the carry-in is 0
- H: state that the carry-in is1

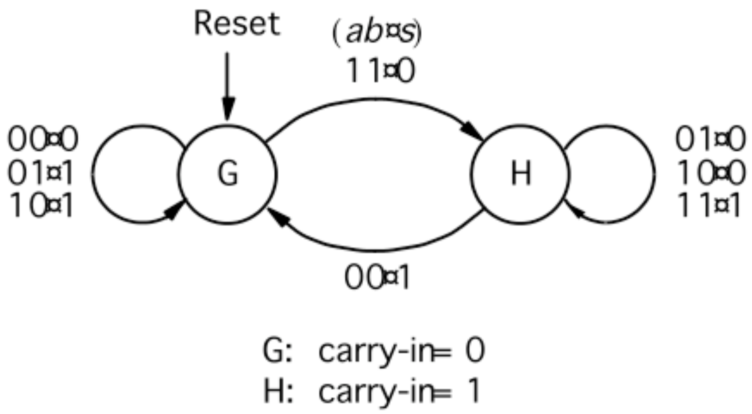
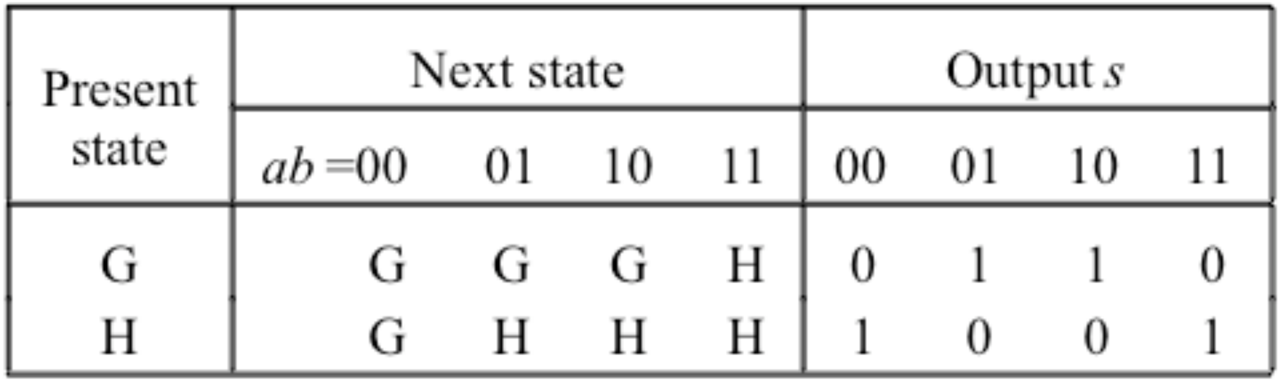


Figure 8.40. State diagram for the serial adder FSM.

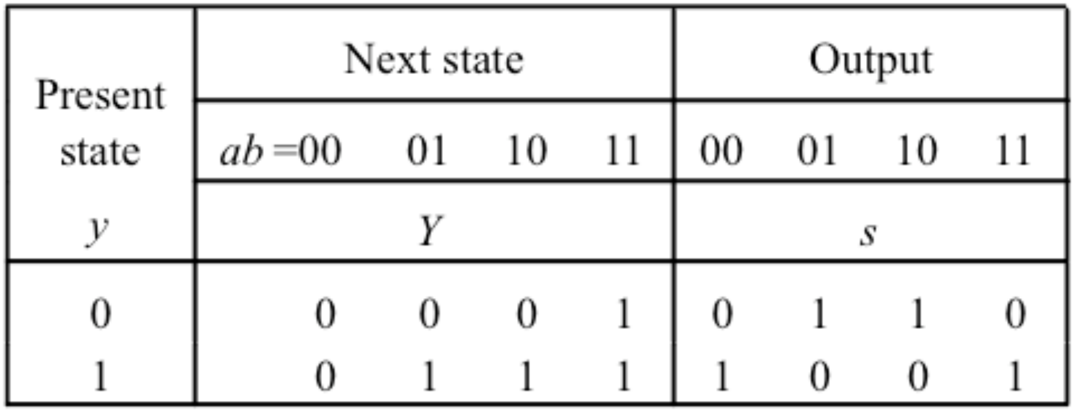
Serial Adder



Present state	Next state				Output s			
	ab =00	01	10	11	00	01	10	11
G	G	G	G	H	0	1	1	0
H	G	H	H	H	1	0	0	1

Figure 8.41. State table for the serial adder FSM.

Serial Adder



Present state	Next state				Output			
	ab =00	01	10	11	00	01	10	11
y	*Y*				*s*			
0	0	0	0	1	0	1	1	0
1	0	1	1	1	1	0	0	1

Figure 8.42. State-assigned table for Figure 8.41.

$$Y = ab + ay + by$$

$$s = a \oplus b \oplus c$$

Serial Adder

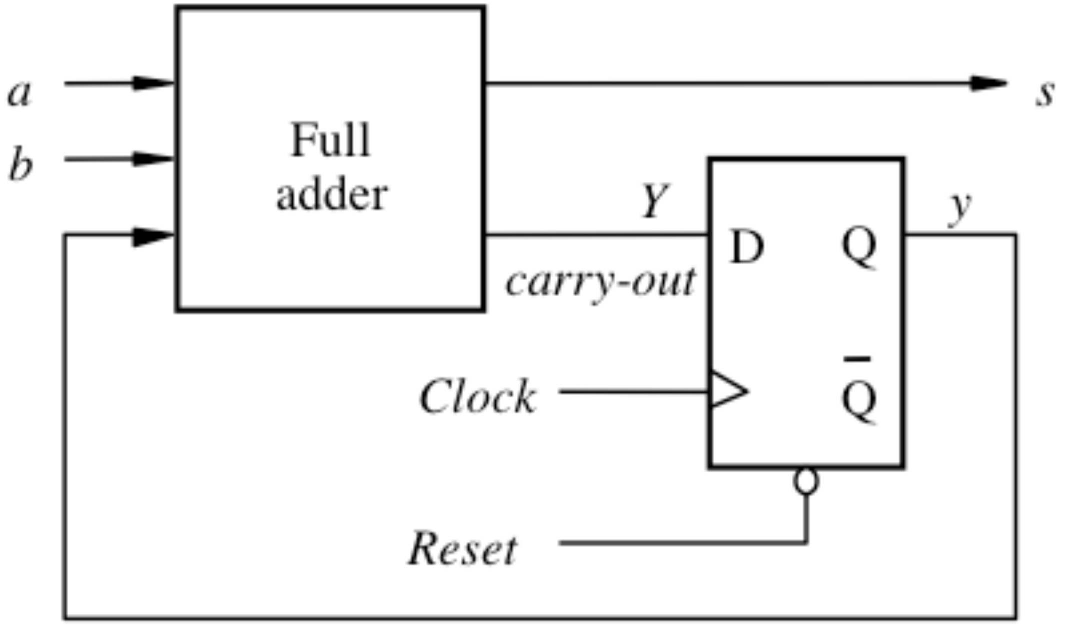


Figure 8.43. Circuit for the adder FSM in Figure 8.39.

Moore-type serial adder

- Since in both states G and H, it is possible to generate two outputs depending on the input, a Moore-type FSM will need more than two states
- G0 and G1: carry is 0 sum is 0 or 1
- H0 andH1: carry is 1 sum is 0 or 1

Moore-type serial adder

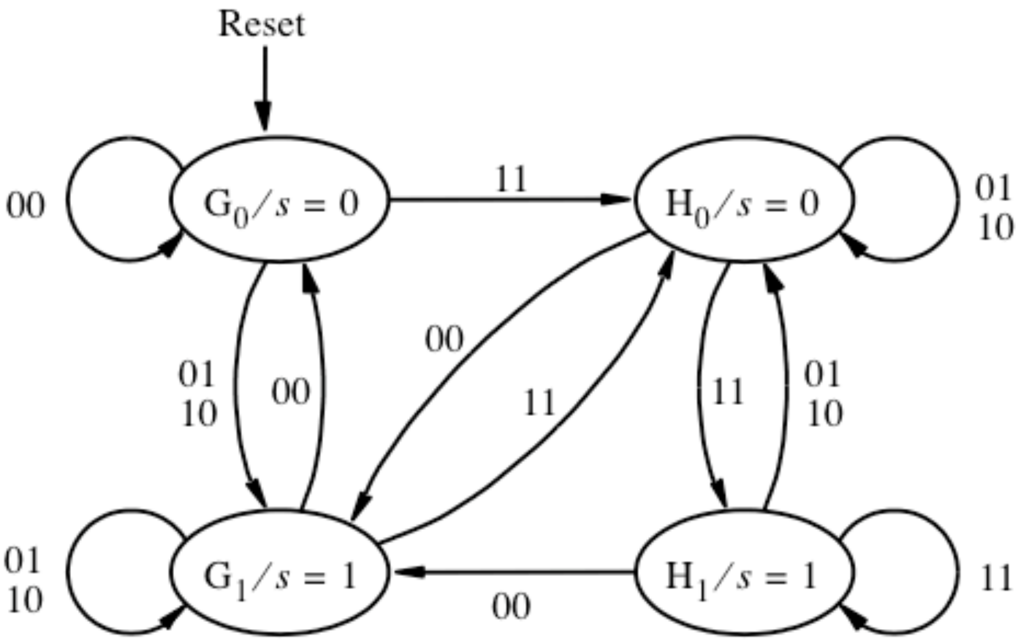
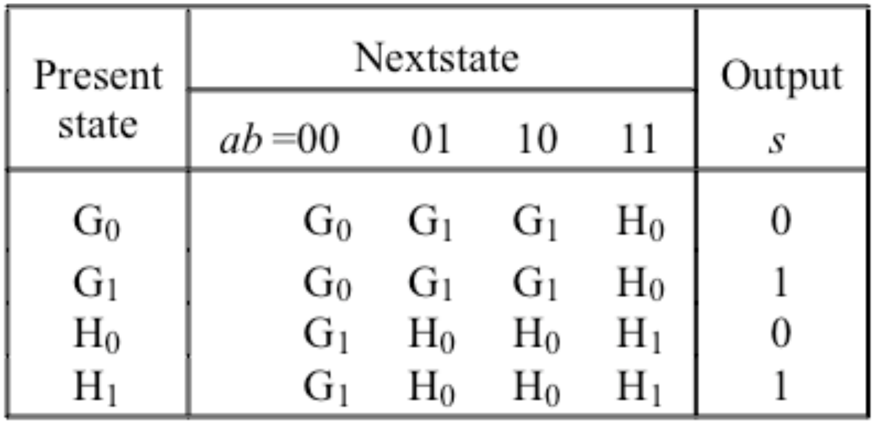


Figure 8.44. State diagram for the Moore-type serial adder FSM.

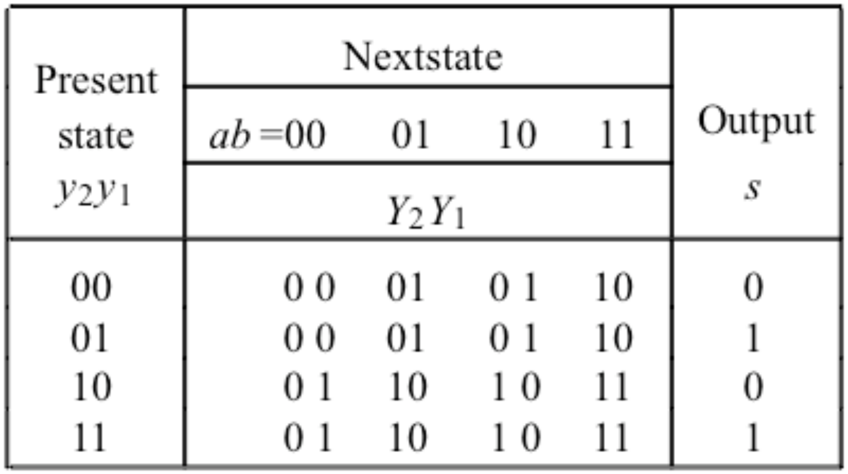
Moore-type serial adder



Present state	Nextstate				Output
	ab =00	01	10	11	*s*
G_0	G_0	G_1	G_1	H_0	0
G_1	G_0	G_1	G_1	H_0	1
H_0	G_1	H_0	H_0	H_1	0
H_1	G_1	H_0	H_0	H_1	1

Figure 8.45. State table for the Moore-type serial adder FSM.

Moore-type serial adder



Present state	Nextstate				Output
	ab =00	01	10	11	
y_2y_1	Y_2Y_1				s
00	0 0	01	0 1	10	0
01	0 0	01	0 1	10	1
10	0 1	10	1 0	11	0
11	0 1	10	1 0	11	1

Figure 8.46. State-assigned table for Figure 8.45.

$$Y_2 = ab + ay_2 + by_2$$

$$Y_1 = a \oplus b \oplus c$$

$$s = y_1$$

Moore-type serial adder

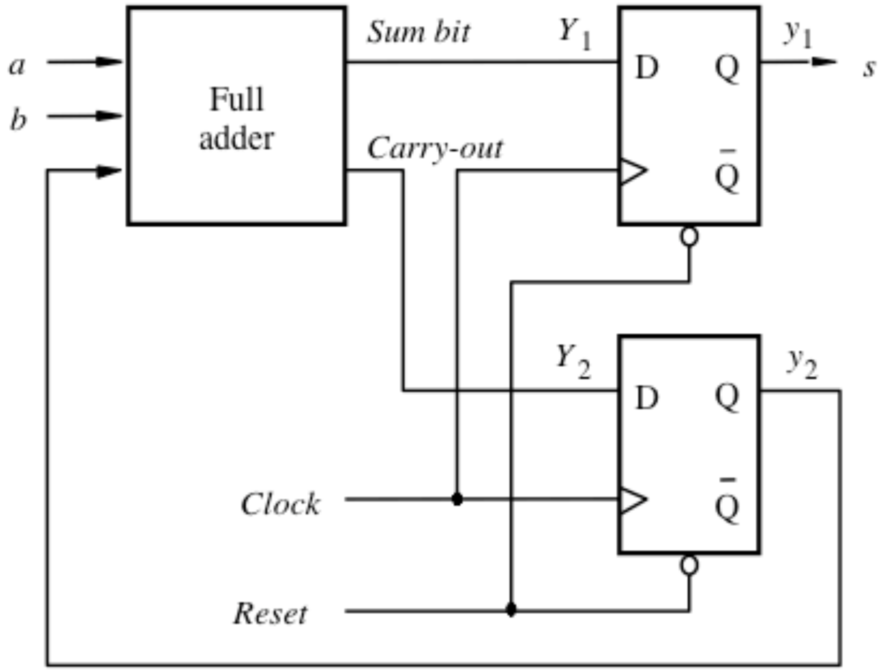


Figure 8.47. Circuit for the Moore-type serial adder FSM.

Counter design using sequential circuits

- Counting sequence: 0,1,2,3,4,5,6,7,0,1,..
- Input signal w: if w=1 count is incremented, if w=0 count is frozen

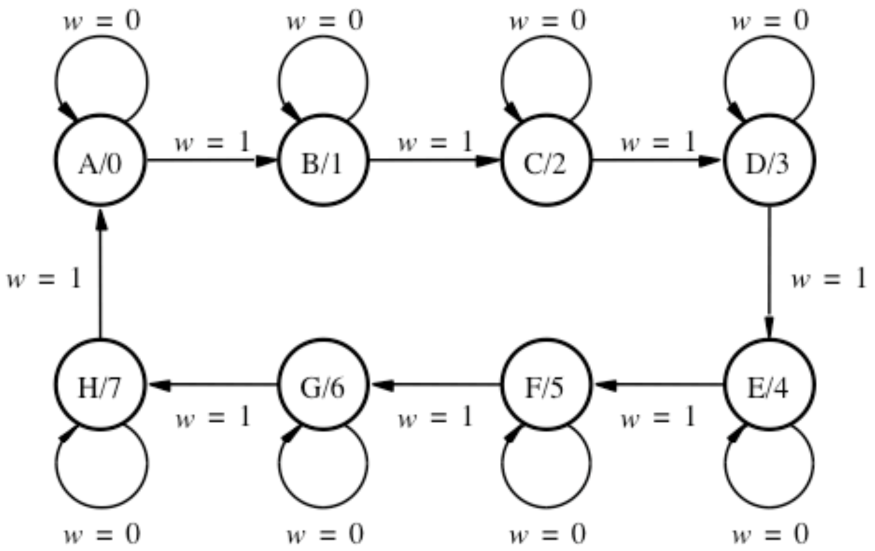
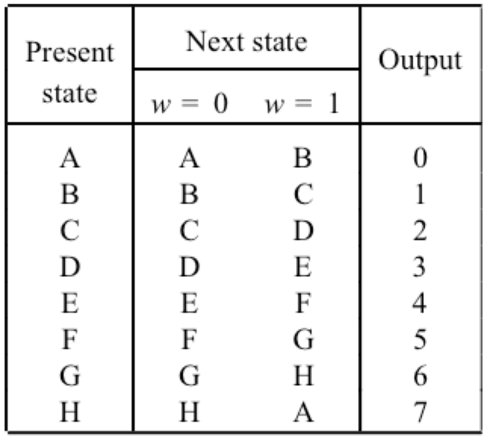


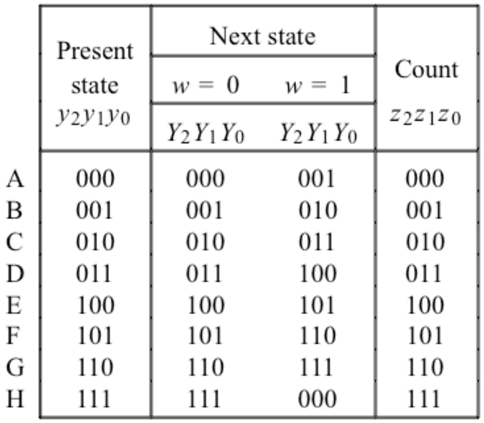
Figure 8.60. State diagram for the counter.

State table



Present state	Next state		Output
	$w = 0$	$w = 1$	
A	A	B	0
B	B	C	1
C	C	D	2
D	D	E	3
E	E	F	4
F	F	G	5
G	G	H	6
H	H	A	7

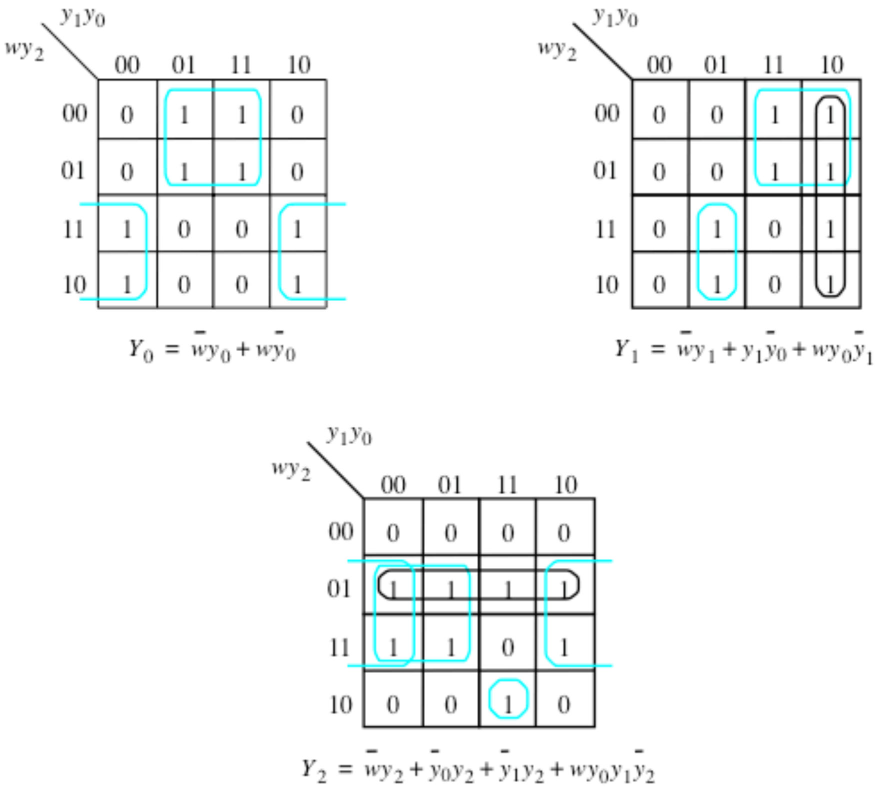
Figure 8.61. State table for the counter.



	Present state	Next state		Count
		$w = 0$	$w = 1$	
	$y_2y_1y_0$	$Y_2Y_1Y_0$	$Y_2Y_1Y_0$	$z_2z_1z_0$
A	000	000	001	000
B	001	001	010	001
C	010	010	011	010
D	011	011	100	011
E	100	100	101	100
F	101	101	110	101
G	110	110	111	110
H	111	111	000	111

Figure 8.62. State-assigned table for the counter.

Implementation using D flip-flop



wy_2 \ y_1y_0	00	01	11	10
00	0	1	1	0
01	0	1	1	0
11	1	0	0	1
10	1	0	0	1

$Y_0 = \bar{w}y_0 + w\bar{y}_0$

wy_2 \ y_1y_0	00	01	11	10
00	0	0	1	1
01	0	0	1	1
11	0	1	0	1
10	0	1	0	1

$Y_1 = \bar{w}y_1 + y_1\bar{y}_0 + wy_0\bar{y}_1$

wy_2 \ y_1y_0	00	01	11	10
00	0	0	0	0
01	1	1	1	1
11	1	1	0	1
10	0	0	1	0

$Y_2 = \bar{w}y_2 + \bar{y}_0y_2 + \bar{y}_1y_2 + wy_0y_1\bar{y}_2$

Figure 8.63. Karnaugh maps for D flip-flops for the counter.

$$D_0 = Y_0 = \bar{w}\, y_0 + w\, \bar{y}_0$$

$$D_1 = Y_1 = \bar{w}\, y_1 + y_1\, \bar{y}_0 + w y_0\, \bar{y}_1$$

$$D_2 = Y_2 = \bar{w}\, y_2 + y_2\, \bar{y}_0 + y_2\, \bar{y}_1 + w y_0 y_1\, \bar{y}_2$$

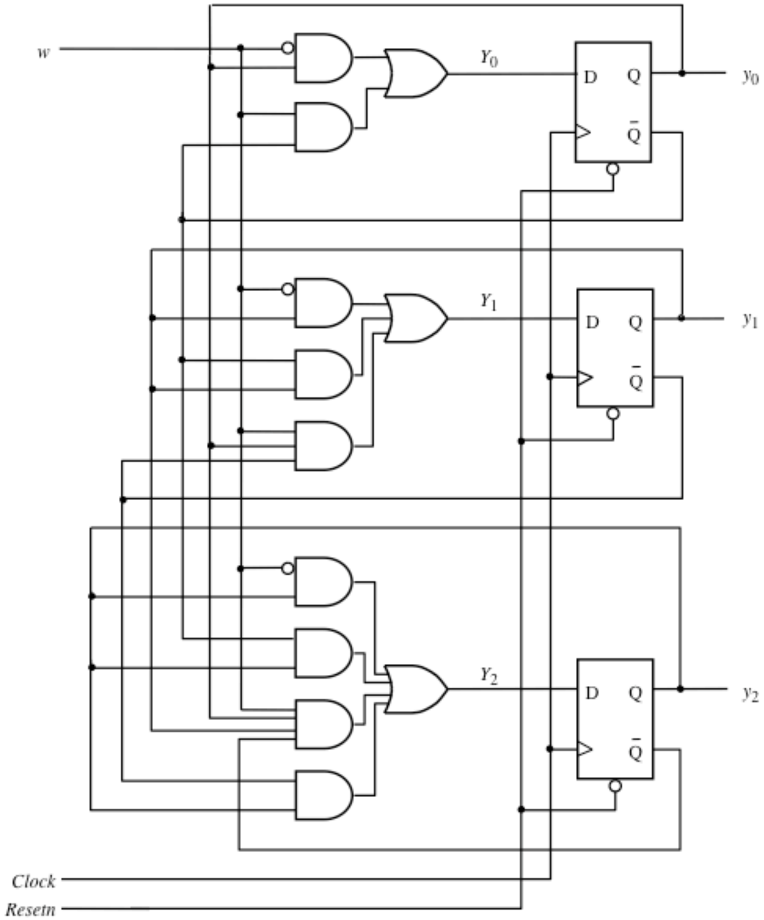
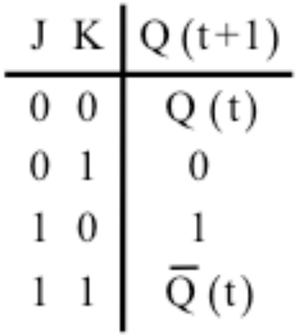


Figure 8.64. Circuit diagram for the counter implemented with D flip-flops.

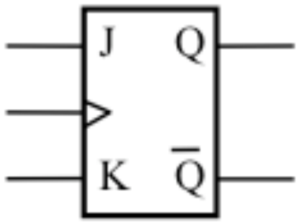
Implementation using JK flip-flop

- For a JK flip-flop:
  - If state=0, to remains in 0 J=0, K=d
  - If state=0, to change to 1 J=1, K=d
  - If state=1, to remains in 1 J=d, K=0
  - If state=1, to remains in 0 J=d, K=1



J	K	Q (t+1)
0	0	Q (t)
0	1	0
1	0	1
1	1	$\overline{Q}$ (t)

(b) Truth table



(c) Graphical symbol

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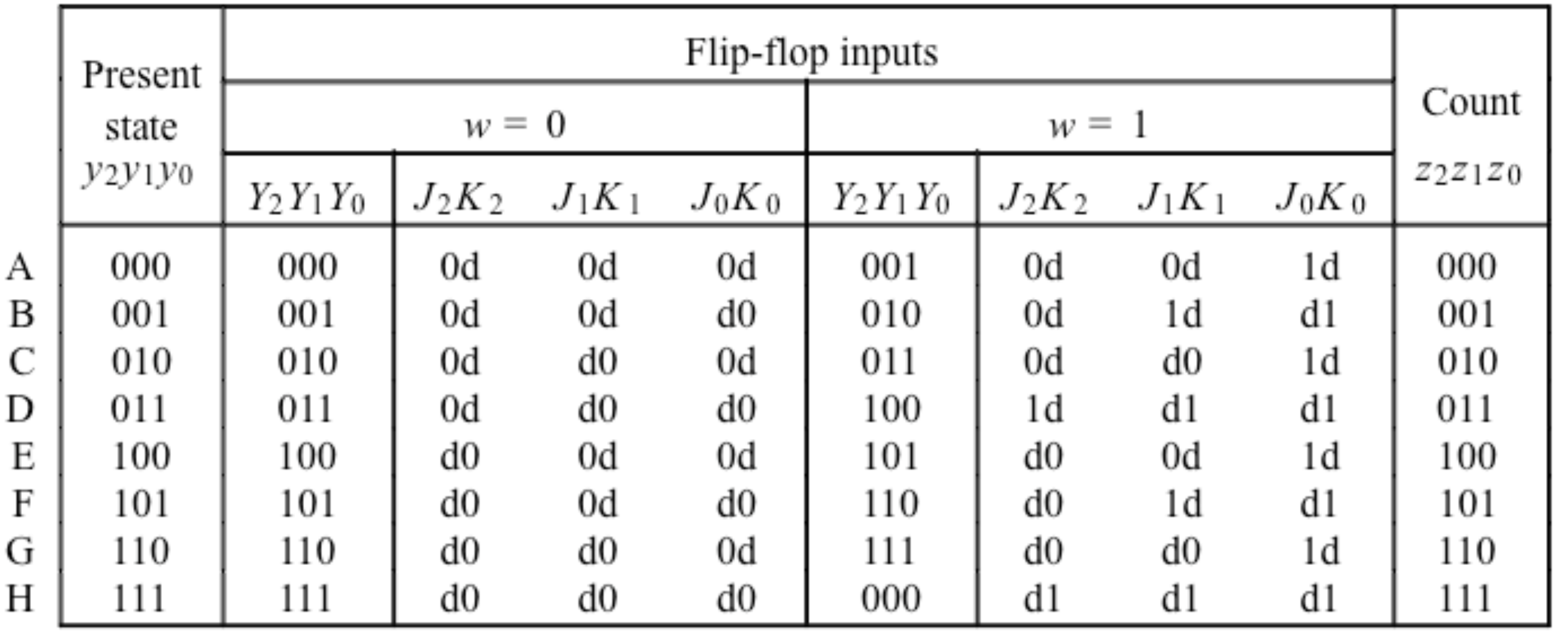
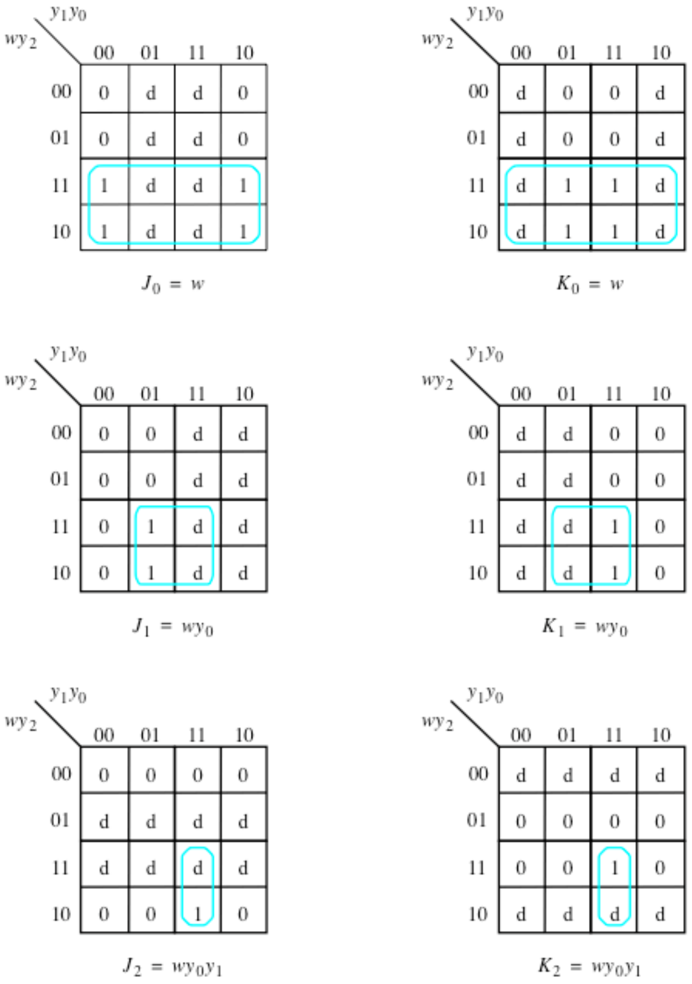


	Present state $y_2y_1y_0$	Flip-flop inputs								Count $z_2z_1z_0$
		$w = 0$				$w = 1$				
		$Y_2Y_1Y_0$	J_2K_2	J_1K_1	J_0K_0	$Y_2Y_1Y_0$	J_2K_2	J_1K_1	J_0K_0	
A	000	000	0d	0d	0d	001	0d	0d	1d	000
B	001	001	0d	0d	d0	010	0d	1d	d1	001
C	010	010	0d	d0	0d	011	0d	d0	1d	010
D	011	011	0d	d0	d0	100	1d	d1	d1	011
E	100	100	d0	0d	0d	101	d0	0d	1d	100
F	101	101	d0	0d	d0	110	d0	1d	d1	101
G	110	110	d0	d0	0d	111	d0	d0	1d	110
H	111	111	d0	d0	d0	000	d1	d1	d1	111

Figure 8.65. Excitation table for the counter with JK flip-flops.



wy_2 \ y_1y_0	00	01	11	10
00	0	d	d	0
01	0	d	d	0
11	1	d	d	1
10	1	d	d	1

$J_0 = w$

wy_2 \ y_1y_0	00	01	11	10
00	d	0	0	d
01	d	0	0	d
11	d	1	1	d
10	d	1	1	d

$K_0 = w$

wy_2 \ y_1y_0	00	01	11	10
00	0	0	d	d
01	0	0	d	d
11	0	1	d	d
10	0	1	d	d

$J_1 = wy_0$

wy_2 \ y_1y_0	00	01	11	10
00	d	d	0	0
01	d	d	0	0
11	d	d	1	0
10	d	d	1	0

$K_1 = wy_0$

wy_2 \ y_1y_0	00	01	11	10
00	0	0	0	0
01	d	d	d	d
11	d	d	d	d
10	0	0	1	0

$J_2 = wy_0y_1$

wy_2 \ y_1y_0	00	01	11	10
00	d	d	d	d
01	0	0	0	0
11	0	0	1	0
10	d	d	d	d

$K_2 = wy_0y_1$

Figure 8.66. Karnaugh maps for JK flip-flops in the counter.

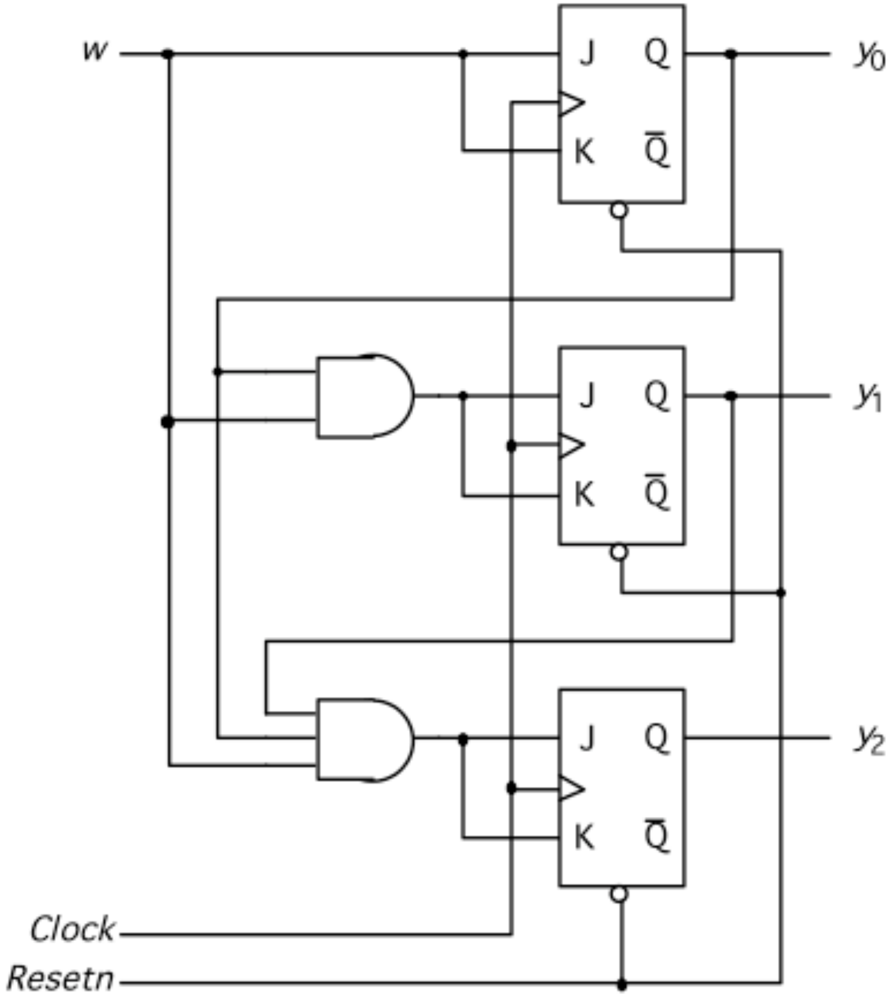


Figure 8.67. Circuit diagram using JK flip-flops.

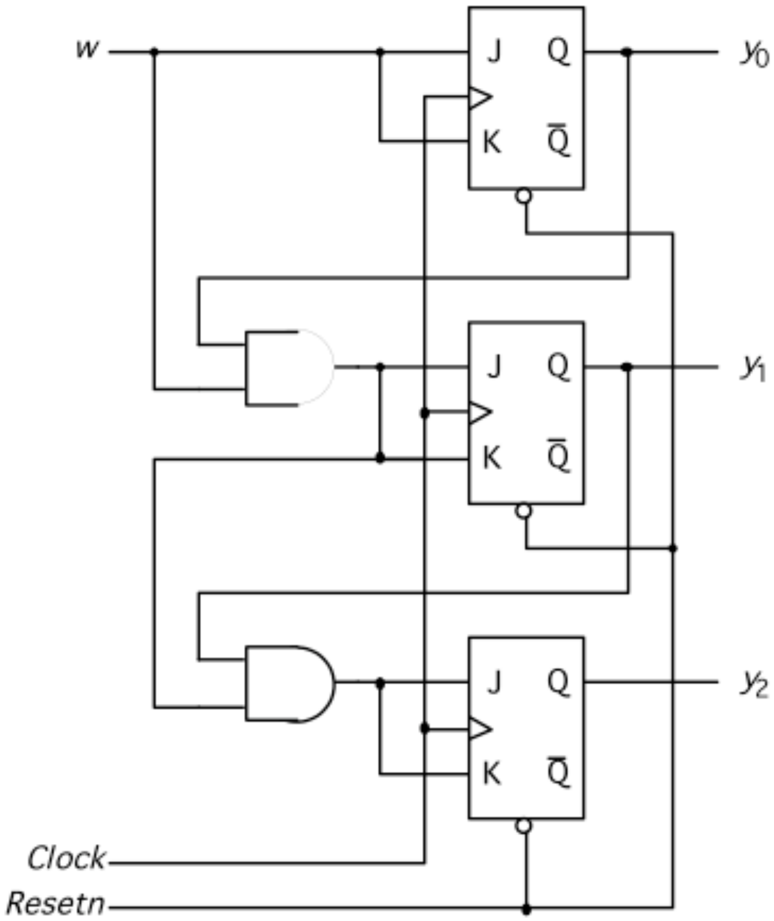


Figure 8.68. Factored-form implementation of the counter.

Analysis of Synchronous Sequential Circuits

- Outputs of flip-flops represent the current state
- Inputs of flip-flops determine the next state
- We can build the state transition table
- Then we build state diagram

Example 1

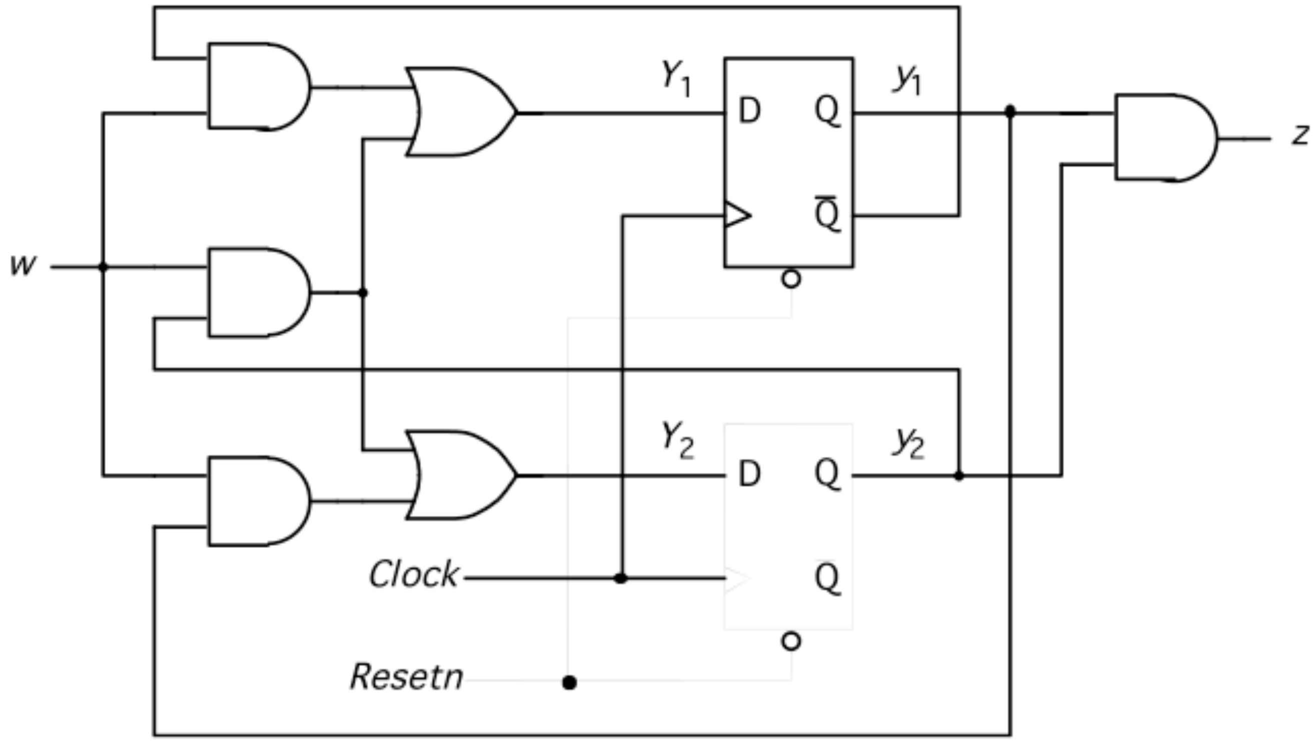


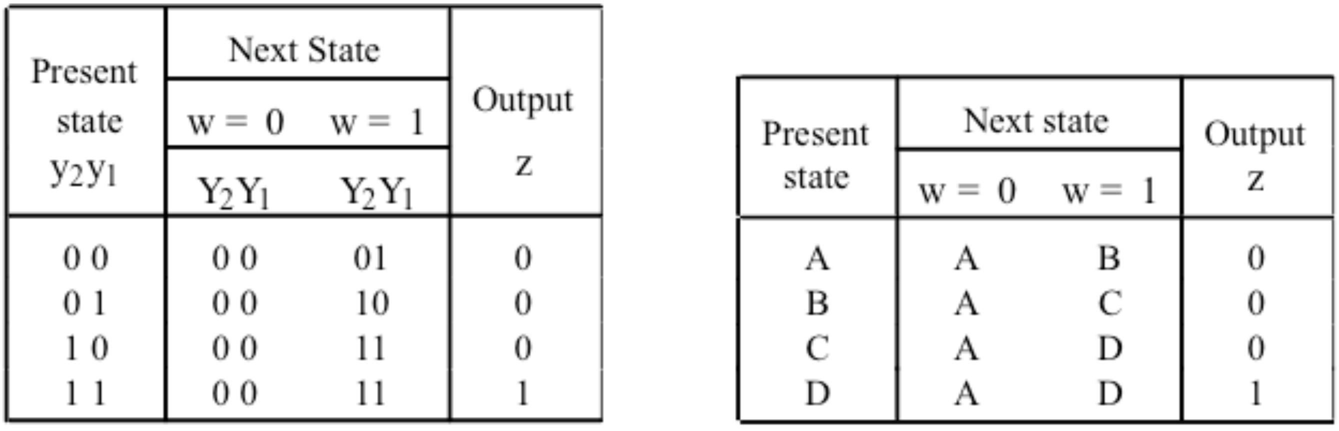
Figure 8.80. Circuit for Example 8.8.

Example 1

$$Y_1 = wy_2 + w\bar{y}_1$$

$$Y_2 = wy_1 + wy_2$$

$$z = y_2y_1$$



Present state y_2y_1	Next State w = 0 Y_2Y_1	Next State w = 1 Y_2Y_1	Output z
0 0	0 0	01	0
0 1	0 0	10	0
1 0	0 0	11	0
1 1	0 0	11	1

(a) State-assigned table

Present state	Next state w = 0	Next state w = 1	Output z
A	A	B	0
B	A	C	0
C	A	D	0
D	A	D	1

(b) State table

Figure 8.81. Tables for the circuit in Example 8.80.

Example 2

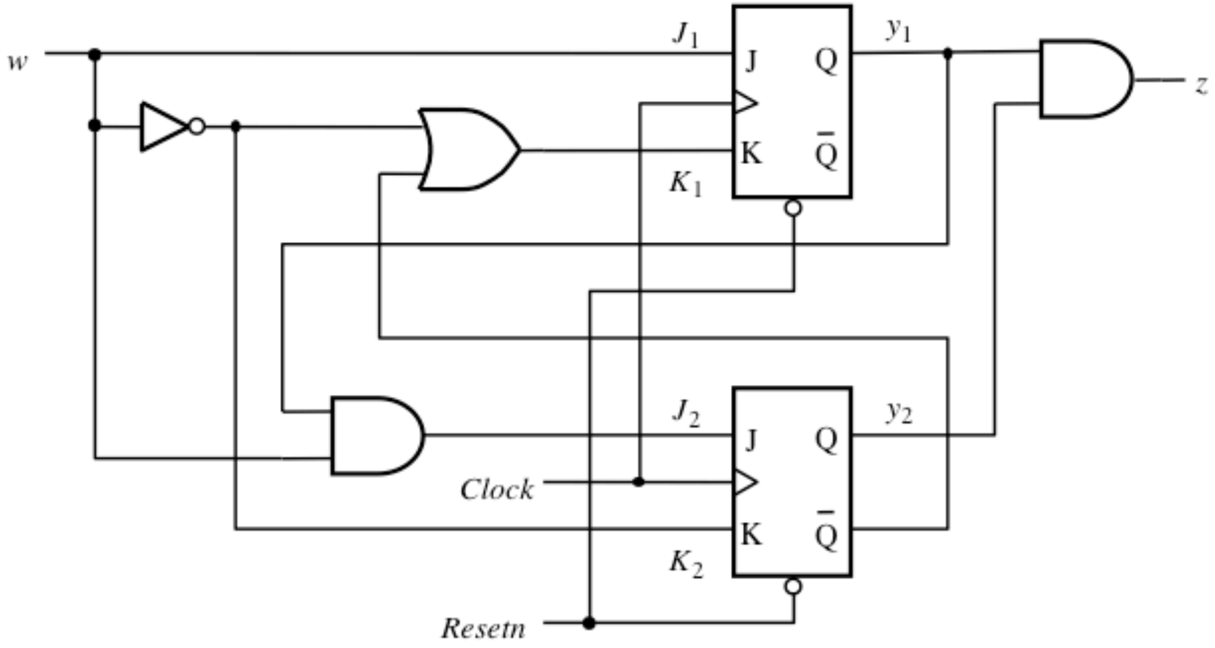


Figure 8.82. Circuit for Example 8.9.

Example 2

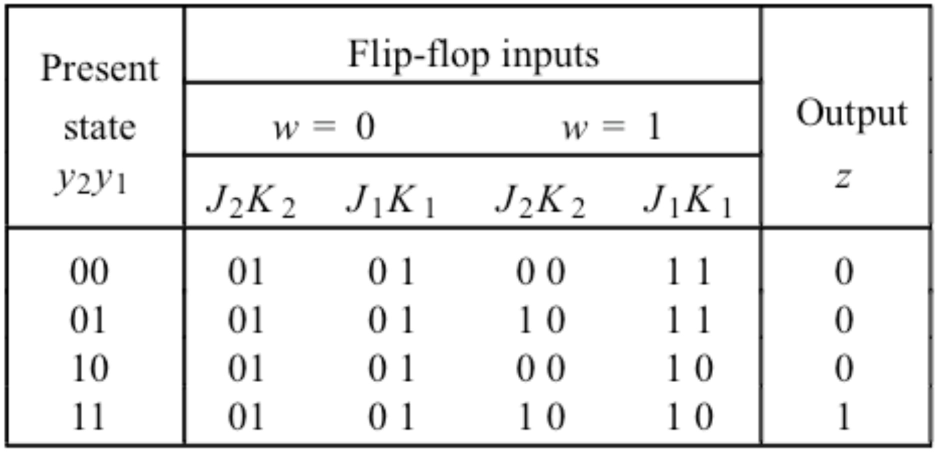
$J_1 = w$

$K_1 = \bar{w} + y_2$

$J_2 = wy_1$

$K_2 = \bar{w}$

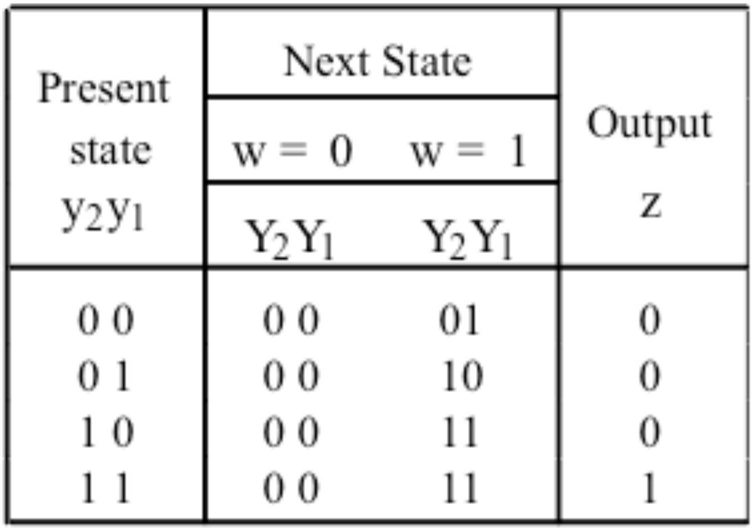
$z = y_2 y_1$



Present state	Flip-flop inputs				Output
	$w = 0$		$w = 1$		
$y_2 y_1$	$J_2 K_2$	$J_1 K_1$	$J_2 K_2$	$J_1 K_1$	z
00	01	0 1	0 0	1 1	0
01	01	0 1	1 0	1 1	0
10	01	0 1	0 0	1 0	0
11	01	0 1	1 0	1 0	1

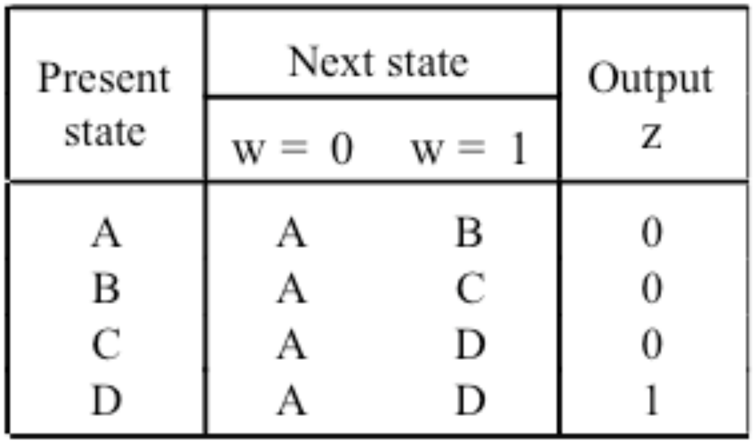
Figure 8.83. The excitation table for the circuit in Figure 8.82.

Example 2



Present state	Next State		Output
	w = 0	w = 1	
y_2y_1	Y_2Y_1	Y_2Y_1	z
0 0	0 0	01	0
0 1	0 0	10	0
1 0	0 0	11	0
1 1	0 0	11	1

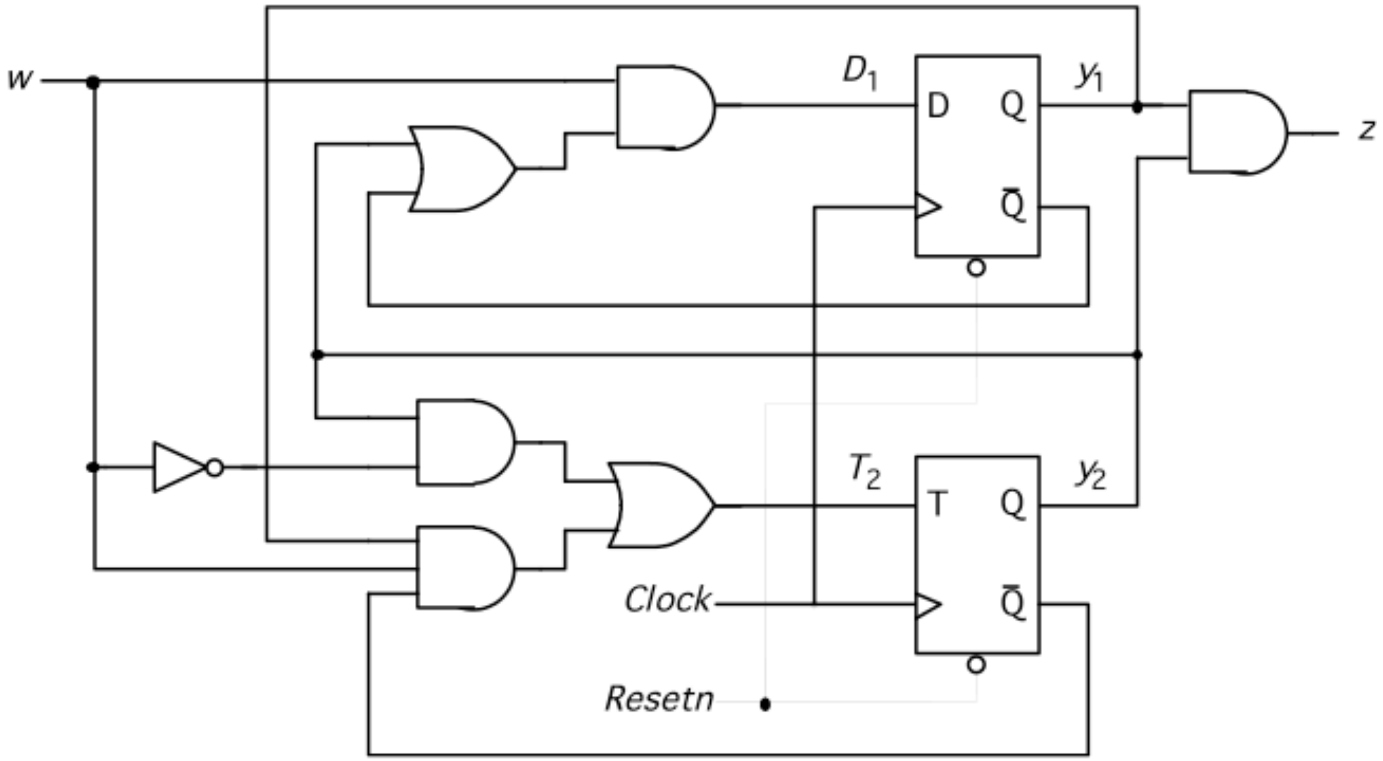
(a) State-assigned table



Present state	Next state		Output z
	w = 0	w = 1	
A	A	B	0
B	A	C	0
C	A	D	0
D	A	D	1

(b) State table

Example 3

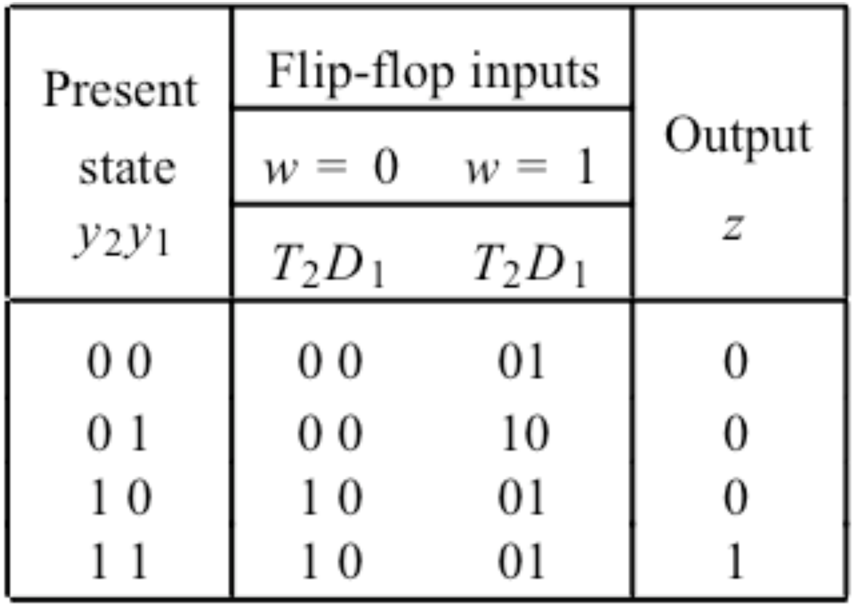


Example 3

$D_1 = w(y_2 + \bar{y}_1)$

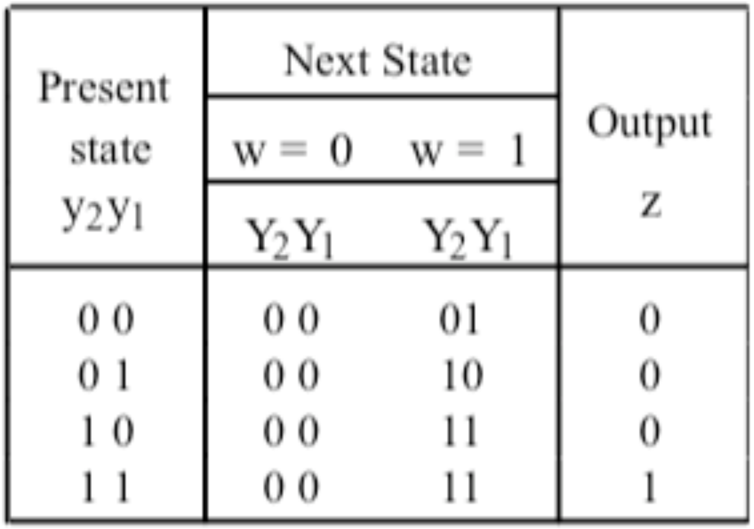
$T_2 = wy_1\bar{y}_2 + \bar{w}y_2$

$z = y_2y_1$



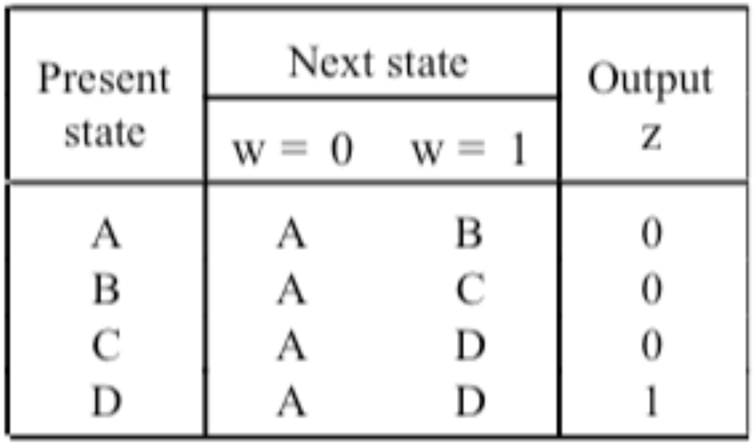
Present state	Flip-flop inputs		Output
	$w = 0$	$w = 1$	
y_2y_1	T_2D_1	T_2D_1	z
0 0	0 0	01	0
0 1	0 0	10	0
1 0	1 0	01	0
1 1	1 0	01	1

Example 3



Present state y_2y_1	Next State		Output z
	$w = 0$	$w = 1$	
	Y_2Y_1	Y_2Y_1	
0 0	0 0	01	0
0 1	0 0	10	0
1 0	0 0	11	0
1 1	0 0	11	1

(a) State-assigned table



Present state	Next state		Output z
	$w = 0$	$w = 1$	
A	A	B	0
B	A	C	0
C	A	D	0
D	A	D	1

(b) State table