Dr. Nicola Nicolici **COE2DI4 Midterm Test #1** *Oct 15, 2007*

Instructions: This examination paper includes 9 pages and 20 multiple-choice questions starting on page 3. You are responsible for ensuring that your copy of the paper is complete. Bring any discrepancy to the attention of your invigilator. The answers for all the questions must be indicated by filling the corresponding circle on the optical scanning (OMR) examination sheet. **This OMR examination sheet is the only page to be handed in.** The instructions for completing the OMR examination sheet are provided on page 2. Read and follow these instructions with care! There is one mark for each question. Answer all questions. There is no penalty for guessing. This is a closed book exam. No reference material of any kind is permitted. No calculators of any kind are permitted. **Time allowed is 50 minutes**.

Note: A' and $\overline{A}$ are used interchangeably.

Continued on page 2

OMR examination instructions

Continued on page 3

Multiple choice questions (numbered 1 to 20) – indicate your answer by filling the corresponding circle on the OMR answer sheet

1. The binary representation of $(-22)_{10}$ with 6 bits in 2's complement format is:

1. $(010110)_2$
2. $(110110)_2$
3. $(101010)_2$
4. $(101001)_2$
5. none of the above

2. The hexadecimal equivalent of the unsigned number represented as $(4444)_8$ in octal is:

1. $(444)_{16}$
2. $(814)_{16}$
3. $(924)_{16}$
4. $(A84)_{16}$
5. $(B22)_{16}$

3. The largest positive number in the sign-magnitude format represented with 12-bits is:

1. $(FFF)_{16}$
2. $(4096)_{10}$
3. $(1777)_8$
4. $(1000\ 0000\ 0000)_2$
5. none of the above

4. The range of numbers that can be represented with 9 bits in 1's complement format is:

1. $(-255)_{10}$ to $(255)_{10}$
2. $(-255)_{10}$ to $(256)_{10}$
3. $(-256)_{10}$ to $(255)_{10}$
4. $(-256)_{10}$ to $(256)_{10}$
5. $(0)_{10}$ to $(511)_{10}$

Continued on page 4

5. Consider the circuit from Figure 1. Function **F** is:

1. **F(A,B)** = AB
2. **F(A,B)** = A'B'
3. **F(A,B)** = AB'
4. **F(A,B)** = A'B
5. none of the above

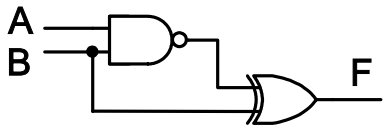

Figure 1 – Circuit for question 5.

6. Function **F(A,B,C,D)** shown in Figure 2 is:

1. $\prod$ **M** (0, 5, 10, 15)
2. $\prod$ **M** (0, 5, 7, 10, 15)
3. $\prod$ **M** (1, 2, 3, 4, 6, 8, 9, 11, 12, 13, 14)
4. $\prod$ **M** (1, 2, 3, 4, 6, 7, 8, 9, 11, 12, 13, 14)
5. none of the above

7. All the prime implicants of **F(A,B,C,D)** shown in Figure 2 are:

1. A'C, AC', A'B'C, A'CD', B'D, BD'
2. AC', A'B'C, A'CD', B'D, BD'
3. AC', A'CD', B'D, BD'
4. AC', A'B'C, B'D, BD'
5. A'C, A'B'C, B'D, BD'

8. All the essential prime implicants of **F(A,B,C,D)** shown in Figure 2 are:

1. AC', A'B'C, A'CD', B'D, BD'
2. AC', A'B'C, B'D, BD'
3. AC', A'CD', B'D, BD'
4. AC', B'D, BD'
5. A'C, B'D, BD'

C D \ A B	00	01	11	10
00	0	1	1	1
01	1	0	1	1
11	1	0	0	1
10	1	1	1	0

Figure 2 - Karnaugh map for function F(A,B,C,D) for questions 6 to 8.

Continued on page 5

C D \ A B	00	01	11	10
00	X	1	1	X
01	X	0	X	1
11	0	X	0	X
10	1	X	X	0

Figure 3 - Karnaugh map for function F(A,B,C,D) for questions 9 and 10. Note, 'X' stands for don't care.

9. Consider the function **F(A,B,C,D)** shown in Figure 3. The simplified logical expression in the sum-of-products (SOP) form (i.e., the minimum number of product terms and the minimum number of literals in every product term) for **F(A,B,C,D)** can be converted into a circuit implementation using NAND gates, which is shown in:

1. Figure 4(a)
2. Figure 4(b)
3. Figure 4(c)
4. Figure 4(d)
5. all of the above

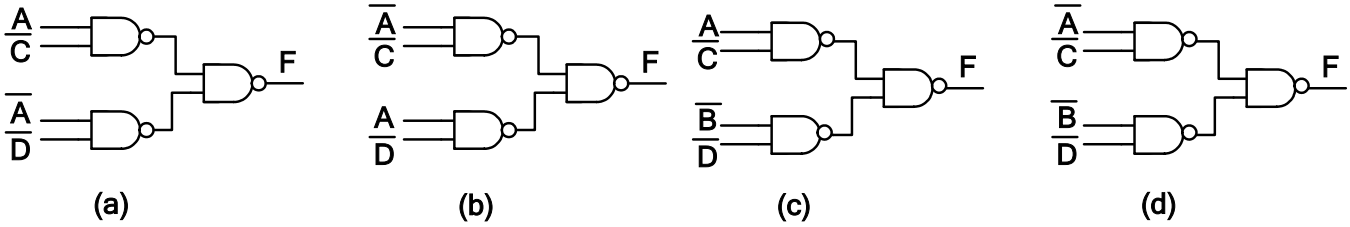

Figure 4 - Implementations for function F(A,B,C,D) for question 9.

10. Consider the function **F(A,B,C,D)** shown in Figure 3. The simplified logical expression in the product-of-sums (POS) form (i.e., the minimum number of sum terms and the minimum number of literals in every sum term) for **F(A,B,C,D)** can be converted into a circuit implementation using NOR gates, which is shown in:

1. Figure 5(a)
2. Figure 5(b)
3. Figure 5(c)
4. Figure 5(d)
5. all of the above

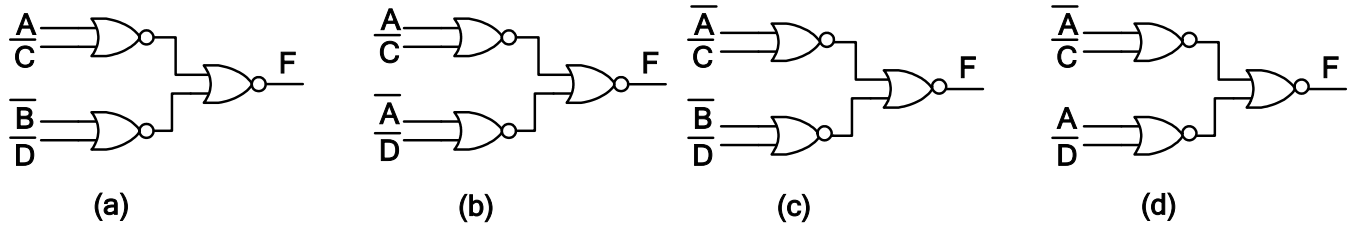

Figure 5 - Implementations for function F(A,B,C,D) for question 10.

Continued on page 6

11. The circuit from Figure 6 is equivalent to the circuit from:

1. Figure 7(a)
2. Figure 7(b)
3. Figure 7(c)
4. Figure 7(d)
5. none of the above

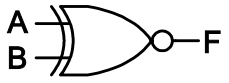

Figure 6 - Circuit for question 11.

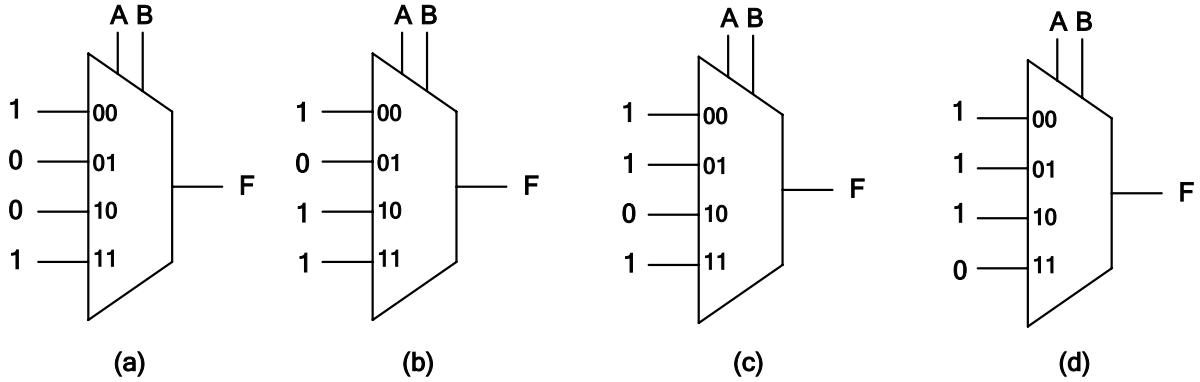

Figure 7 - Circuits for question 11.

12. The circuit from Figure 8 is equivalent to the circuit from:

1. Figure 9(a)
2. Figure 9(b)
3. Figure 9(c)
4. Figure 9(d)
5. none of the above

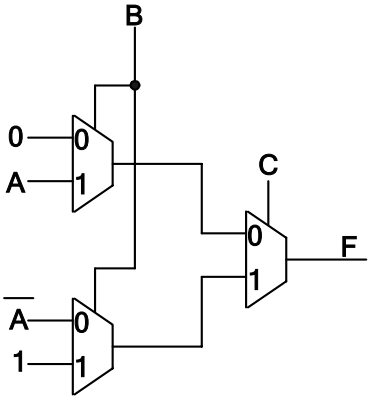

Figure 8 - Circuit for question 12.

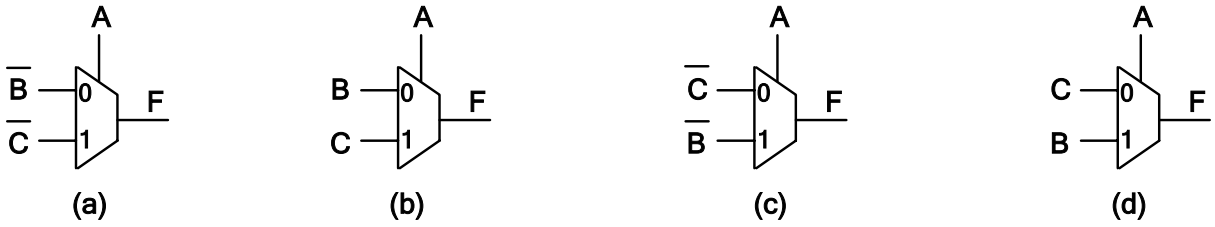

Figure 9 - Circuits for question 12.

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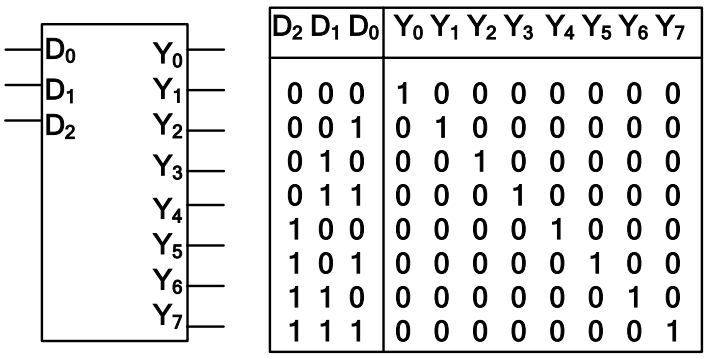
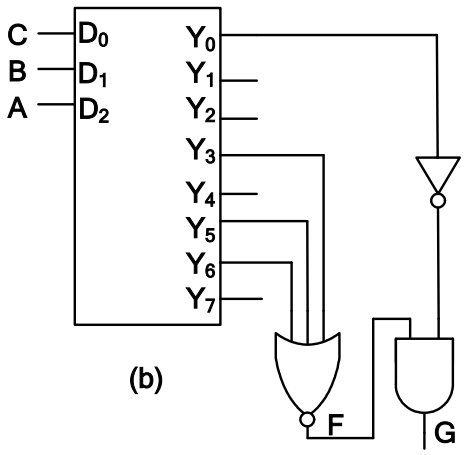


D_2 D_1 D_0	Y_0	Y_1	Y_2	Y_3	Y_4	Y_5	Y_6	Y_7
0 0 0	1	0	0	0	0	0	0	0
0 0 1	0	1	0	0	0	0	0	0
0 1 0	0	0	1	0	0	0	0	0
0 1 1	0	0	0	1	0	0	0	0
1 0 0	0	0	0	0	1	0	0	0
1 0 1	0	0	0	0	0	1	0	0
1 1 0	0	0	0	0	0	0	1	0
1 1 1	0	0	0	0	0	0	0	1

(a)



(b)

Figure 10 - The 3-to-8 decoder without an enable signal for questions 13 and 14.

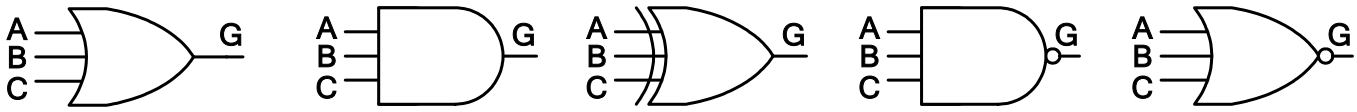
13. In Figure 10(b):

1. **F(A,B,C)** = $\prod$ **M**(3,5)
2. **F(A,B,C)** = Σ **m**(3,5,6)
3. **F(A,B,C)** = $\prod$ **M**(0,1,4,7)
4. **F(A,B,C)** = Σ **m**(0,1,2,4,7)
5. **F(A,B,C)** = $\prod$ **M**(0,1,2,4,5,7)

Note: **For both questions 13 and 14, use the truth table of the 3-to-8 decoder from Figure 10(a).**

14. In Figure 10(b), function **G(A,B,C)** is equivalent to the function shown in:

1. Figure 11(a)
2. Figure 11(b)
3. Figure 11(c)
4. Figure 11(d)
5. Figure 11(e)



(a) (b) (c) (d) (e)

Figure 11 - Circuits for question 14.

15. How many 2-to-4 decoders are used to implement an 8-to-256 decoder?
Note: All the decoders have an enable input and all the inputs and outputs are un-inverted.
Hint**:** It is a hierarchical implementation with more than two levels of 2-to-4 decoders.

1. 5
2. 65
3. 69
4. 73
5. 85

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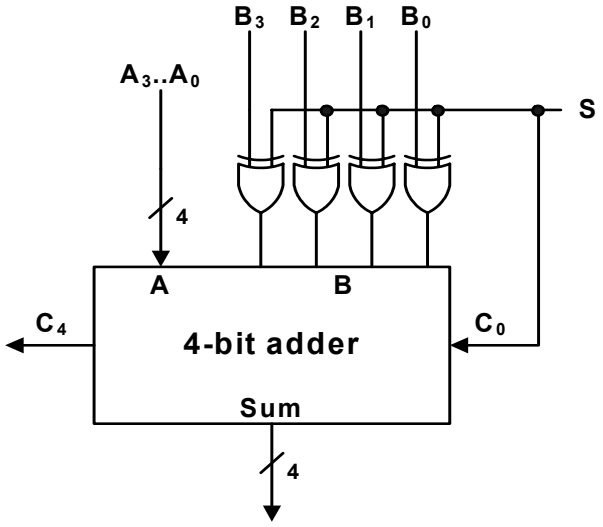

Figure 12 – Circuit for questions 16 and 17. Note, C_0 is carry in and C_4 is carry out for the 4-bit adder.

Reminder: **This adder and subtractor unit operates on 2's complement numbers and the S input signal determines whether an addition or subtraction will occur.**

16. In Figure 12, if $\mathbf{A_3A_2A_1A_0}$=0011, $\mathbf{B_3B_2B_1B_0}$=0111 and **S**=1 then the output is:

1. **Sum**=1100 and $\mathbf{C_4}$=1
2. **Sum**=1100 and $\mathbf{C_4}$=0
3. **Sum**=0100 and $\mathbf{C_4}$=1
4. **Sum**=0100 and $\mathbf{C_4}$=0
5. none of the above

17. In Figure 12, arithmetic overflow occurs for:

1. $\mathbf{A_3A_2A_1A_0}$=0001, $\mathbf{B_3B_2B_1B_0}$=1111 and **S**=1
2. $\mathbf{A_3A_2A_1A_0}$=0001, $\mathbf{B_3B_2B_1B_0}$=1111 and **S**=0
3. $\mathbf{A_3A_2A_1A_0}$=1111, $\mathbf{B_3B_2B_1B_0}$=0111 and **S**=1
4. $\mathbf{A_3A_2A_1A_0}$=1111, $\mathbf{B_3B_2B_1B_0}$=0111 and **S**=0
5. none of the above

18. Consider a 1-bit adder cell with 3 inputs (1-bit operands $\mathbf{A_i}$, $\mathbf{B_i}$ and input carry $\mathbf{C_i}$) and 2 outputs (1-bit sum $\mathbf{S_i}$ and output carry $\mathbf{C_{i+1}}$). Then $\mathbf{C_{i+1}}$ can be implemented as shown in:

1. Figure 13(a)
2. Figure 13(b)
3. Figure 13(c)
4. Figure 13(d)
5. none of the above

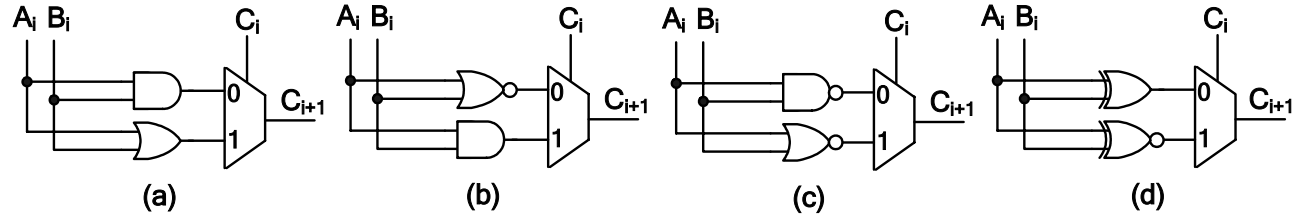

Figure 13 - Implementations for output carry C_{i+1} for question 18.

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19. A 2-to-1 multiplexer illustrated in Figure 14(a) can be implemented using only 2-input NAND gates, as shown in Figure 14(b). Figure 14(c) gives the implementation of a function **f** using an interconnection of three 2-to-1 multiplexers. It is assumed that the 2-input NAND gate's propagation delays from Low to High and High to Low are equal to 5 ns. Then the *longest* propagation delay from *any* input (**$d_3 d_2 d_1 d_0 s_2 s_1 s_0$**) to the output (**f**) from Figure 14(c) is:

1. 25 ns
2. 30 ns
3. 35 ns
4. 40 ns
5. 45 ns

Hint: **Determine the propagation delay to the output of each NAND gate within every 2-to-1 multiplexer.**

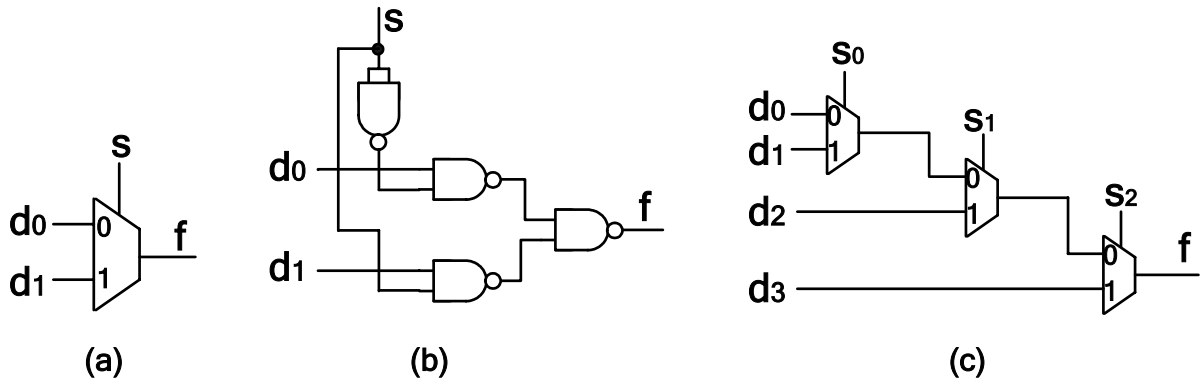

Figure 14 – Multiplexer circuits for question 19.

20. Consider the circuit from Figure 15(a). It is assumed that the 2-input NAND and 2-input XOR gates' propagation delays from Low to High and High to Low are equal to 5 ns. As shown in Figure 15(b), the input signal (**input** from Figure 15(a)) is a periodic signal with a frequency of 25 MHz. Then the output signal (**output** from Figure 15(a)) is a periodic signal and its frequency is:

1. 100 MHz
2. 50 MHz
3. 25 MHz
4. 10 MHz
5. 5 MHz

Hint: **Draw the waveforms on the inputs and the output of the XOR gate.**

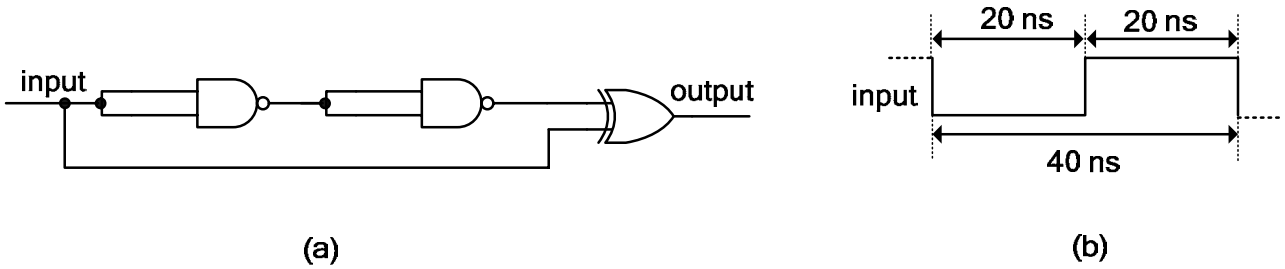

Figure 15 - Circuit for question 20.

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