# Lab #1     Logic Gates

## Objective:

To introduce some basic concepts and laboratory techniques in working with digital logic gates.

## Preparation:

Obtain the data sheets for each of the following TTL devices below.  Familiarize yourself with their logical and electrical characteristics and bring a copy to your lab session.  Read the following experiment and study the circuits as shown.
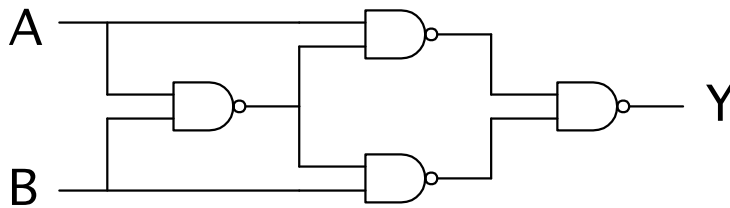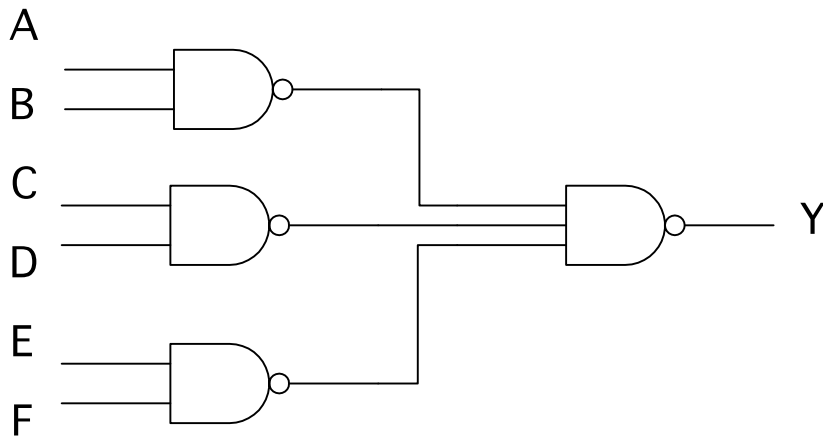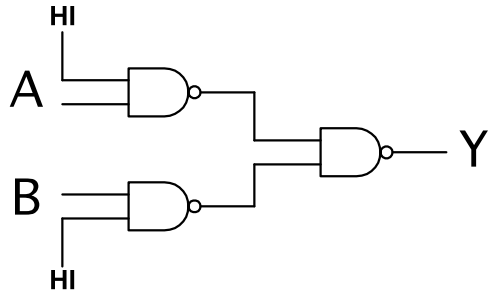
## Devices used:

sn74LS00     2-input NAND
sn74LS04     inverters
sn74LS10     3-input NAND
sn74LS86     2-input XOR

## Experiment:

1.     Connect each of the following circuits and experimentally verify their truth tables using switches for inputs and LEDs for outputs). State their equivalent logic function and draw the truth tables beside each circuit.

A

B

Y

A
B

C
D

E
F

Y

A

B

Y
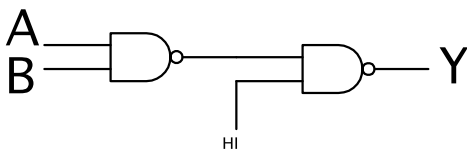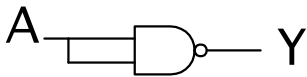
2.     The output of the 2-input XOR gate is HI when its inputs are different and LO otherwise.  Verify the truth table for the XOR gate and explain how it could also be considered to be a "controllable inverter".

A
B

Y
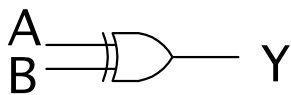
3.      Parity generator

        Parity bits are commonly used to detect errors in serial communications and memory accesses.  A binary number is said to have odd parity if the number of 1's contained in it is odd; it has even parity when the number of 1's is even.  This may be detected using XOR gates.  Build the following circuit to verify that its output Y is HI when the parity of the input word ABCD is odd and LO otherwise.  Draw the corresponding truth table.
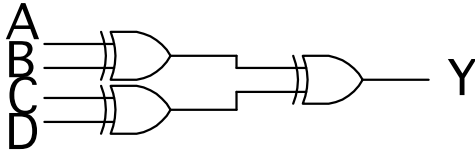
4.      Equality detector

        The equality of two bits can be indicated with the XNOR (sometimes called a "coincidence gate").  Verify this by examining the truth table of the XNOR.  For testing the equality of multi-bit numbers, corresponding bits from each number may be compared using an XNOR gate, and the results of each of these AND'ed together.

Build a circuit to implement the following logic and verify that its output Y is HI only when 3-bit inputs ABC and PQR are equal.
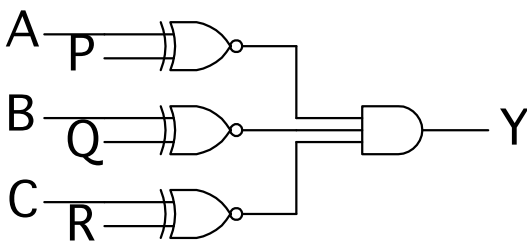
Note:  this idea is readily extended to produce a circuit that compares the magnitude of input numbers.  For example the SN74LS85 takes two 4-bit inputs A and B, and produces three outputs that indicate A=B, A>B or A<B.

5.      Half adder

        The fundamental circuit for computer arithmetic is the *half adder* as shown
below.  The output S is the sum of inputs A and B and the output $C_{out}$ indicates when a
carry is generated.  Build the circuit and verify its truth table.
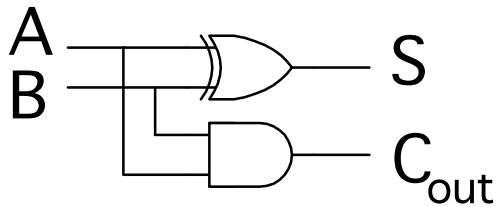


6.      Full adder

        The *full adder* is the combination of two half adders to produce a sum output S
and a carry output $C_{out}$ as a function of inputs A, B and $C_{in}$.  This allows implementation
of fast, parallel addition of multiple bit numbers and is the basis for other arithmetic
functions including subtraction, multiplication and division.  Construct the circuit shown
below and verify its truth table using switches and LEDs.

Leave this circuit connected, as you will use it again in the next part.
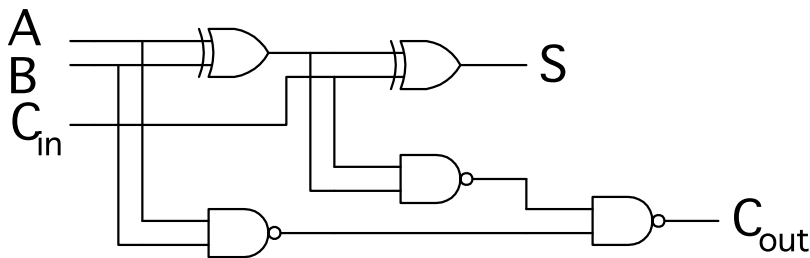


## Note:

*In the following exercises, we will use the digital oscilloscope to measure some electrical
properties of LS TTL logic gates.  To begin, set the output of the function generator to
produce a 100KHz square wave, 5V peak-to-peak iin magnitude with 2.5v DC offset.
This gives a waveform with a minimum of 0V and a maximum of +5v.  **Carefully** verify
this output on the oscilloscope and do not proceed until <u>this is checked by a lab
demonstrator</u>.  TTL inputs must **never** exceed 5V !*

7.      Dynamic behavior of full adder

Disconnect the switch from the A input to the full adder and replace with the square wave output from the function generator.  Observe the output on S and $C_{out}$ for various combinations of inputs on B and $C_{in}$.

Carefully explain what you observe at $C_{out}$ for the case when $B = C_{in} = HI$.

8.      Measure gate delay using pulse generator

Gate propagation delays can be used to advantage to generate a short pulse (when this is done inadvertently, it is called a "glitch" and can be the source of frustrating problems as we saw in the previous part of this lab ! ).  Build the circuit as shown below and apply the square wave to the clock input and display this on channel 1.  Display the output Y of the NAND gate on channel 2 and explain the result.  Note carefully the location of the pulse at Y relative to the edges of the input waveform.



Odd # of inverters
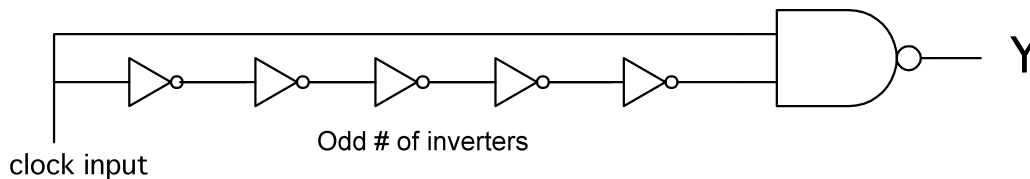
clock input

*sketch clock input and waveform at Y  here:*

Using this waveform, what would you estimate for $t_{pd}$?      _____

Vary the number of inverters in the circuit and observe the affect.

Replace the NAND gate in this circuit with an XOR gate and explain the observed output.

Sketch the output you would *expect* to see if the NAND in the original circuit were replaced with a NOR gate ( you are not required to actually modify the circuit ).

*sketch clock input and waveform at Y  here:*

9.      Measure gate delay using oscillator

Connect a series of 4 inverters plus a NAND gate as shown below and display the output on the scope.  An odd number of inversions back-to-back will produce an oscillator whose period will be equal to twice the delay through the chain.



Enable (HI)

output

Even # of inverters
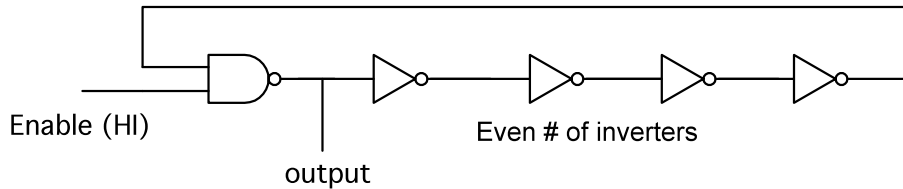
Measure the time for 1/2 of one cycle of this circuit using the automatic measurement functions of the 'scope.  _____

How does this compare to parameters $t_{PLH}$ and $t_{PHL}$ from the sn74LS00 data sheet ?

$t_{PLH}$ =  _____

$t_{PHL}$ =  _____

10.     Verify TTL levels

For *input* to a TTL gate, voltages from 0 to 0.8 V are taken as logical LO.  Input voltages between 2.0 and 5.0 are considered logical HI.  Voltages between 0.8V and 2.0V are indeterminate.  These ranges are slightly different for TTL outputs to allow some noise margin.

Change the output of the function generator to a 100KHz triangular wave, again carefully verifying that it is 5V peak-to-peak with 2.5V DC offset using the 'scope.  Apply this triangular waveform to from the function generator to the NAND gate input as shown below.  Display this on channel 1 of the 'scope and show the output of the NAND gate on channel 2.



HI

Triangular wave input

Y
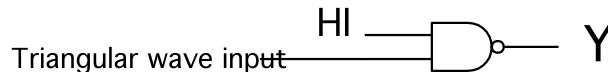
 Using the automatic measuring functions of the digital 'scope, at what input voltage level does the output of the NAND change ?      _____