Name: _____ Student # : _____ Signature: _____

Dr. S. Shirani **CoE2DI4 Midterm Test #1** *Oct. 15, 2008*

Instructions: This examination paper includes 9 pages and 20 multiple-choice questions starting on page 3. You are responsible for ensuring that your copy of the paper is complete. Bring any discrepancy to the attention of your invigilator. The answers for all the questions must be indicated by filling the corresponding circle on the optical scanning (OMR) examination sheet. **This OMR examination sheet is the only page to be handed in.** The instructions for completing the OMR examination sheet are provided on page 2. Read and follow these instructions with care! There is one mark for each question. Answer all questions. There is no penalty for guessing. This is a closed book exam. No reference material of any kind is permitted. No calculators of any kind are permitted. **Time allowed is 50 minutes**.

Note: A' and $\overline{A}$ are used interchangeably.

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OMR instructions

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Multiple choice questions (numbered 1 to 20) – indicate your answer by filling the corresponding circle on the OMR answer sheet

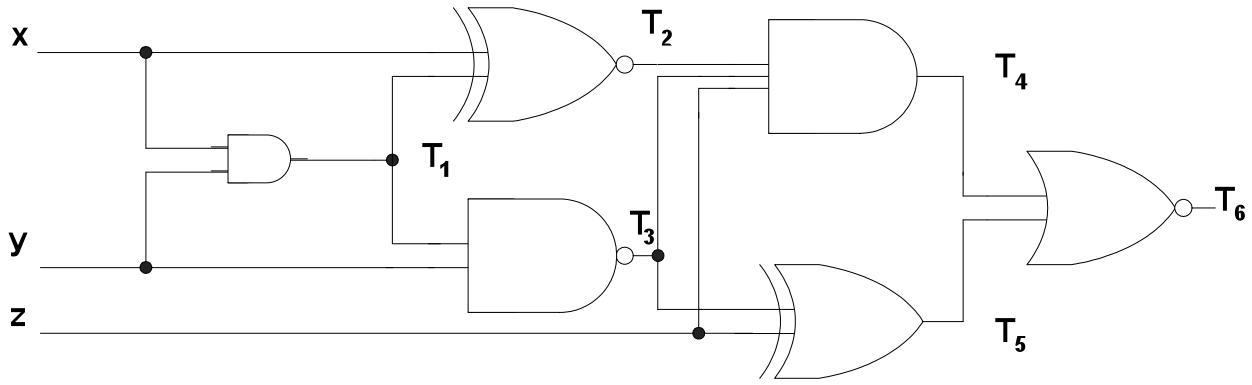

Figure 1- Circuit for question 1.

1. If input z=1 then the logic function at point $\mathbf{T_6}$ of the circuit from Figure 1 is:

1. x'
2. x+y'
3. x'+y
4. x'+y'
5. none of the above

2. Which of the following equations is correct?

1. $x \oplus y = (x \uparrow y') \uparrow (x' \uparrow y)$
2. $x \oplus y = (x \uparrow (x \uparrow y)) \uparrow ((x \uparrow y) \uparrow y)$
3. $x \oplus y = (x \downarrow y) \downarrow (x' \downarrow y')$
4. 1 and 2
5. 1 and 2 and 3

3. Function **F(A,B,C,D)** shown in Figure 2 is:

1. **F(A,B,C,D) = Σ m** (0,1,2,3,4,5,6,7,8,9,10,11,12,13,14,15)
2. **F(A,B,C,D) = Σ m** (1,7,8,10,12,14)
3. **F(A,B,C,D) = Σ m** (1,5,6,7,12,14)
4. **F(A,B,C,D) = Σ m** (1,5,6,7,8,10)
5. none of the above

4. Function **F(A,B,C,D)** shown in Figure 2 is:

1. **F(A,B,C,D) = ∏ M** (0,1,2,3,4,5,6,7,8,9,10,11,12,13,14,15)
2. **F(A,B,C,D) = ∏ M** (0,2,3,4,8,9,10,11,13,15)

Continued on page 4

3. **F(A,B,C,D)** = $\prod$ **M** (0,1,2,3,4,8,9,10,11,13)
4. **F(A,B,C,D)** = $\prod$ **M** (0,1,2,3,4,6,8,9,11,13)
5. none of the above

5. All the prime implicants of **F(A,B,C,D)** shown in Figure 2 are:

1. A'BC, A'BD, A'C'D, ABD', BCD'
2. A'BC, A'C'D, ABD', BCD'
3. A'BC, A'C'D, ABD'
4. A'C'D, ABD'
5. none of the above

6. All the essential prime implicants of **F(A,B,C,D)** shown in Figure 2 are:

1. A'BC, A'BD, A'C'D, ABD', BCD'
2. A'BC, A'C'D, ABD', BCD'
3. A'BC, A'C'D, ABD'
4. A'C'D, ABD'
5. none of the above

C D \ A B	00	01	11	10
00	0	0	1	0
01	1	1	0	0
11	0	1	0	0
10	0	1	1	0

Figure 2 - Karnaugh map for a logic function F(A,B,C,D) for questions 3 to 6.

7. The binary representation of $(-17)_{10}$ with 8 bits in 2's complement format is:

1. $(1000\ 0001)_2$
2. $(1000\ 1110)_2$
3. $(1110\ 1111)_2$
4. $(1111\ 0010)_2$
5. $(1111\ 0001)_2$

8. The hexadecimal equivalent of $(124)_{10}$ is:

1. $(7A)_{16}$
2. $(7B)_{16}$
3. $(7C)_{16}$
4. $(7D)_{16}$
5. $(7E)_{16}$

Continued on page 5

9. The octal equivalent of $(7C)_{16}$ is:

1. $(172)_8$
2. $(174)_8$
3. $(176)_8$
4. $(372)_8$
5. $(374)_8$

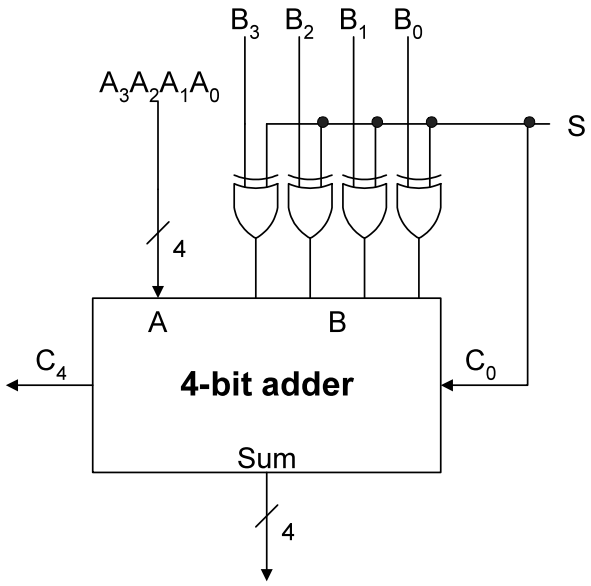

Figure 3 - Circuit for questions 10 to 13. Note, c_0 is carry in and c_4 is carry out for the 4-bit adder.

Reminder: **This adder and subtractor unit operates on 2's complement numbers and the S input signal determines whether an addition or subtraction will occur.**

10. In Figure 3, if $A_3A_2A_1A_0$=0111, $B_3B_2B_1B_0$=1000 and S=0 then the output is:

1. Sum = 0000 and C_4 = 0
2. Sum = 0000 and C_4 = 1
3. Sum = 1111 and C_4 = 0
4. Sum = 1111 and C_4 = 1
5. none of the above

11. In Figure 3, if $A_3A_2A_1A_0$=1001, $B_3B_2B_1B_0$=1001 and S=1 then the output is:

1. Sum = 0000 and C_4 = 0
2. Sum = 0000 and C_4 = 1
3. Sum = 1111 and C_4 = 0
4. Sum = 1111 and C_4 = 1
5. none of the above

12. In Figure 3 overflow occurs for:

1. $A_3A_2A_1A_0$=0111, $B_3B_2B_1B_0$=1000 and S=0
2. $A_3A_2A_1A_0$=0111, $B_3B_2B_1B_0$=1001 and S=0

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3. $A_3A_2A_1A_0$=1001, $B_3B_2B_1B_0$=1000 and S=1
4. $A_3A_2A_1A_0$=1001, $B_3B_2B_1B_0$=1001 and S=1
5. none of the above

13. In Figure 3, detecting a zero result can be achieved by connecting the output Sum to a:

1. 4-input NAND gate
2. 4-input AND gate
3. 4-input XOR gate
4. 4-input XNOR gate
5. none of the above

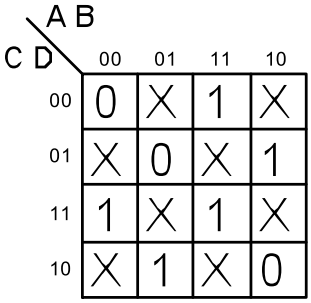
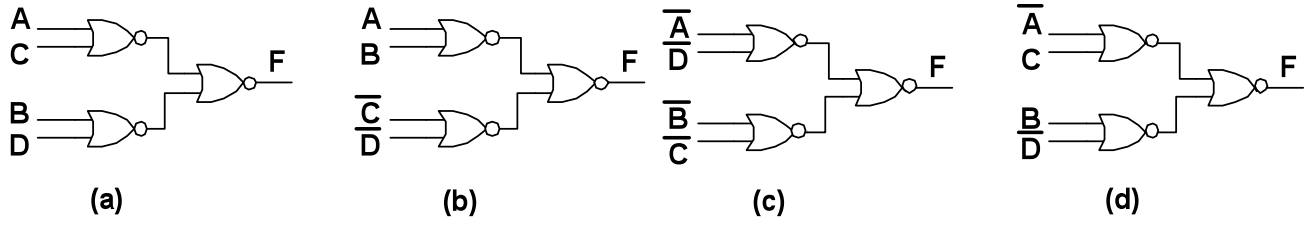


Figure 4 - Karnaugh map for a logic function F(A,B,C,D) for question 14. Note, 'X' stands for don't care.

14. Consider the function F(A,B,C,D) shown in Figure 4. The simplified logical expression in the product-of-sums (POS) form (i.e., the minimum number of sum terms and the minimum number of literals in every sum term) for F(A,B,C,D) can be converted into a circuit implementation using only NOR gates, which is shown in:

1. Figure 5(a)
2. Figure 5(b)
3. Figure 5(c)
4. Figure 5(d)
5. none of the above



15. Which of the circuits shown in Figure 6 are equivalent (i.e., the logic functions they implement have identical truth tables)?

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1. Figure 6(a) and Figure 6(c)
2. Figure 6(a) and Figure 6(d)
3. Figure 6(b) and Figure 6(c)
4. Figure 6(b) and Figure 6(d)
5. none of the above

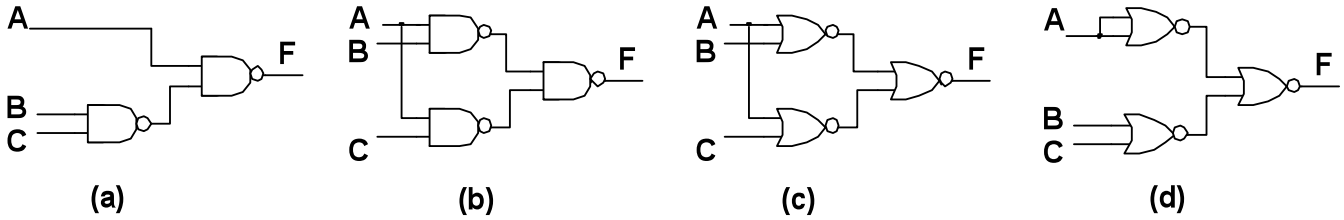

Figure 6 - Circuits function for question 15

16. Consider the logic gate implementation of a 2-bit carry look-ahead adder circuit shown in Figure 7. It is assumed that all the propagation delays (i.e., both low to high and high to low) for all the logic gates shown in Figure 7 (i.e., 2 and 3 input AND, 2 and 3 input OR and 2 input XOR) are equal to 10 ns. If all the inputs (a_1, a_0, b_1, b_0 and c_0) have been updated at the same time, then the correct values of signals s_1 and c_2 can be observed as follows:

1. **s_1** after 10 ns and **c_2** after 20 ns
2. **s_1** after 30 ns and **c_2** after 30 ns
3. **s_1** after 30 ns and **c_2** after 40 ns
4. **s_1** after 40 ns and **c_2** after 20 ns
5. **s_1** after 40 ns and **c_2** after 30 ns

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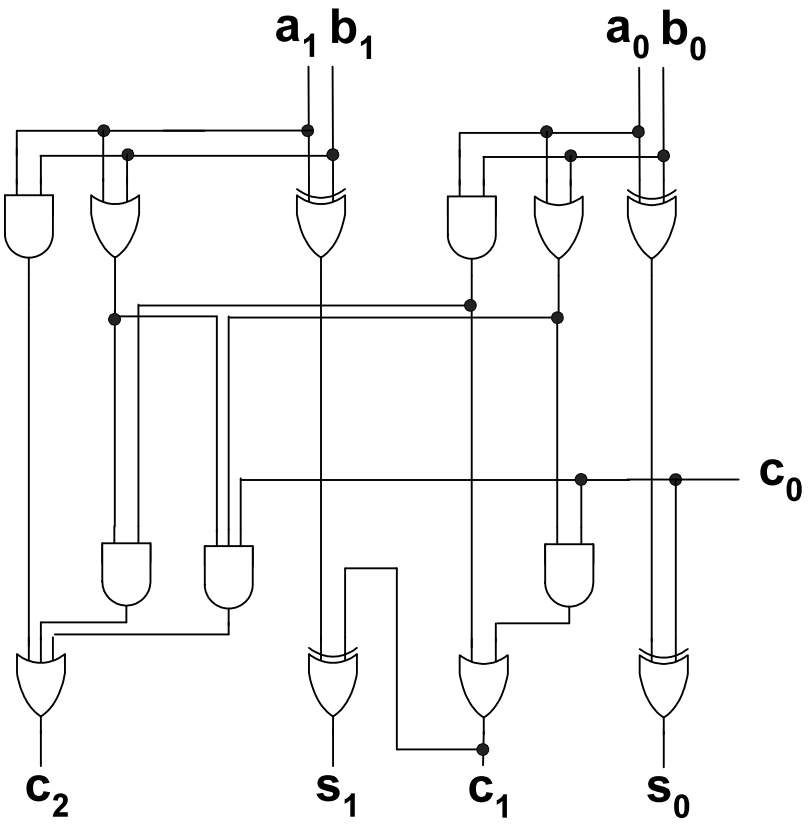

Figure 7- Carry look-ahead adder circuit for question 16

17. A four-variable logic function **F(A,B,C,D)** equals to 1 if input **A** is identical to input **B** and if input **C** is different from input **D**. Function **F(A,B,C,D)** can be written as:

1. **F(A,B,C,D)** = Σ **m** (4,7)
2. **F(A,B,C,D)** = Σ **m** (8,11)
3. **F(A,B,C,D)** = ∏ **M**(0,1,2,3,5,6,10,11,12,13,14,15)
4. **F(A,B,C,D)** = ∏ **M**(0,3,4,5,6,7,8,9,10,11,12,15)
5. none of the above

18. A four-variable logic function **F(A,B,C,D)** equals to 1 if the number of input signals equal to 1 is greater than or equal to the number of input signals equal to 0. Function **F(A,B,C,D)** can be written as:

1. **F(A,B,C,D)** = Σ **m** (3,5,6,7,11,12,13,14,15)
2. **F(A,B,C,D)** = Σ **m** (3,5,6,7,13,14,15)
3. **F(A,B,C,D)** = ∏ **M**(0,1,2,4,8,10)
4. **F(A,B,C,D)** = ∏ **M**(0,1,2,4,8)
5. none of the above

19. Consider a combinational logic system that determines if a 4-bit binary quantity A, B, C, D in the range of 0000 (0) through 1100 (12 in base 10) is divisible by the decimal numbers six. That is, the function is true if the input can be divided by six with no remainder. Assume that the binary patterns 1101 (13) through 1111 (15) are "don't cares." Tread the values as unsigned. Minimized Sum of Products form of this function is:

1. A'B'C'D' + A'BCD'
2. A'B'+BD
3. A'B'C'D'+BCD'
4. AB+BCD'+A'B'C'D'
5. None of the above

20. A self-dual logic function is a function that is identical to its dual. Which of the following functions are self dual?

1. **F = A**
2. **F(A,B,C)** = **Σ m** (0,3,5,6)
3. **F = AB' + A'B**
4. 1 and 2
5. 1 and 2 and 3

"THE END"