Dr. Shahram Shirani **COE2DI4 Midterm Test #2** *Nov 19, 2008*

Instructions: This examination paper includes 13 pages and 20 multiple-choice questions starting on page 3. You are responsible for ensuring that your copy of the paper is complete. Bring any discrepancy to the attention of your invigilator. The answers for all the questions must be indicated by filling the corresponding circle on the optical scanning (OMR) examination sheet. **This OMR examination sheet is the only page to be handed in.** The instructions for completing the OMR examination sheet are provided on page 2. Read and follow these instructions with care! There is one mark for each question. Answer all questions. There is no penalty for guessing. This is a closed book exam. No reference material of any kind is permitted. No calculators of any kind are permitted. **Time allowed is 50 minutes**.

Note: A' and $\overline{A}$ are used interchangeably.

Continued on page 2

OMR examination instructions

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Multiple choice questions (numbered 1 to 20) – indicate your answer by filling the corresponding circle on the OMR answer sheet

1. Consider function **G(A,B,C)=AB+BC**. Let **F(A,B,C)** be the dual of **G(A,B,C)**. Then **F(A,B,C)** can be implemented using **A** as the select (control) input to a 2-to-1 multiplexer. The correct implementation of **F(A,B,C)** is shown in:

1. Figure 1(a)
2. Figure 1(b)
3. Figure 1(c)
4. Figure 1(d)
5. none of the above

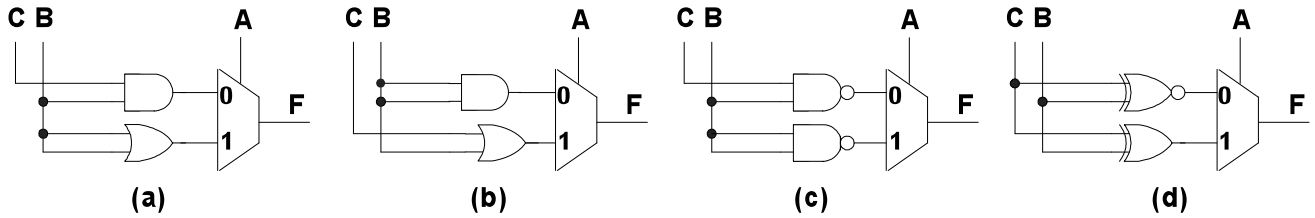

Figure 1 - Implementations for function F(A,B,C) for question 1.

2. Function **F(A,B,C**)= Σ **m**(1,3,4,5) can be implemented using **B** and **C** as the select (control) inputs to a 4-to-1 multiplexer. The correct implementation is shown in:

1. Figure 2(a)
2. Figure 2(b)
3. Figure 2(c)
4. Figure 2(d)
5. none of the above

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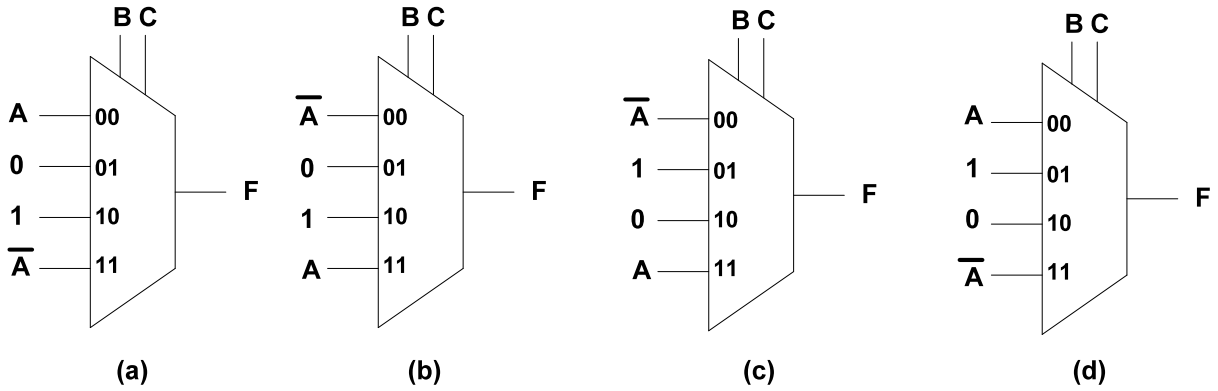
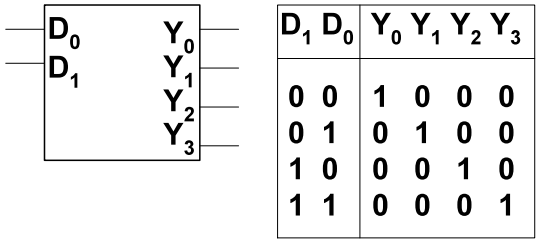
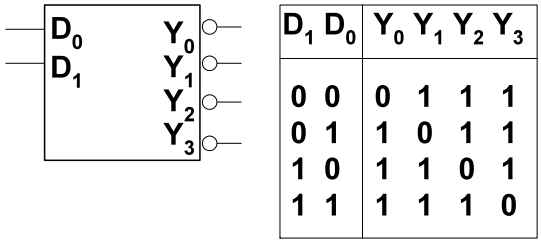


Figure 2 - Implementations for function F(A,B,C) for question 2.



D_1	D_0	Y_0	Y_1	Y_2	Y_3
0	0	1	0	0	0
0	1	0	1	0	0
1	0	0	0	1	0
1	1	0	0	0	1

(a) Decoder with un-inverted outputs



D_1	D_0	Y_0	Y_1	Y_2	Y_3
0	0	0	1	1	1
0	1	1	0	1	1
1	0	1	1	0	1
1	1	1	1	1	0

(b) Decoder with inverted outputs

Figure 3 - Block diagrams and truth tables for decoders without an enable signal for questions 3 and 4

3. The circuit shown in Figure 4 is:

1. **F(A,B,C,D)** = Σ **m**(0,1,2,3)
2. **F(A,B,C,D)** = Σ **m**(0,3,12,15)
3. **F(A,B,C,D)** = Σ **m**(0,4,8,12)
4. **F(A,B,C,D)** = Σ **m**(0,5,10,15)
5. none of the above

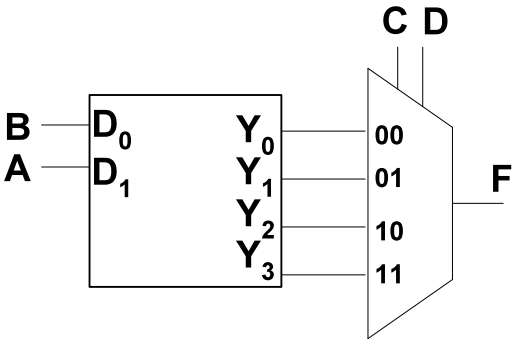


Figure 4 – Circuit for question 3. Use the truth table of the decoder with un-inverted outputs shown in Figure 3(a).

Continued on page 5

4. The circuit shown in Figure 5 is:

1. **F(A,B,C,D)** = ∏ **M**(0,2,13,15)
2. **F(A,B,C,D)** = ∏ **M**(0,4,11,15)
3. **F(A,B,C,D)** = ∏ **M** (0,5,10,15)
4. **F(A,B,C,D)** = ∏ **M** (0,7,8,15)
5. none of the above

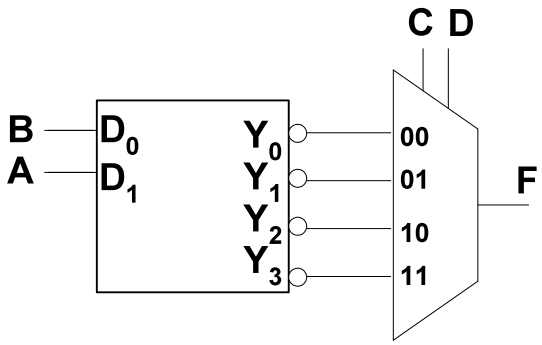


Figure 5 – Circuit for question 4. Use the truth table of the decoder with inverted outputs shown in Figure 3(b).

5. The circuit from Figure 6 is equivalent to the circuit from:

1. Figure 7(a)
2. Figure 7(b)
3. Figure 7(c)
4. Figure 7(d)
5. none of the above

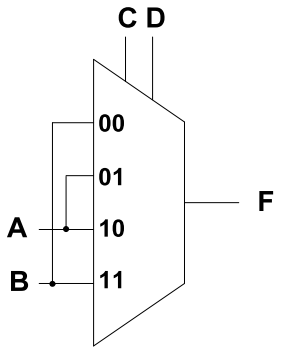


Figure 6 - Circuit for question 5.

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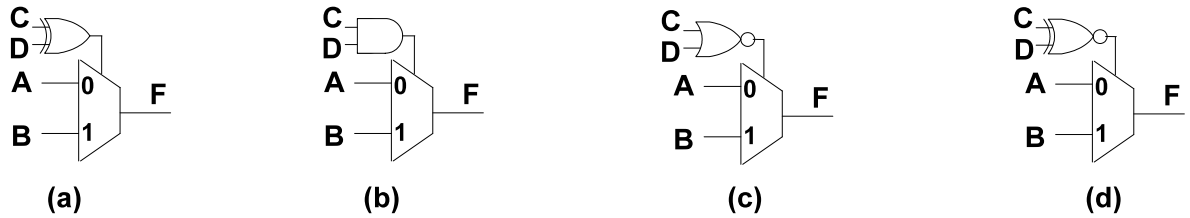

Figure 7 - Circuits for question 5.

6. A Moore machine has one input and one output. The output should be 1 if the total number of 0s received at the input is odd and the total number of 1s received is an even number greater than 0. This machine can be implemented in how many states?

1. 3
2. 4
3. 5
4. 6
5. 8

7. A flip-flop has a 3-ns delay from the time the clock edge occurs to the time the output is complemented. What is the maximum frequency that a 10-bit binary ripple counter that uses this flip-flop can operate with reliability?

1. 10 MHz
2. 20 MHz
3. 25 MHz
4. 30 MHz
5. 33 MHz

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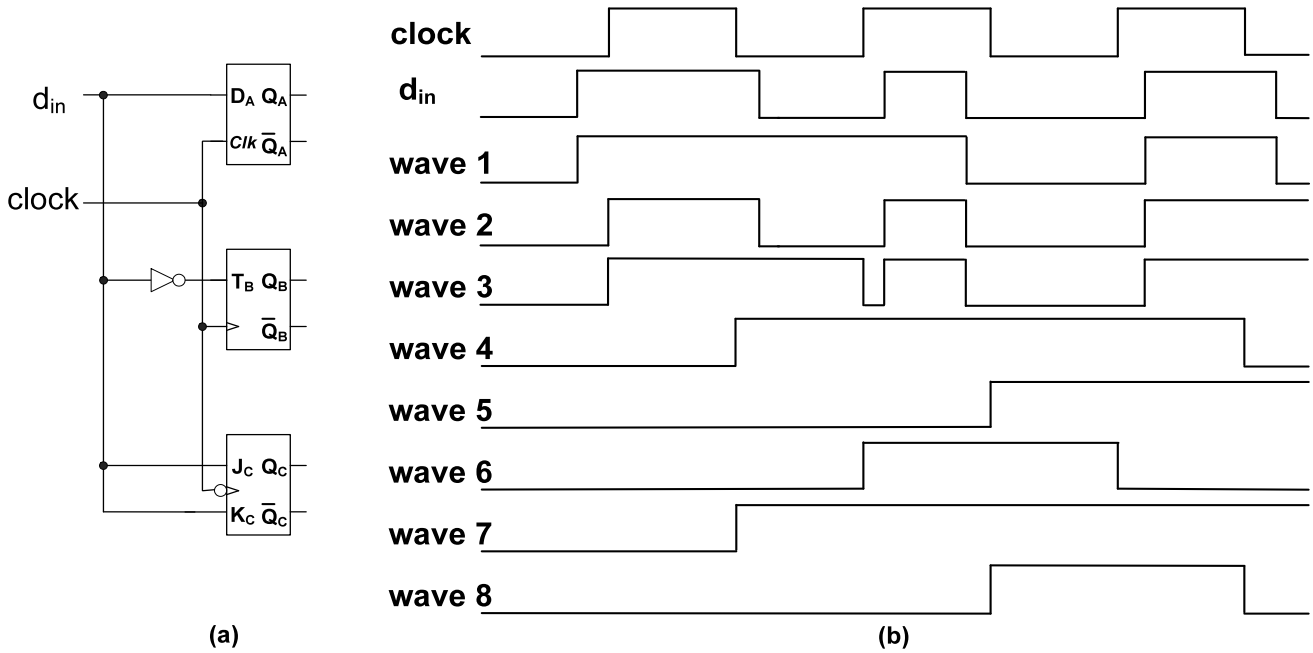

Figure 8 - Sequential (or storage) elements and signal waveforms for questions 8, 9 and 10. Note, the initial value of all the storage elements is zero and they are assumed to be ideal, i.e., the propagation delays and setup/hold times are considered to be zero.

8. Given the **clock** and $\mathbf{d_{in}}$ waveforms in Figure 8(b) the waveform for $\mathbf{Q_A}$ from Figure 8(a) is:

1. wave 1 from Figure 8(b)
2. wave 2 from Figure 8(b)
3. wave 3 from Figure 8(b)
4. wave 4 from Figure 8(b)
5. wave 5 from Figure 8(b)

9. Given the **clock** and $\mathbf{d_{in}}$ waveforms in Figure 8(b) the waveform for $\mathbf{Q_B}$ from Figure 8(a) is:

1. wave 4 from Figure 8(b)
2. wave 5 from Figure 8(b)
3. wave 6 from Figure 8(b)
4. wave 7 from Figure 8(b)
5. wave 8 from Figure 8(b)

10. Given the **clock** and $\mathbf{d_{in}}$ waveforms in Figure 8(b) the waveform for $\mathbf{Q_C}$ from Figure 8(a) is:

1. wave 4 from Figure 8(b)
2. wave 5 from Figure 8(b)
3. wave 6 from Figure 8(b)
4. wave 7 from Figure 8(b)
5. wave 8 from Figure 8(b)

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11. In Figure 9, if the current state is $Q_3Q_2Q_1Q_0$=1101, then after the next *positive edge* of the ***clock*** signal the new state will be:

1. 0000
2. 1111
3. 0111
4. 0011
5. 0001

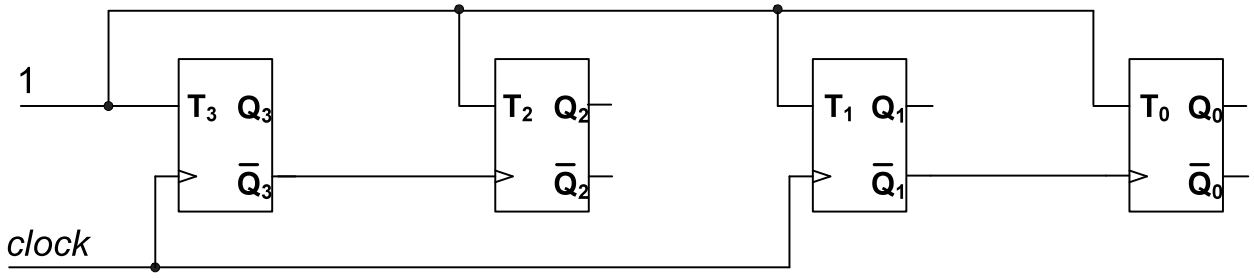

Figure 9 - Circuit for question 11 (note, the flip-flops are *positive edge* triggered).

<u>Note for question 11:</u> Because NOT all the flip-flops' clock inputs share the same *clock* signal, it is considered that the new state value will be observed only when all the flip-flops' outputs have become stable, i.e., after *all* the events triggered by the *positive edge* of the *clock* signal have been completed.

12. The periodic sequence $Q_2Q_1Q_0$ generated by the circuit shown in Figure 10 is:

1. 000, 111, 011, 010, 101
2. 000, 111, 011, 101
3. 000, 111, 101
4. 000, 111
5. none of the above

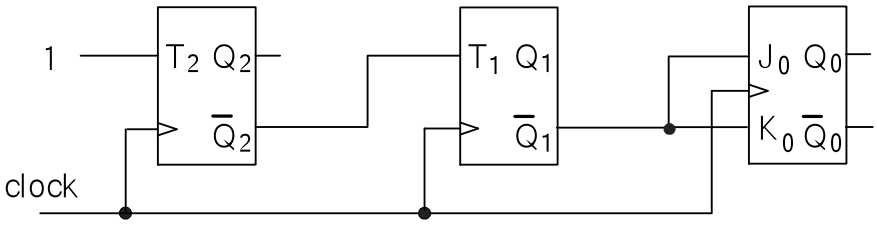

Figure 10 - Circuit for question 12 (it is assumed that after power up the state is 000).

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13. Using a synchronous 3-bit *up counter* with parallel load capability (**Q_2** and **D_2** are the most significant bits) the circuit shown in Figure 11 generates the following periodic sequence:

1. 0, 2, 3, 4, 6, 7
2. 0, 2, 3, 4, 6
3. 0, 2, 3, 4
4. 0, 2, 4
5. 0, 4

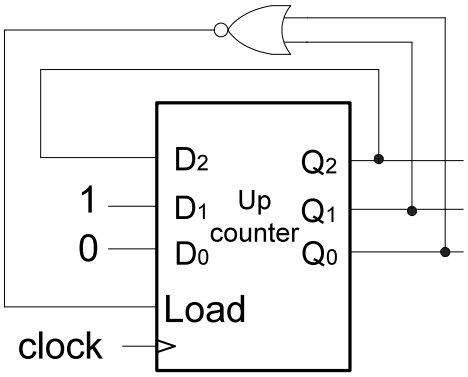


Figure 11– Circuit for question 13 (it is assumed that after power up the state is 000).

14. Figure 12 shows a frequency division circuit implemented using a synchronous 4-bit *up-counter* with parallel load capability capability (**Q_3** and **D_3** are the most significant bits). If the frequency of the ***clock*** signal is 60 MHz, then signal ***z***, which is a periodic signal, has its frequency equal to:

1. 20 MHz
2. 15 MHz
3. 12 MHz
4. 10 MHz
5. 6 MHz

<u>Tip for question 14:</u> To compute the frequency of signal *z*, you must derive the periodic sequence generated by the circuit from Figure 12.

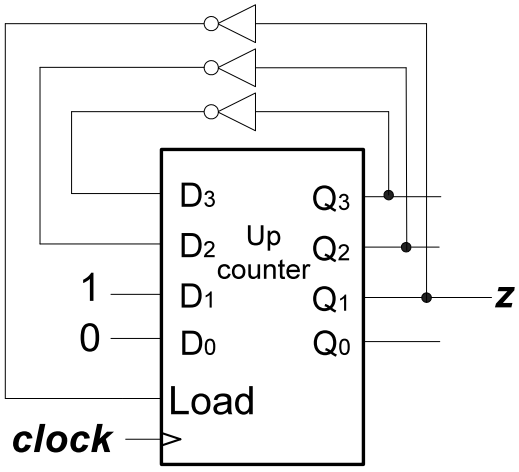


Figure 12 – Circuit for question 14 (it is assumed that after power up the state is 1010).

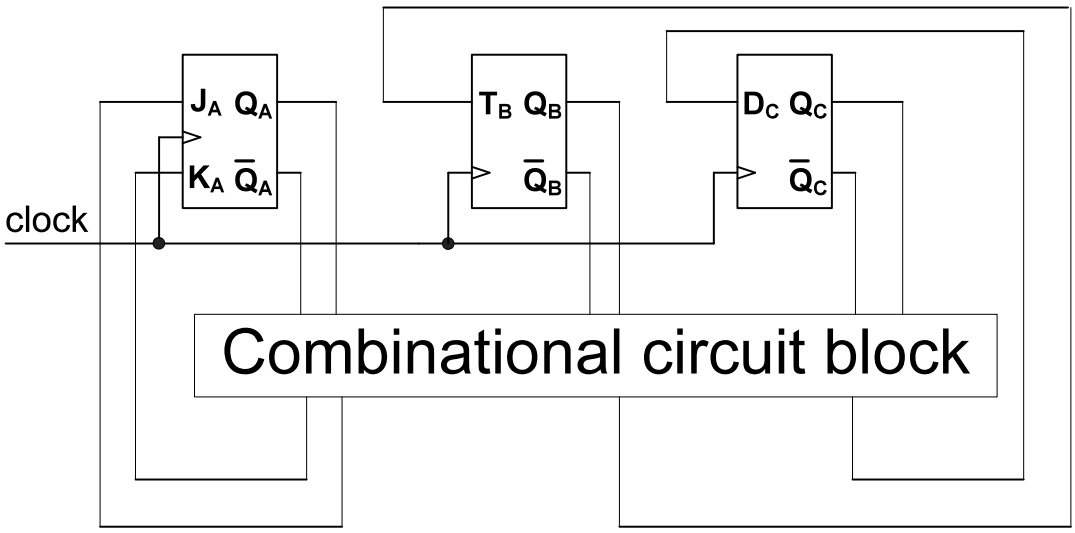
15. The single precision IEEE binary floating point representation of a number is **01000000011000000000000000000000.** What is the decimal value of this number?

1. 1.5
2. 3.5
3. 1.11
4. 2.22
5. none of the above

Continued on page 10

Present State	Next State	Use this area for the truth tables of the flip-flops' inputs
000	010	
001	101	
010	011	
011	001	
100	000	
101	111	
110	100	
111	110	

(a)



(b)

Figure 13 - State table and circuit for questions 16, 17 and 18. Note, Q_A is the most significant bit. Tip: fill in the truth tables and use K-maps for logic minimization.

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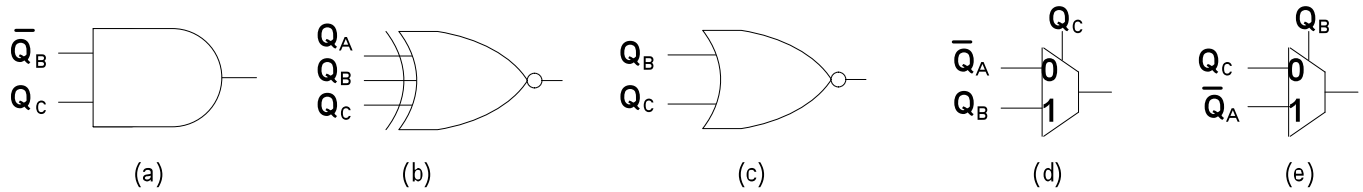

Figure 14 - Circuit implementations for questions 16, 17 and 18.

16. Consider the state transition table of a sequential circuit shown in Figure 13(a) (see previous page). If in our technology library we have only one **JK** flip-flop, one **T** flip-flop and one **D** flip-flop, then a generic implementation is shown Figure 13(b) (see previous page). Based on the state transition table and circuit topology shown in Figure 13, the logic function, which drives the *input* $\mathbf{J_A}$ *of the leftmost flip-flop from Figure 13(b)* is shown in:

1. Figure 14(a)
2. Figure 14(b)
3. Figure 14(c)
4. Figure 14(d)
5. Figure 14(e)

17. Consider the state transition table of a sequential circuit shown in Figure 13(a) (see previous page). If in our technology library we have only one **JK** flip-flop, one **T** flip-flop and one **D** flip-flop, then a generic implementation is shown Figure 13(b) (see previous page). Based on the state transition table and circuit topology shown in Figure 13, the logic function, which drives the *input* $\mathbf{T_B}$ *of the center flip-flop from Figure 13(b)* is shown in:

1. Figure 14(a)
2. Figure 14(b)
3. Figure 14(c)
4. Figure 14(d)
5. Figure 14(e)

18. Consider the state transition table of a sequential circuit shown in Figure 13(a) (see previous page). If in our technology library we have only one **JK** flip-flop, one **T** flip-flop and one **D** flip-flop, then a generic implementation is shown Figure 13(b) (see previous page). Based on the state transition table and circuit topology shown in Figure 13, the logic function, which drives the *input* $\mathbf{D_C}$ *of the rightmost flip-flop from Figure 13(b)* is shown in:

1. Figure 14(a)
2. Figure 14(b)
3. Figure 14(c)
4. Figure 14(d)
5. Figure 14(e)

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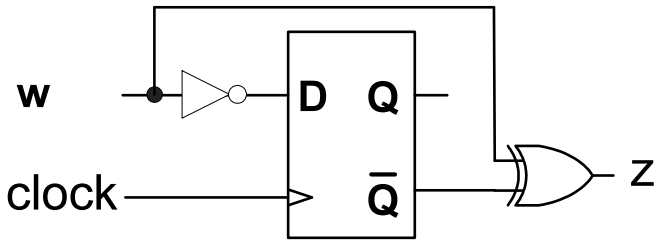

Figure 15 - Circuit for question 19.

19. Consider the sequential circuit shown in Figure 15. Consider the following state assignment: **A** stands for **Q**=0, **B** stands for **Q**=1. The state transition diagram for the circuit from Figure 15 is shown in:

1. Figure 16(a)
2. Figure 16(b)
3. Figure 16(c)
4. Figure 16(d)
5. none of the above

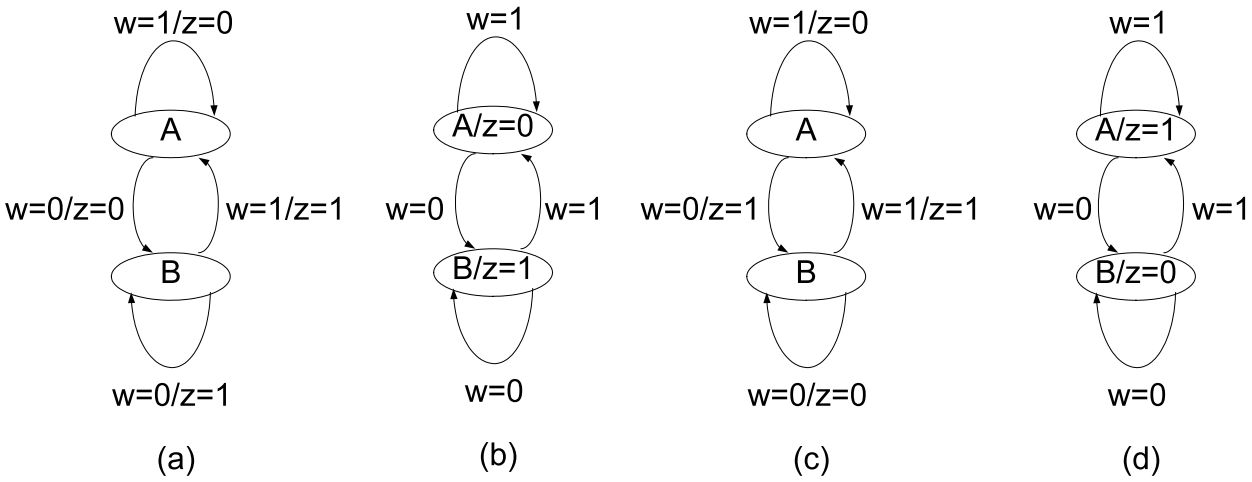

Figure 16 - State transition diagrams for question 19.

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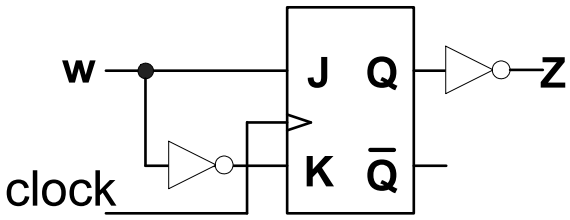

Figure 17 - Circuit for question 20.

20. Consider the sequential circuit shown in Figure 17. Consider the following state assignment: **A** stands for **Q**=0, **B** stands for **Q**=1. The state transition diagram for the circuit from Figure 16 is shown in:

1. Figure 18(a)
2. Figure 18(b)
3. Figure 18(c)
4. Figure 18(d)
5. none of the above

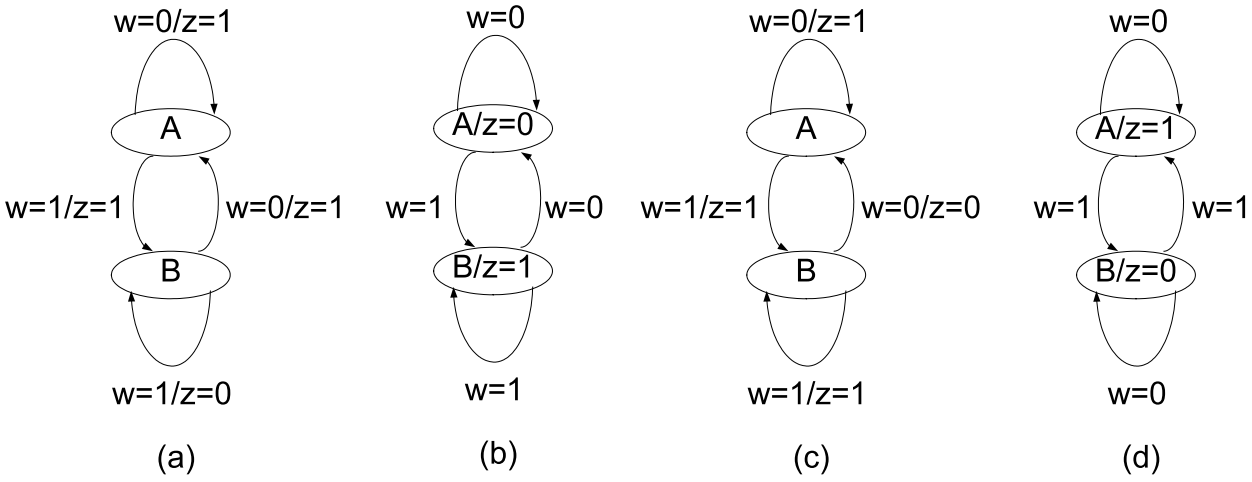

Figure 18 - State transition diagrams for question 20.

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