Dr. Nicola Nicolici **COE/EE2DI4 Midterm Test #1** *Oct 18, 2006*

Instructions: This examination paper includes 10 pages and 20 multiple-choice questions starting on page 3. You are responsible for ensuring that your copy of the paper is complete. Bring any discrepancy to the attention of your invigilator. The answers for all the questions must be indicated by filling the corresponding circle on the optical scanning (OMR) examination sheet. **This OMR examination sheet is the only page to be handed in.** The instructions for completing the OMR examination sheet are provided on page 2. Read and follow these instructions with care! There is one mark for each question. Answer all questions. There is no penalty for guessing. This is a closed book exam. No reference material of any kind is permitted. No calculators of any kind are permitted. **Time allowed is 50 minutes**.

Note: A' and $\overline{A}$ are used interchangeably.

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OMR examination instructions

Continued on page 3

Multiple choice questions (numbered 1 to 20) – indicate your answer by filling the corresponding circle on the OMR answer sheet

1. The binary representation of $(-24)_{10}$ with 8 bits in 2's complement format is:

1. $(0001\ 1000)_2$
2. $(1001\ 1000)_2$
3. $(1111\ 1000)_2$
4. $(1110\ 0111)_2$
5. $(1110\ 1000)_2$

2. The octal equivalent of the unsigned number $(129)_{10}$ is:

1. $(101)_8$
2. $(111)_8$
3. $(201)_8$
4. $(211)_8$
5. $(221)_8$

3. The largest *positive* number in 2's complement format represented with 8-bits is:

1. $(FF)_{16}$
2. $(128)_{10}$
3. $(777)_8$
4. $(0111\ 1111)_2$
5. none of the above

4. The binary equivalent of the unsigned number $(20.125)_{10}$ is:

1. $(0010\ 0000.\ 0001\ 0010\ 0101)_2$
2. $(10100.\ 001)_2$
3. $(10100.01)_2$
4. $(10100.1)_2$
5. none of the above

Continued on page 4

5. Consider the circuit from Figure 1. Function **F** is:

1. **F(A,B)** = A' + B'
2. **F(A,B)** = A'B'
3. **F(A,B)** = A + B'
4. **F(A,B)** = A' + B
5. none of the above

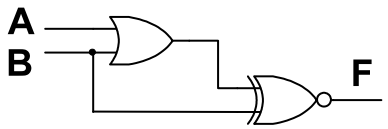

Figure 1 – Circuit for question 5.

6. Consider a comparator circuit between two *unsigned* 2-bit numbers. There is one output **F** and four inputs (i.e., two bits for each number, $\mathbf{A_1A_0}$ and $\mathbf{B_1B_0}$). **F** will be activated to a 1 when $\mathbf{A_1A_0}$ is greater than or equal to $\mathbf{B_1B_0}$ and it will be 0 otherwise. Then, function **F** is:

1. $\mathbf{F(A_1,A_0,B_1,B_0)} = \prod \mathbf{M}\ (1,2,3,6,7,11)$
2. $\mathbf{F(A_1,A_0,B_1,B_0)} = \prod \mathbf{M}\ (1,2,3,6,7,11,15)$
3. $\mathbf{F(A_1,A_0,B_1,B_0)} = \prod \mathbf{M}\ (0,1,2,3,6,7,11,15)$
4. $\mathbf{F(A_1,A_0,B_1,B_0)} = \prod \mathbf{M}\ (0,1,2,3,5,6,7,10,11,15)$
5. none of the above

7. All the prime implicants of **F(A,B,C,D)** shown in Figure 2 are:

1. A'B'C', AB'D', AC'D, B'C'D, BC'D'
2. A'BC', AB'D, AC'D, B'CD, BC'D
3. A'BC', A'CD, B'CD, BC'D
4. A'CD, B'CD, BC'D
5. none of the above

8. All the essential prime implicants of **F(A,B,C,D)** shown in Figure 2 are:

1. A'BC', B'CD
2. A'CD, B'CD
3. A'B'C', AB'D', AC'D, B'C'D, BC'D'
4. A'BC', AB'D, AC'D, B'CD, BC'D
5. none of the above

C D \ A B	00	01	11	10
00	0	1	0	0
01	0	1	1	1
11	1	0	0	1
10	0	0	0	0

Figure 2 - Karnaugh map for function F(A,B,C,D) for questions 7 and 8.

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C D \ A B	00	01	11	10
00	0	X	1	X
01	X	0	X	1
11	1	X	0	X
10	X	0	X	0

Figure 3 - Karnaugh map for function F(A,B,C,D) for question 9. Note, 'X' stands for don't care.

9. Consider the function **F(A,B,C,D)** shown in Figure 3. The simplified logical expression in the sum-of-products (SOP) form (i.e., the minimum number of product terms and the minimum number of literals in every product term) for **F(A,B,C,D)** can be converted into a circuit implementation using only NAND gates, which is shown in:

1. Figure 4(a)
2. Figure 4(b)
3. Figure 4(c)
4. Figure 4(d)
5. none of the above

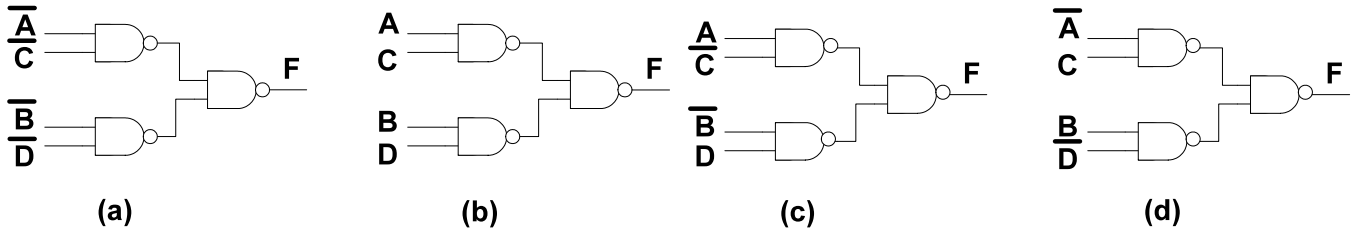

Figure 4 - Implementations for function F(A,B,C,D) for question 9.

10. The logic function **F(A,B)** implemented by the circuit shown in Figure 5 is equivalent to the logic function of a:

1. 2-input AND gate
2. 2-input NAND gate
3. 2-input XOR gate
4. 2-input XNOR gate
5. none of the above

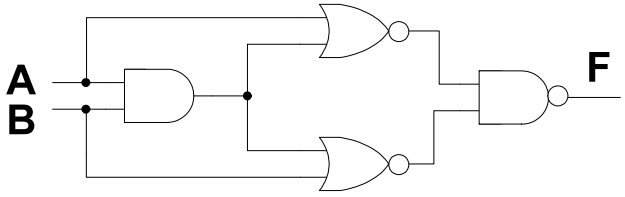

Figure 5 - Implementation for function F(A,B) for question 10.

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11. The circuit from Figure 6 is equivalent to the circuit from:

1. Figure 7(a)
2. Figure 7(b)
3. Figure 7(c)
4. Figure 7(d)
5. none of the above

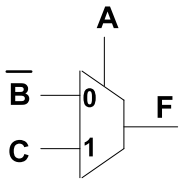

Figure 6 - Circuit for question 11.

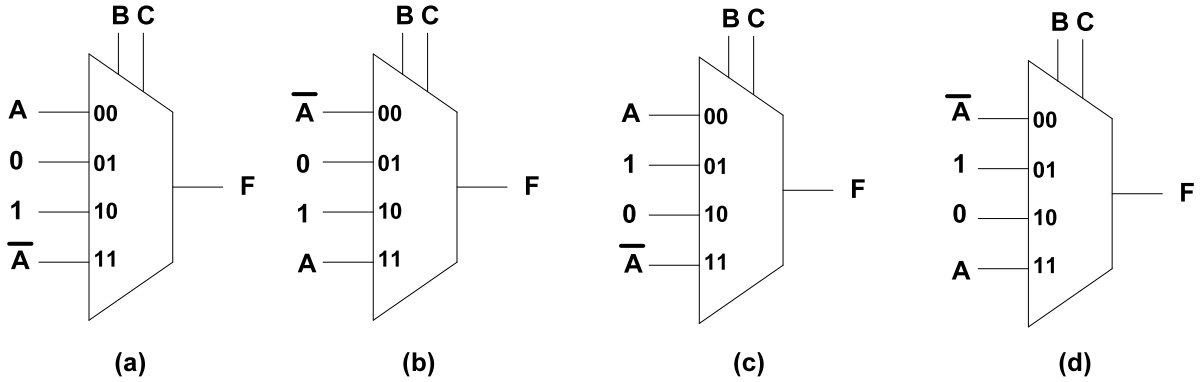

Figure 7 - Circuits for question 11.

12. The circuit from Figure 8 is equivalent to the circuit from:

1. Figure 9(a)
2. Figure 9(b)
3. Figure 9(c)
4. Figure 9(d)
5. none of the above

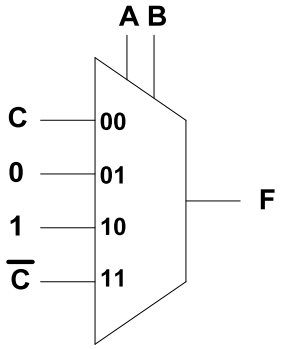

Figure 8 - Circuit for question 12.

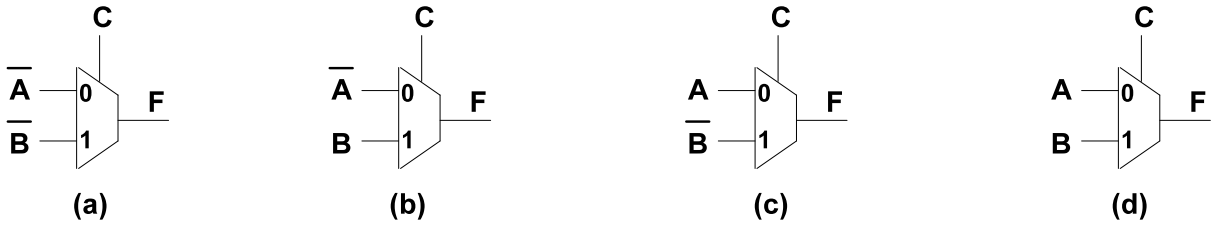

Figure 9 - Circuits for question 12.

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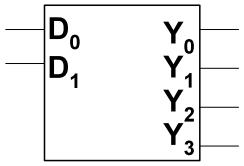
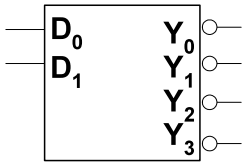


D_1	D_0	Y_0	Y_1	Y_2	Y_3
0	0	1	0	0	0
0	1	0	1	0	0
1	0	0	0	1	0
1	1	0	0	0	1

(a) Decoder with un-inverted outputs



D_1	D_0	Y_0	Y_1	Y_2	Y_3
0	0	0	1	1	1
0	1	1	0	1	1
1	0	1	1	0	1
1	1	1	1	1	0

(b) Decoder with inverted outputs

Figure 10 - Block diagrams and truth tables for decoders without an enable signal for questions 13 and 14.

13. The circuit shown in Figure 11 is:

1. **F(A,B)** = Σ **m** (2,3)
2. **F(A,B)** = Σ **m** (1,3)
3. **F(A,B)** = Σ **m** (1,2)
4. **F(A,B)** = Σ **m** (0,1)
5. none of the above

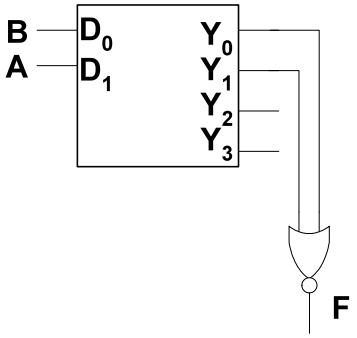


Figure 11 – Circuit for question 13. Use the truth table of the decoder with un-inverted outputs from Figure 10(a).

14. The circuit shown in Figure 12 is:

1. **F(A,B)** = Σ **m** (2,3)
2. **F(A,B)** = Σ **m** (1,3)
3. **F(A,B)** = Σ **m** (1,2)
4. **F(A,B)** = Σ **m** (0,1)
5. none of the above

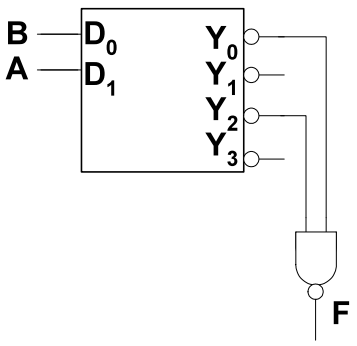


Figure 12 – Circuit for question 14. Use the truth table of the decoder with inverted outputs from Figure 10(b).

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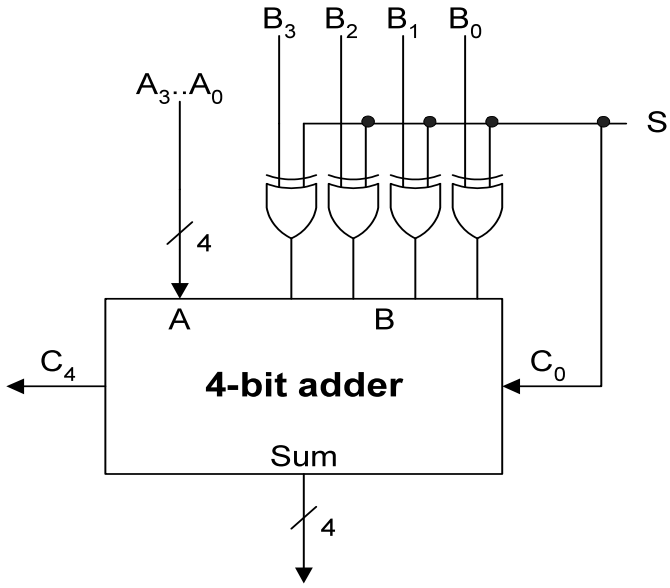

Figure 13 – Circuit for questions 15 to 17. Note, C_0 is carry in and C_4 is carry out for the 4-bit adder.

Reminder: **This adder and subtractor unit operates on 2's complement numbers and the S input signal determines whether an addition or subtraction will occur.**

15. In Figure 13, if $\mathbf{A_3A_2A_1A_0}$=0001, $\mathbf{B_3B_2B_1B_0}$=1111 and **S**=0 then the output is:

1. **Sum**=0010 and $\mathbf{C_4}$=1
2. **Sum**=0010 and $\mathbf{C_4}$=0
3. **Sum**=0000 and $\mathbf{C_4}$=1
4. **Sum**=0000 and $\mathbf{C_4}$=0
5. none of the above

16. In Figure 13, if $\mathbf{A_3A_2A_1A_0}$=1111, $\mathbf{B_3B_2B_1B_0}$=0001 and **S**=1 then the output is:

1. **Sum**=0010 and $\mathbf{C_4}$=1
2. **Sum**=0010 and $\mathbf{C_4}$=0
3. **Sum**=0000 and $\mathbf{C_4}$=1
4. **Sum**=0000 and $\mathbf{C_4}$=0
5. none of the above

17. In Figure 13 overflow occurs for:

1. $\mathbf{A_3A_2A_1A_0}$=0010, $\mathbf{B_3B_2B_1B_0}$=0110 and **S**=1
2. $\mathbf{A_3A_2A_1A_0}$=0010, $\mathbf{B_3B_2B_1B_0}$=0110 and **S**=0
3. $\mathbf{A_3A_2A_1A_0}$=1110, $\mathbf{B_3B_2B_1B_0}$=0110 and **S**=1
4. $\mathbf{A_3A_2A_1A_0}$=1110, $\mathbf{B_3B_2B_1B_0}$=0110 and **S**=0
5. none of the above

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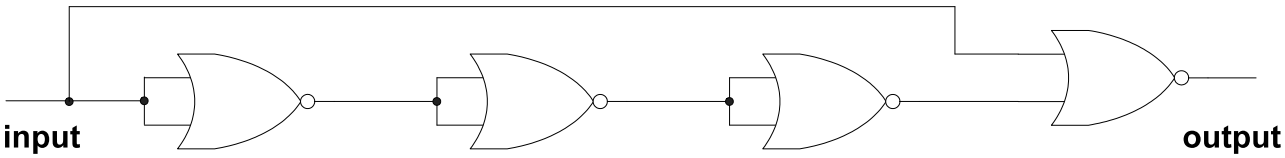

Figure 14 - Pulse generator circuit for question 18.

18. The pulse generator circuit shown in Figure 14 receives on its input a periodic signal shown in Figure 15. Let's assume that the 2 input NOR gate's propagation delays from Low to High and High to Low are identical and they are equal to 3 ns. Then the output signal will be periodic as well and, for each period, its Low to High transition and High to Low transition will be placed in between the High to Low transition and Low to High transition of the input signal. Let **d** be the time between the High to Low transition of the input signal and the High to Low transition of the output signal. Based on the above specifications and using the circuit diagram and the input waveform from Figures 14 and 15, the correct value for **d** is:

1. 3 ns
2. 6 ns
3. 9 ns
4. 12 ns
5. 15 ns

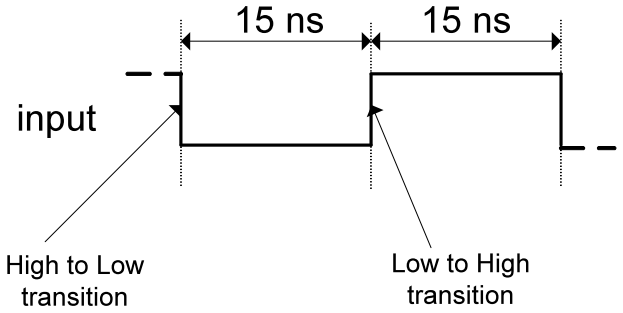

Figure 15 - Periodic input waveform for question 18.

Hint: **Draw the waveforms on the inputs and the output of the rightmost NOR gate.**

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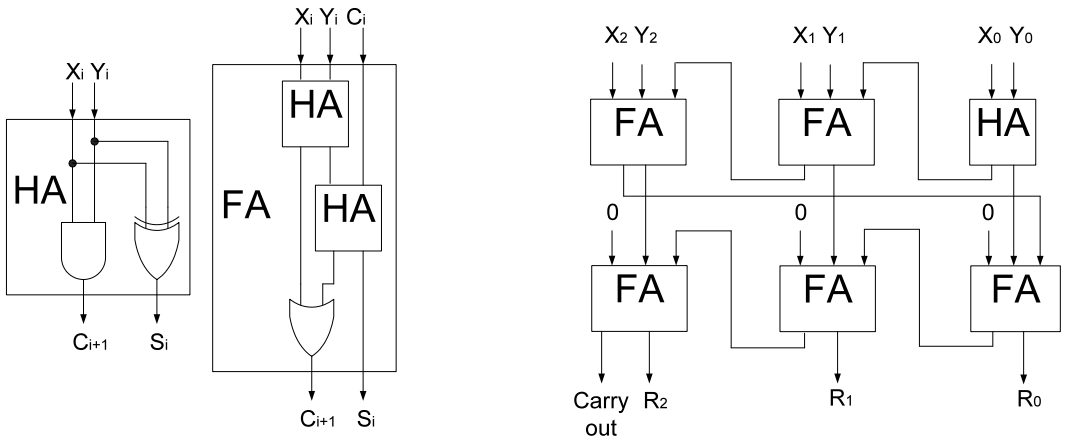

Figure 16 – Circuits for questions 19 and 20.

19. A half adder (HA) cell is shown in Figure 16(a) and the implementation of a full adder (FA) cell using two HA cells and one OR gate is shown in Figure 16(b). Figure 16(c) shows an arithmetic circuit that adds two 3-bit numbers provided in 1s complement format (the output $\mathbf{R_2R_1R_0}$ is also a 3-bit number represented in 1s complement format). Let's assume that the propagation delays from high to low and low to high for 2-input AND, 2-input OR and 2-input XOR gates are equal to 5 ns. Then the *longest* propagation delay from *any* input ($\mathbf{X_2X_1X_0Y_2Y_1Y_0}$) to the **Carry out** signal of the circuit from Figure 16(c) is:

1. 50 ns
2. 55 ns
3. 60 ns
4. 65 ns
5. none of the above

***Note:* The order of signals on the inputs and the outputs of HA and FA cells in Figure 16(c) follows the convention from Figures 16(a) and 16(b).**

20. Consider the setup from problem 19 with the following change. In Figure 16(c) we replace the rightmost FA adder cell from the second level of addition with an HA (as shown in Figure 17). The behavior of the circuit is preserved. The *longest* propagation delay from *any* input ($\mathbf{X_2X_1X_0Y_2Y_1Y_0}$) to the **Carry out** signal of the circuit from Figure 17 is:

1. 50 ns
2. 55 ns
3. 60 ns
4. 65 ns
5. none of the above

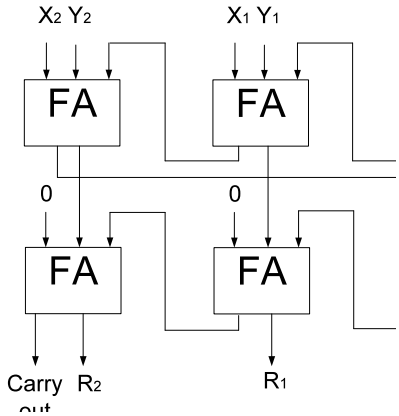

Figure 17 – Circuit for question 20.

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