Dr. S. Shirani **COE2DI4 Midterm Test #1** Oct. 15*, 2009*

Instructions: This examination paper includes 10 pages and 20 multiple-choice questions starting on page 3. You are responsible for ensuring that your copy of the paper is complete. Bring any discrepancy to the attention of your invigilator. The answers for all the questions must be indicated by filling the corresponding circle on the optical scanning (OMR) examination sheet. **This OMR examination sheet is the only page to be handed in.** The instructions for completing the OMR examination sheet are provided on page 2. Read and follow these instructions with care! There is one mark for each question. Answer all questions. There is no penalty for guessing. This is a closed book exam. No reference material of any kind is permitted. No calculators of any kind are permitted. **Time allowed is 50 minutes**.

Note: A' and $\overline{A}$ are used interchangeably.

OMR examination instructions

Multiple choice questions (numbered 1 to 20) – indicate your answer by filling the corresponding circle on the OMR answer sheet

1. The hexadecimal equivalent of 224_{10} is:

1. $F0_{16}$
2. $E0_{16}$
3. $E1_{16}$
4. $1E_{16}$
5. $D0_{16}$

2. The octal equivalent of FA_{16} is:

1. 372_8
2. 554_8
3. 122_8
4. 525_8
5. 255_8

3. The binary equivalent of 22.25_{10} is:

1. 10110.01_2
2. 1011.10_2
3. 10111.10_2
4. $1101.\ 01_2$
5. $1101.\ 101_2$

4. The decimal equivalent of 11111010_2 represented in sign 1's complement format is:

1. -6_{10}
2. -5_{10}
3. -122_{10}
4. -250_{10}
5. 250_{10}

5. We would like to design a "ones count" circuit that works as follows. The circuit has four binary inputs: A, B, C, D and generates a 3-bit output: XYZ. XYZ is 000 if none of the inputs are 1, 001 if one input is 1, 010 if two are one, 011 if three inputs are 1 and 100 if all four inputs are 1. The minimal SOP form of Z:

1. Has 4 product terms
2. Has 8 product terms
3. Has 6 product terms
4. Has 5 product terms
5. None of the above

6. Consider a combinational logic system that determines if a 4-bit binary quantity A, B, C, D in the range of 0010 (2_{10}) to 1111 (15_{10}) is a prime number. That is, the function is 1 if the input is prime. (Note: an integer p is called a prime number if the only positive integers that divide p are 1 and p itself). Assume that the binary patterns 0000 (0_{10}) and 0001 (1_{10}) are "don't cares." Treat the values as unsigned. Minimized Sum of Products form of this function is:

1. A'B'C'D' + A'BCD'
2. A'B'+A'D+ BC'D + B'CD
3. A'B'C'D'+BCD'
4. BC'D+A'BD+A'B'C+B'CD
5. None of the above

CD \ AB	00	01	11	10
00	0	0	1	0
01	1	0	0	0
11	1	1	1	0
10	0	0	1	0

Figure 1 - Karnaugh map for a logic function F(A,B,C,D) for questions 7 to 9

7. All the prime implicants of **F(A,B,C,D)** shown in Figure 1 are:

1. A'B'D, A'CD, ABD', ABC, BCD
2. A'B'D, A'CD, ABD', ABC
3. A'B'D, ABD', BCD
4. A'B'D, ABD'
5. none of the above

8. All the essential prime implicants of **F(A,B,C,D)** shown in Figure 1 are:

1. A'B'D, A'CD, ABD', ABC, BCD
2. A'B'D, A'CD, ABD', ABC
3. A'B'D, ABD', BCD
4. A'B'D, ABD'
5. none of the above

9. The simplified logical expression in the sum-of-products (SOP) form (i.e., the minimum number of product terms and the minimum number of literals in every product term) for **F(A,B,C,D)** shown in Figure 1 is:

1. A'B'D + ABD' + ABC + BCD
2. A'B'D + A'CD + ABD'+ ABC
3. A'B'D + ABD' + BCD
4. A'B'D + ABD'
5. none of the above

CD \ AB	00	01	11	10
00	1	X	0	X
01	0	X	1	X
11	X	1	X	0
10	X	0	X	1

Figure 2 - Karnaugh map for a logic function F(A,B,C,D) for questions 10 and 11. Note, 'X' stands for don't care.

10. Consider the function **F(A,B,C,D)** shown in Figure 2. The simplified logical expression in the sum-of-products (SOP) form (i.e., the minimum number of product terms and the minimum number of literals in every product term) for **F(A,B,C,D)** can be converted into a circuit implementation using only NAND gates, which is:

1. shown in Figure 3(a)
2. shown in Figure 3(b)
3. shown in Figure 3(c)
4. shown in Figure 3(d)
5. none of the above

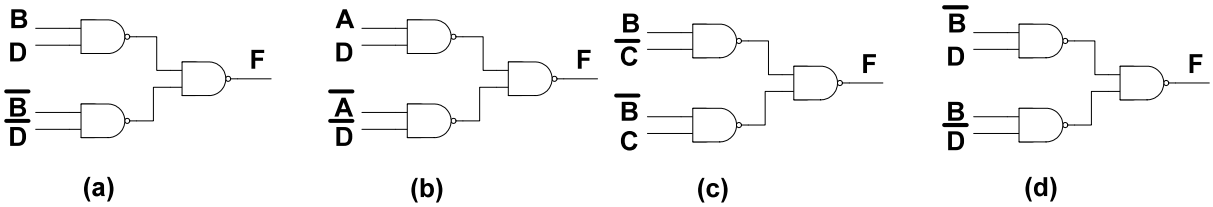

Figure 3 - Implementations for function F(A,B,C,D) for question 10

11. Consider the function **F(A,B,C,D)** shown in Figure 2. The simplified logical expression in the product-of-sums (POS) form (i.e., the minimum number of sum terms and the minimum number of literals in every sum term) for **F(A,B,C,D)** can be converted into a circuit implementation using only NOR gates, which is:

1. shown in Figure 4(a)
2. shown in Figure 4(b)
3. shown in Figure 4(c)
4. shown in Figure 4(d)
5. none of the above

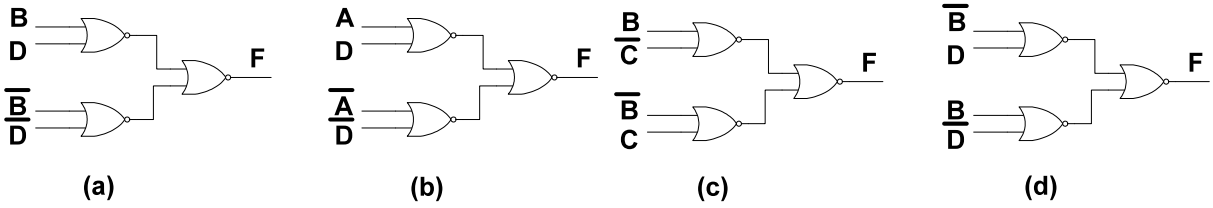

Figure 4 - Implementations for function F(A,B,C,D) for question 11

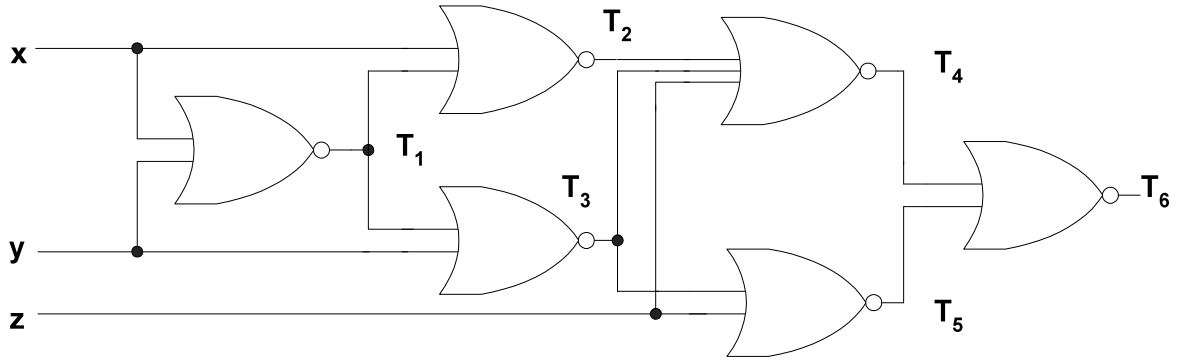

Figure 5 - Circuit for questions 12 and 13.

12. If input z=1 then output $\mathbf{T_6}$ of Figure 5 is:

1. 0
2. x'y
3. xy'
4. 1
5. none of the above

13. Assuming the propagation delay is 10ns through a NOR gate, what is the longest delay between inputs and $\mathbf{T_6}$ of Figure 5:

1. 20ns
2. 30ns
3. 40ns
4. 50ns
5. 60ns

14. The function $f = X_1 \oplus X_2 \oplus X_3 ... \oplus X_n$ defined over n variable has how many minterms:

1. n/2
2. $n^2/2$
3. 2^{n-1}
4. 2^{n-2}
5. none of the above

15. Consider the function f(A,B,C)=AB+B'C'+AC'. The canonical product of sum (POS) form of the complement of f is:

1. f'(A,B,C)=Π(0,4,6,7)
2. f'(A,B,C)=Π(1,2,3,5)
3. f'(A,B,C)=Π(0,2,3,)
4. f'(A,B,C)=Π(1,4,5,6,7)
5. None of the above

16. The logic function **F(X,Y)** implemented by the circuit shown in Figure 6 is equivalent to the logic function of a:

1. 2-input AND gate
2. 2-input NAND gate
3. 2-input XOR gate
4. 2-input XNOR gate
5. none of the above

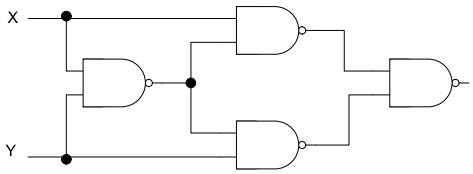

Figure 6. Circuit for problem 16

17. In Figure 7, if $A_3A_2A_1A_0$=1001, $B_3B_2B_1B_0$=1101 and S=1 then the output is:

1. Sum = 0110 and C_4 = 0
2. Sum = 0110 and C_4 = 1
3. Sum = 1100 and C_4 = 0
4. Sum = 1100 and C_4 = 1
5. none of the above

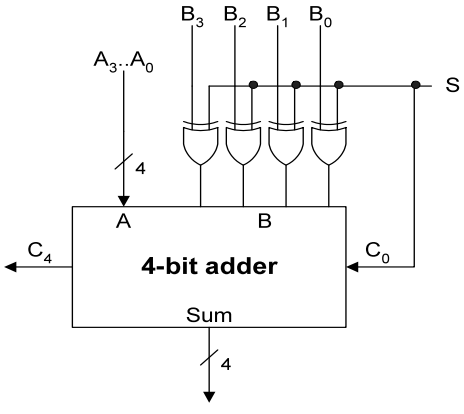

Figure 7 – Circuit for questions 17 and 18. Note, c_0 is carry in and c_4 is carry out for the 4-bit adder.

18. In Figure 7, overflow occurs for:

1. $A_3A_2A_1A_0$=0100, $B_3B_2B_1B_0$=1010 and S=0
2. $A_3A_2A_1A_0$=0100, $B_3B_2B_1B_0$=0110 and S=1
3. $A_3A_2A_1A_0$=1100, $B_3B_2B_1B_0$=0110 and S=0
4. $A_3A_2A_1A_0$=1100, $B_3B_2B_1B_0$=1010 and S=1
5. none of the above

19. Consider the oscillator circuit shown in Figure 8(a), which produces a periodic signal (**OUTPUT**) with a period of 36 ns, as shown in Figure 8(b). Let's assume that the 2 input NAND gate's propagation delays from low to high and high to low are equal and they are labeled as T_{pd}. Then the value of T_{pd} is:

1. 4 ns
2. 6 ns
3. 9 ns
4. 12 ns
5. 18 ns

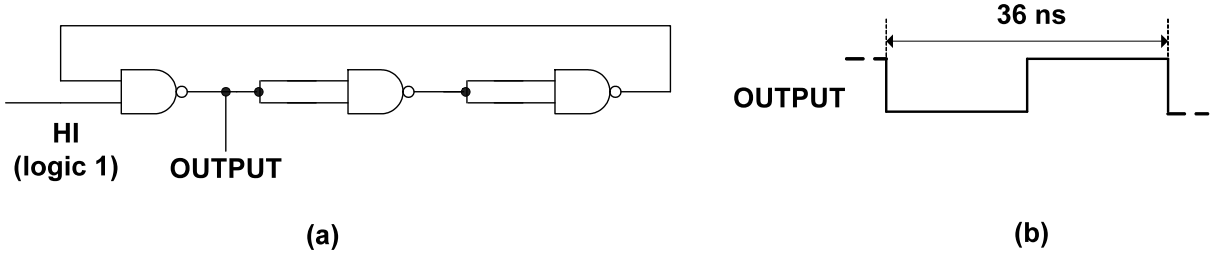

Figure 8 - Circuit and waveform for question 19

20. A 32-bit adder is designed by connecting 4 eight-bit carry-lookahead adders as shown in Figure 9. The carry-lookahead adders are similar to the one discussed in the class. What is the critical path delay of the circuit shown in Fig. 9? (Hint: in an n-bit carry-lookahead adder the delay for carry-out is 3 gates from the input and 2 gates from the carry-in. Also, the delay for sum bits is 3 gates from the carry-in and 4 gates from the inputs.)

1. 4 gate delays
2. 9 gate delays
3. 10 gate delays
4. 12 gate delays
5. none of the above

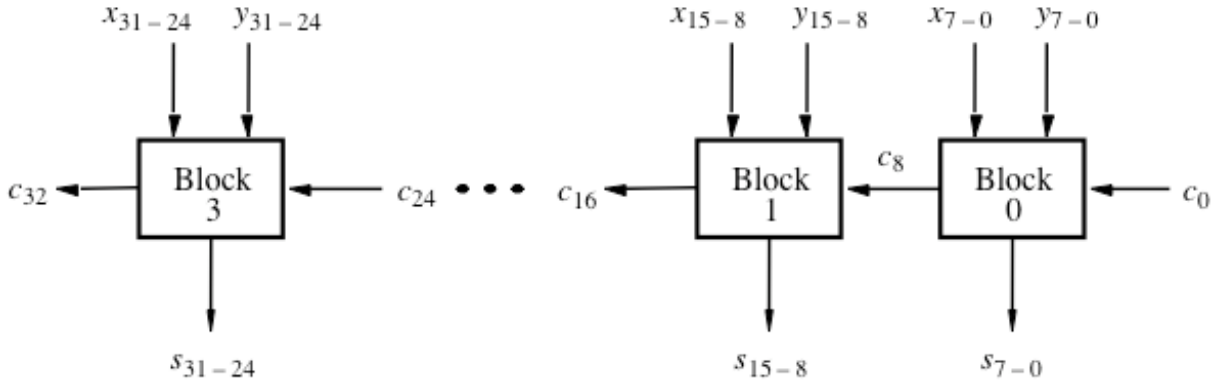

Figure 9 - Circuit for question 20

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