Dr. Nicola Nicolici **COE/EE2DI4 Midterm Test #2** *Nov 22, 2006*

Instructions: This examination paper includes 12 pages and 20 multiple-choice questions starting on page 3. You are responsible for ensuring that your copy of the paper is complete. Bring any discrepancy to the attention of your invigilator. The answers for all the questions must be indicated by filling the corresponding circle on the optical scanning (OMR) examination sheet. **This OMR examination sheet is the only page to be handed in.** The instructions for completing the OMR examination sheet are provided on page 2. Read and follow these instructions with care! There is one mark for each question. Answer all questions. There is no penalty for guessing. This is a closed book exam. No reference material of any kind is permitted. No calculators of any kind are permitted. **Time allowed is 50 minutes**.

Note: A' and $\overline{A}$ are used interchangeably.

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OMR examination instructions

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Multiple choice questions (numbered 1 to 20) – indicate your answer by filling the corresponding circle on the OMR answer sheet

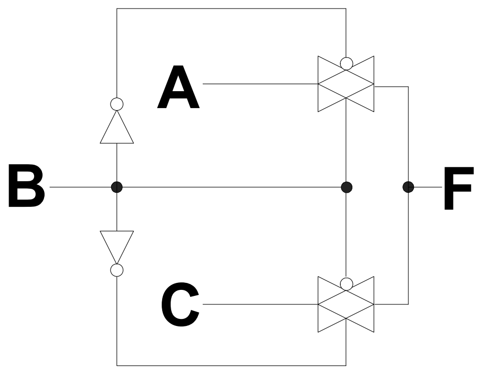

Figure 1 - CMOS circuit for question 1.

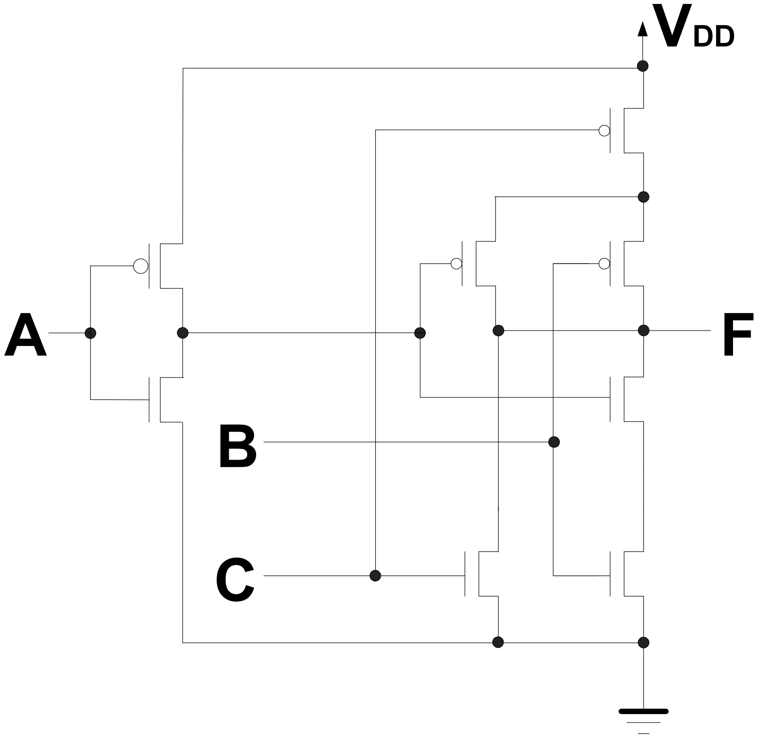

Figure 2 - CMOS circuit for question 2.

1. The logic function **F(A,B,C)** implemented by the complementary metal-oxide semiconductor (CMOS) circuit shown in Figure 1:

1. AB' + B'C
2. AB' + BC
[✓ 3.] AB + B'C
4. AB + BC
5. none of the above

2. The logic function **F(A,B,C)** implemented by the CMOS circuit shown in Figure 2 is:

[✓ 1.] AC' + B'C'
2. A'C' + B'C'
3. A' + B'C'
4. A + B'C'
5. none of the above

Continued on page 4

3. The function implemented using three 2-input look-up tables (LUTs) as shown in Figure 3 is:

1. **F(A,B,C)** = **Σ m** (0,1,2,4,7)
[✓ 2.] **F(A,B,C)** = **Σ m** (0,1,4,7)
3. **F(A,B,C)** = **Σ m** (0,4,7)
4. **F(A,B,C)** = **Σ m** (0,7)
5. none of the above

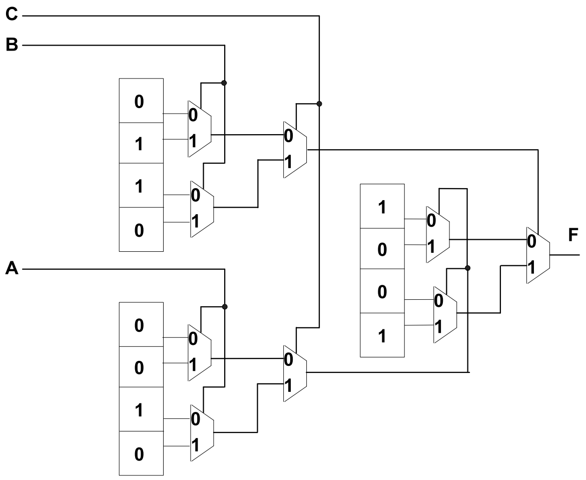

Figure 3 – Circuit for question 3.

4. The programmable array logic (PAL) implementation of function F shown in Figure 4 is:

1. **F(A,B,C)** = **Σ m** (0,1,2,7)
2. **F(A,B,C)** = **Σ m** (0,1,6,7)
3. **F(A,B,C)** = **Σ m** (1,4,6,7)
[✓ 4.] **F(A,B,C)** = **Σ m** (3,4,6,7)
5. none of the above

5. The PAL implementation of function G shown in Figure 4 is:

1. **G(A,B,C)** = **Σ m** (0,1,2,7)
2. **G(A,B,C)** = **Σ m** (0,1,6,7)
3. **G(A,B,C)** = **Σ m** (1,4,6,7)
4. **G(A,B,C)** = **Σ m** (3,4,6,7)
[✓ 5.] none of the above

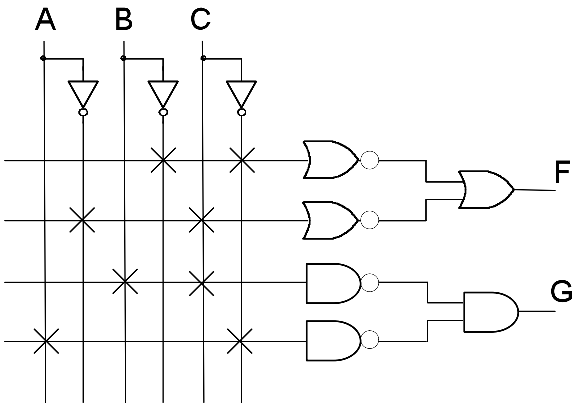

Figure 4 – Circuit for questions 4 and 5. An X indicates that the wires are connected, i.e., the vertical signal is an input to the corresponding horizontal NOR or NAND gates respectively.

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6. Consider a read-only memory (ROM) that performs binary to 2-digit binary-coded decimal (BCD) conversion as follows. The binary number is applied on the 7 input address lines, $\mathbf{A_6A_5A_4A_3A_2A_1A_0}$, and the equivalent 2-digit BCD number is read on the 8 output data lines, $\mathbf{D_7D_6D_5D_4D_3D_2D_1D_0}$, after the memory access time (note, the most significant BCD digit will appear on the four most significant bits on the output). Consequently, when applying the input address $\mathbf{A_6A_5A_4A_3A_2A_1A_0}$=1010001, after the memory access time the output data will become:

[✓ 1.] $\mathbf{D_7D_6D_5D_4D_3D_2D_1D_0}$=1000 0001
2. $\mathbf{D_7D_6D_5D_4D_3D_2D_1D_0}$=1001 1001
3. $\mathbf{D_7D_6D_5D_4D_3D_2D_1D_0}$=1010 1110
4. $\mathbf{D_7D_6D_5D_4D_3D_2D_1D_0}$=0101 0001
5. none of the above

7.

```
LIBRARY IEEE;
USE IEEE.std_logic_1164.ALL;

ENTITY question7 IS
  PORT(   s0, s1, enb    : IN    STD_LOGIC;
          y0, y1, y2, y3 : OUT   STD_LOGIC);
END question7;

ARCHITECTURE behavior OF question7 IS
BEGIN
  y0 <= not(not s0 and not s1 and enb);
  y1 <= not(s0 and not s1 and enb);
  y2 <= not(not s0 and s1 and enb);
  y3 <= not(s0 and s1 and enb);
END behavior;
```

In the above VHDL description, if the inputs are s0=1,s1=0,enb=1, then the outputs are:

1. y0=1, y1=1, y2=1, y3=0
2. y0=1, y1=1, y2=0, y3=1
[✓ 3.] y0=1, y1=0, y2=1, y3=1
4. y0=0, y1=1, y2=1, y3=1
5. y0=1, y1=1, y2=1, y3=1

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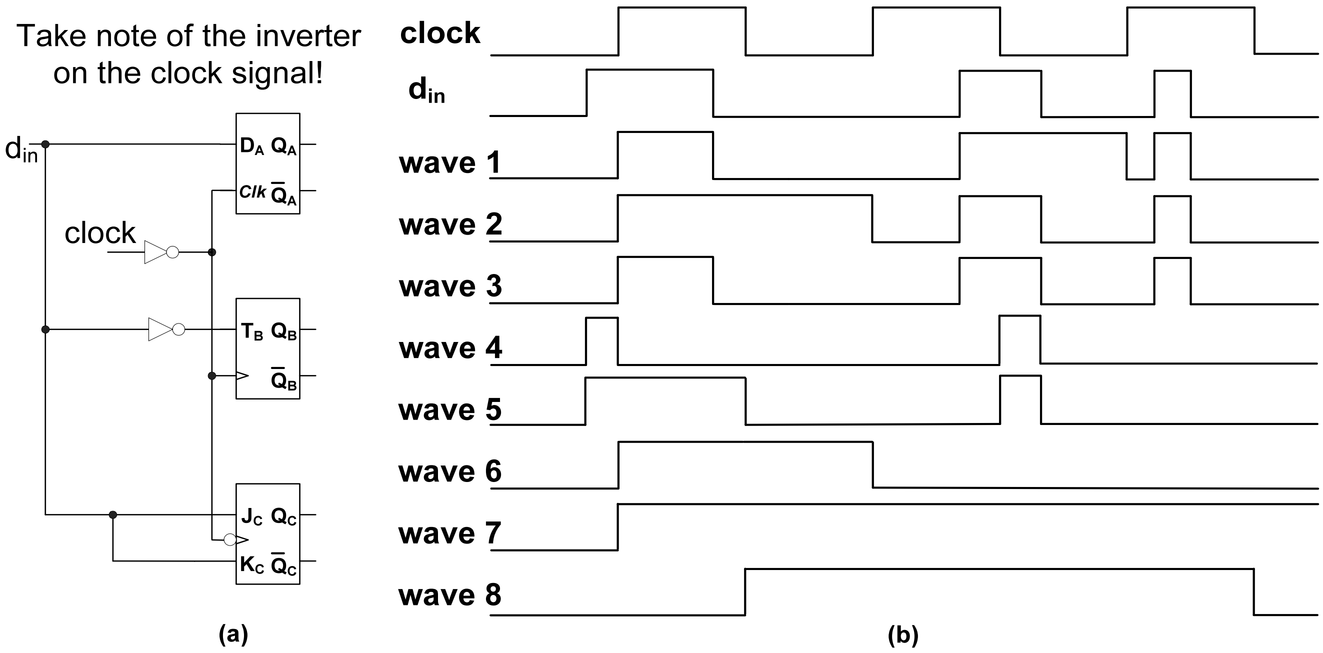
Take note of the inverter on the clock signal!

Figure 5 - Sequential (or storage) elements and signal waveforms for questions 8, 9 and 10. Note, the initial value of all the storage elements is zero and they are assumed to be ideal, i.e., the propagation delays and setup/hold times are considered to be zero. The propagation delays on the two inverters placed on the d_{in} and clock inputs are considered also to be zero.

8. Given the **clock** and **d_{in}** waveforms in Figure 5(b) the waveform for **Q_A** from Figure 5(a) is:

1. wave 1 from Figure 5(b)
2. wave 2 from Figure 5(b)
3. wave 3 from Figure 5(b)
4. wave 4 from Figure 5(b)

[✓ 5.] wave 5 from Figure 5(b)

9. Given the **clock** and **d_{in}** waveforms in Figure 5(b) the waveform for **Q_B** from Figure 5(a) is:

1. wave 4 from Figure 5(b)
2. wave 5 from Figure 5(b)
3. wave 6 from Figure 5(b)
4. wave 7 from Figure 5(b)

[✓ 5.] wave 8 from Figure 5(b)

10. Given the **clock** and **d_{in}** waveforms in Figure 5(b) the waveform for **Q_C** from Figure 5(a) is:

1. wave 4 from Figure 5(b)
2. wave 5 from Figure 5(b)
3. wave 6 from Figure 5(b)

[✓ 4.] wave 7 from Figure 5(b)

5. wave 8 from Figure 5(b)

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11. In Figure 6, if the current state is **$Q_3Q_2Q_1Q_0$**=1001, then after the next *negative edge* of the ***clock*** signal the new state will be:

1. 0110
[✓ 2.] 0111
3. 1110
4. 0101
5. 0100

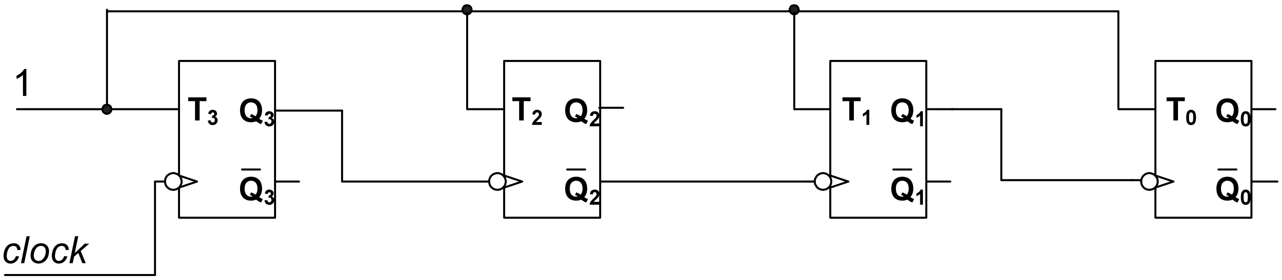

Figure 6 - Circuit for question 11 (note, the flip-flops are *negative edge* triggered).

<u>Note for question 11:</u> Because NOT all the flip-flops' clock inputs share the same *clock* signal, it is considered that the new state value will be observed only when all the flip-flops' outputs have become stable, i.e., after *all* the events triggered by the *negative edge* of the *clock* signal have been completed.

12. In Figure 7, if the current state is **$Q_3Q_2Q_1Q_0$**=1001, then the next state will be:

1. 0001
2. 0011
3. 0110
[✓ 4.] 0100
5. none of the above

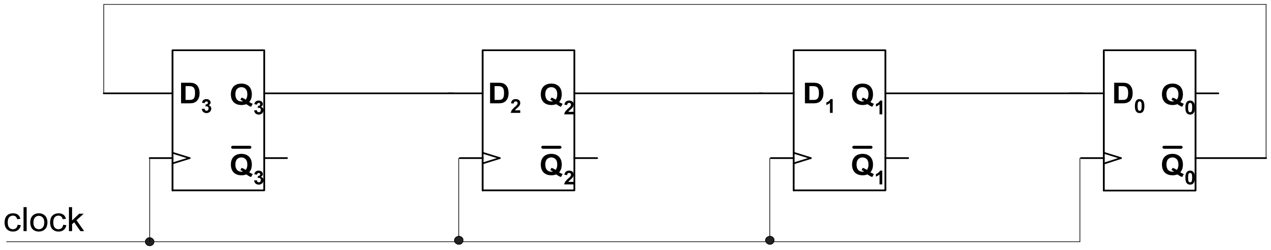

Figure 7 - Circuit for question 12.

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13. In Figure 8, if the current state is **$Q_2Q_1Q_0$**=101, then the next state will be:

1. 000

[✓ 2.] 001

3. 010

4. 011

5. none of the above

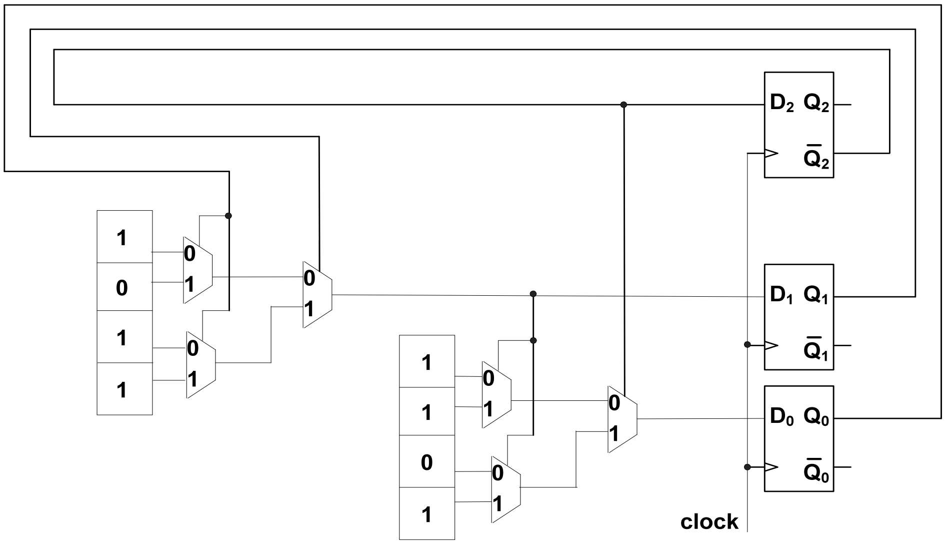

Figure 8 - Circuit for question 13.

14. The periodic sequence **$Q_2Q_1Q_0$** generated by the circuit shown in Figure 9 is:

[✓ 1.] 000, 101, 110, 010, 100, 011, 001

2. 000, 101, 010, 100, 011, 001

3. 000, 101, 100, 011, 001

4. 000, 101, 011, 001

5. none of the above

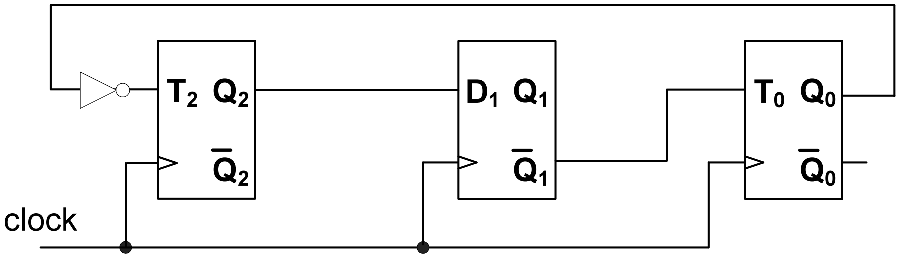

Figure 9 - Circuit for question 14 (it is assumed that after power up the state is 000). Note, the flip-flop in the middle is a D flip-flop.

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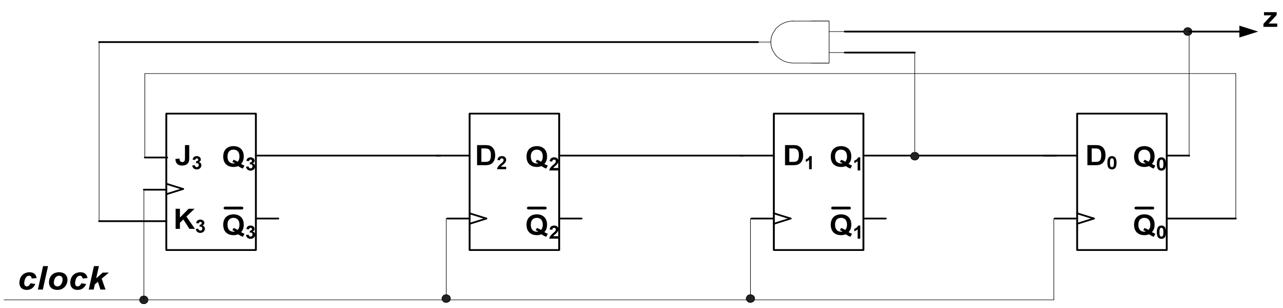

Figure 10 - Circuit for question 15.

15. The circuit from Figure 10 is used to generate a periodic sequence (it is assumed that after power up the state is 0000). If the frequency of the ***clock*** signal is 64 MHz, then signal ***z***, which is also a periodic signal, has its frequency equal to:

1. 32 MHz
2. 16 MHz
[✓ 3.] 8 MHz
4. 4 MHz
5. none of the above

16. The periodic sequence $\mathbf{Q_2Q_1Q_0}$ generated by the circuit shown in Figure 11 is:

1. 000,001,111,110
2. 000,011,111,110
3. 000,111,110,001
[✓ 4.] 000,111,100,011
5. 000,110,100,011

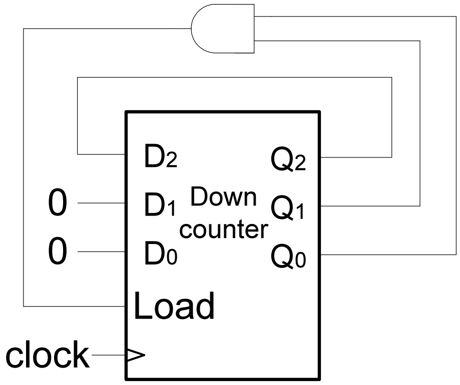

Figure 11 – A 3-bit synchronous down counter with parallel load capability for question 16. It is assumed that after power up the state is 000 and Q_2 and D_2 are the most significant bits.

17. Which of the circuits shown in Figure 12 (see next page) are equivalent?

1. Figure 12(a) and Figure 12(c)
2. Figure 12(a) and Figure 12(d)
3. Figure 12(b) and Figure 12(c)
4. Figure 12(b) and Figure 12(d)
[✓ 5.] none of the above

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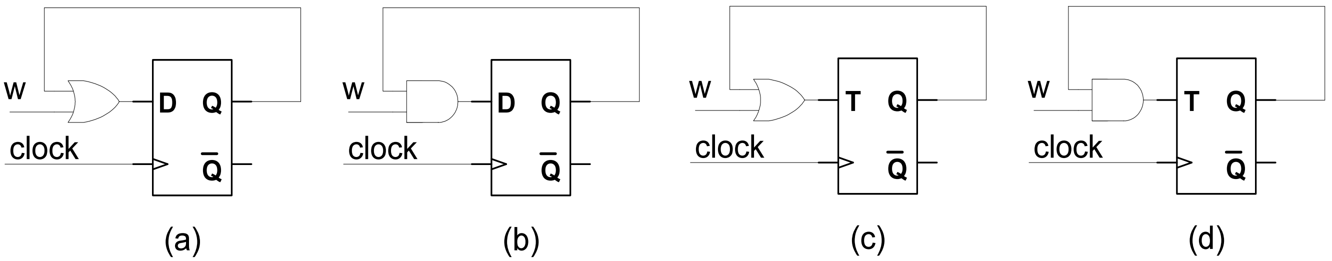
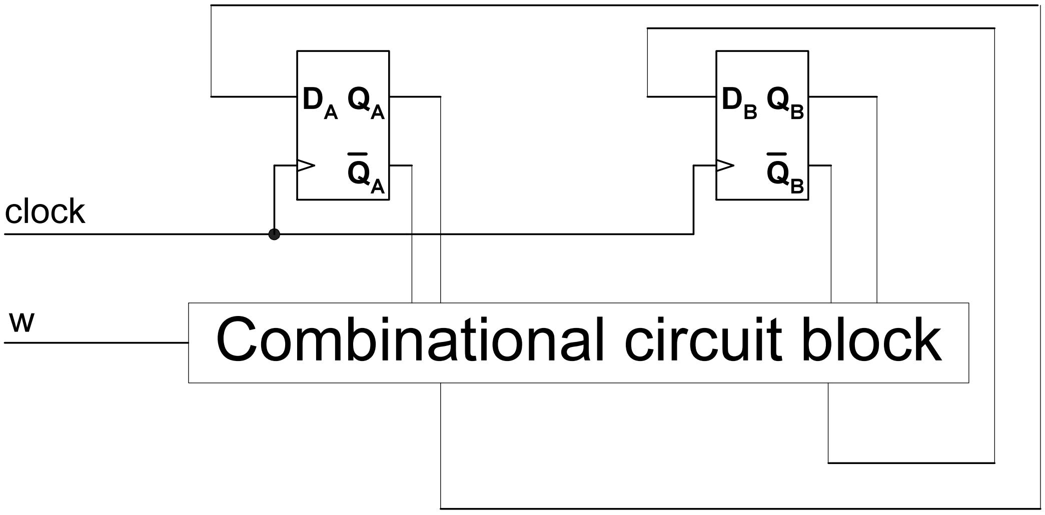


Figure 12 - Circuits for question 17.

w	Present State	Next State
0	00	10
0	01	00
0	10	11
0	11	01
1	00	01
1	01	11
1	10	00
1	11	10

(a)



(b)

Figure 13 - State table and circuit for questions 18 and 19 (Q_A is the most significant bit). Tip: Use K-maps for logic minimization.

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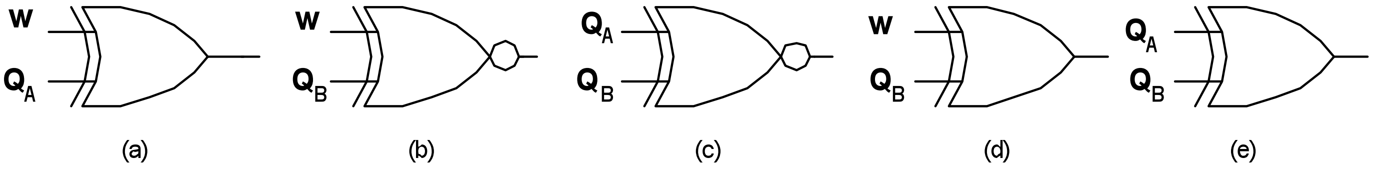

Figure 14 - Circuit implementations for questions 18 and 19.

18. Consider the state transition table of a two-bit up/down Gray-code counter, where the counting direction is controlled using an external input **w**, as shown in Figure 13(a) (see previous page). If in our technology library we have only **D** flip-flops then a generic implementation is shown Figure 13(b). Based on the state transition table and circuit topology shown in Figure 13, the logic function which drives the *input* **D_A** *of the leftmost flip-flop from Figure 13(b)* is shown in:

1. Figure 14(a)
[✓ 2.] Figure 14(b)
3. Figure 14(c)
4. Figure 14(d)
5. Figure 14(e)

19. Consider the state transition table of a two-bit up/down Gray-code counter, where the counting direction is controlled using an external input **w**, as shown in Figure 13(a) (see previous page). If in our technology library we have only **D** flip-flops then a generic implementation is shown Figure 13(b). Based on the state transition table and circuit topology shown in Figure 13, the logic function which drives the *input* **D_B** *of the rightmost flip-flop from Figure 13(b)* is shown in:

[✓ 1.] Figure 14(a)
2. Figure 14(b)
3. Figure 14(c)
4. Figure 14(d)
5. Figure 14(e)

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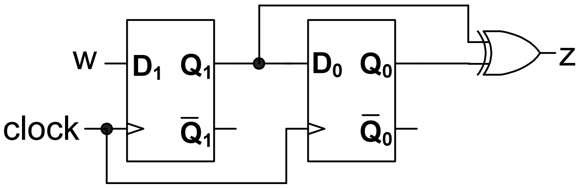
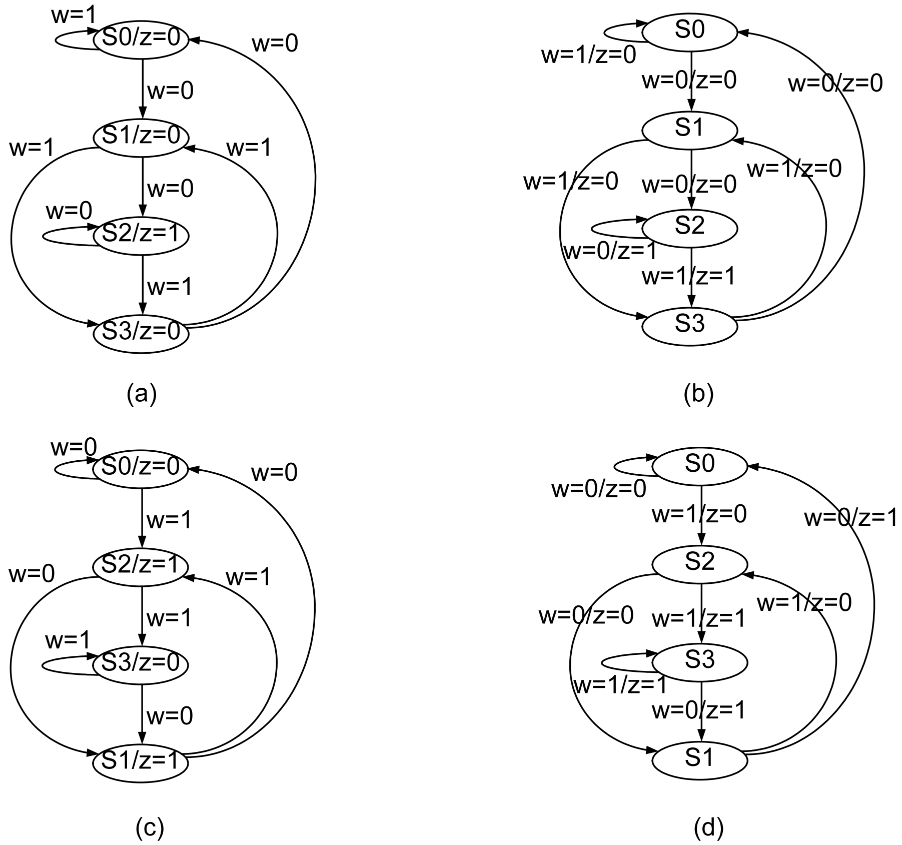


Figure 15 - Circuit for question 20.

20. Consider the sequential circuit shown in Figure 15. Consider the following state assignment: **S0** stands for $\mathbf{Q_1Q_0}$=00, **S1** stands for $\mathbf{Q_1Q_0}$=01, **S2** stands for $\mathbf{Q_1Q_0}$=10 and **S3** stands for $\mathbf{Q_1Q_0}$=11. The state transition diagram for the circuit from Figure 15 is shown in:

1. Figure 16(a)
2. Figure 16(b)
[✓ 3.] Figure 16(c)
4. Figure 16(d)
5. none of the above



(a) (b)

(c) (d)

Figure 16 - State transition diagrams for question 20.

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