Logic Design

Outline

Topics

- ***Binary Numbers***
  - Unsigned binary numbers, base conversions, representation of negative numbers, binary arithmetic
- ***Boolean Algebra, Digital Logic and Electrical Properties of Logic Gates***
  - Introduction to Boolean algebra, truth tables and logic gates
  - Propagation delay, signal levels, noise margins, fan-in, fan-out, glitches
- ***Combinational Circuit Design***
  - Circuit simplification using K-maps, ripple carry adders, carry look-ahead adders
  - Design of basic building blocks such as decoders, multiplexers, encoders, comparators

Topics

- ***Implementation technology and programmable logic***
  - Complementary metal-oxide semiconductors (CMOS) technology
  - Programmable logic arrays (PLA), field programmable gate arrays (FPGA), read only memories (ROM)
  - Introduction to hardware description languages (VHDL)
- ***Sequential Circuit Design***
  - Latches, flip-flops, counters, shift registers, state diagrams and tables
  - Control logic implementation using finite state machines (FSM)
- ***Introduction to Computer Organization***
  - Central processing unit (CPU), arithmetic and logic unit (ALU), register files
  - Register transfer logic; microoperations and microprograms

Textbook & Assessment

- Textbook:
  - ***"Fundamentals of Digital Logic with VHDL Design, third edition"*, by Brown & Vranesic, 2009.**
- We will cover chapters 1 to 8 (maybe 9).
- Chapters are not covered in the order of the book.
- Tests: In addition to the final exam, there will be ***two compulsory*** midterm tests on October 14 and November 9.
- *Students who miss the midterms, and who have a valid excuse will be accommodated. Those who do not have a valid excuse will be assessed zero for the midterm components of the final grade.*
- Assessment:
  - Labs **10** %
  - Midterm Test #1 **20** %
  - Midterm Test #2 **20**%
  - Final Examination **50** %

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Labs

- You will work in groups of 2.
- The five lab sessions are:
  1. Logic Gates
  2. Combinational Logic Design
  3. Programmable Logic
  4. Sequential Logic Design
  5. Design of a Register File and Datapath

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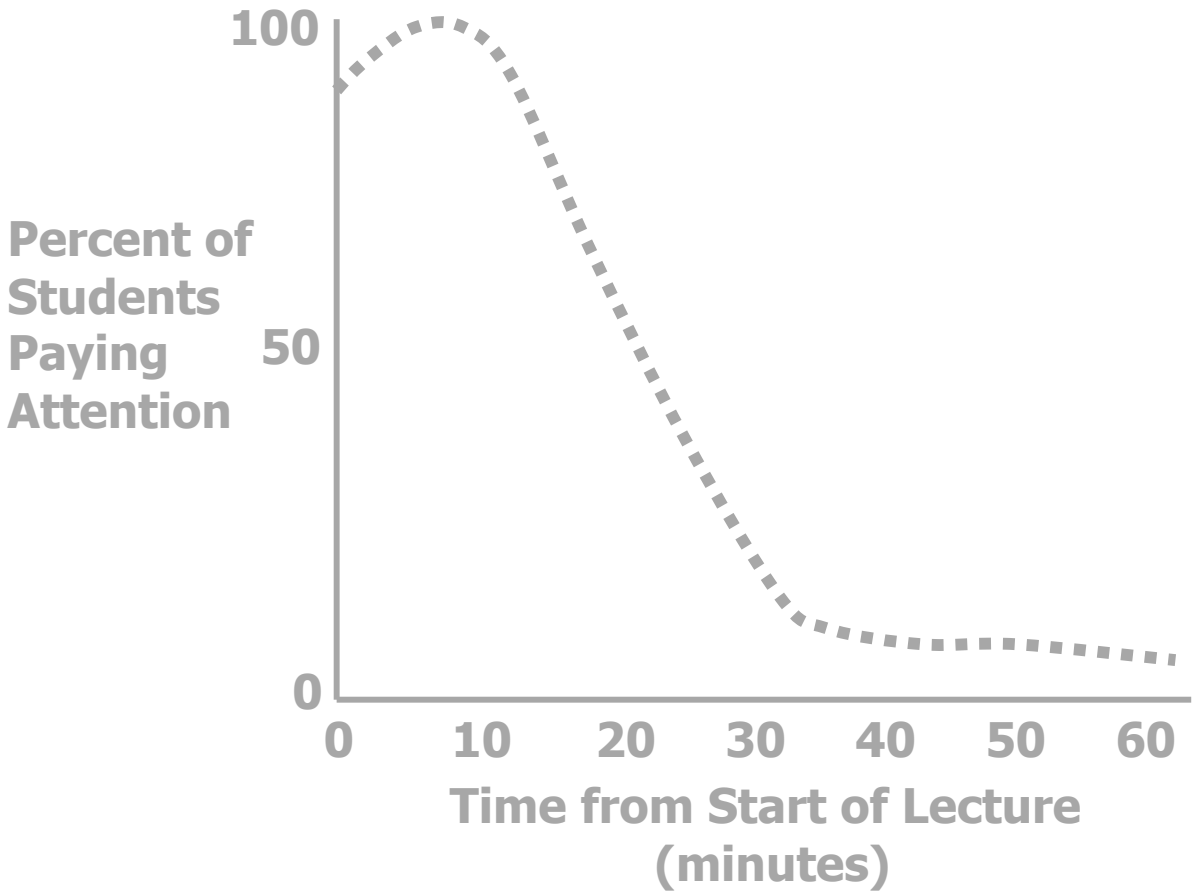
Fact 1

- People only remember the first 15 minutes of what you say



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Fact 2

- The only way a skill is developed - skiing, cooking, writing, critical thinking, or solving logic design problems—is practice: trying something, seeing how well or poorly it works, reflecting on how to do it differently, then trying it again and seeing if it works better.

Our approach to learning Digital Logic

- An instructional methodology that takes students out of the passive mode and involves them actively in classroom learning: active/cooperative learning
- Data shows students taught in this way have higher GPAs, higher retention and graduation rates, and better attitudes about the program, the discipline, and themselves.
- Employers consider "good team skills" an important attribute. Enthusiastically participating in the in-class exercises will provide practice with this important skill in a technical setting

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Active learning

- I will ask you to do something
  - Solve problem
  - Generate questions
  - Working through derivations
- I will tell you to work individually, in pairs, or in groups of three or four (students in adjacent seats constituted the groups)
- I will tell you how long you will have (anywhere from 3 to 10 minutes).
- I will then call on one or two groups or individuals or ask for volunteers to tell what they came up with.

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Learning by Doing

- Practice, Practice and Practice! Need not be afraid of failures
  - No hostile spectators
- We never forget riding a bike- because we learn after many failures.

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Reminders

- Attend your assigned lab section
  - TAs will not give you a mark for the lab if you attend another lab section
- Do not miss a lab
  - Due to the size of class there is no possibility of makeup labs
- Labs are on alternative weeks
- If you are in lab section #6, your second lab will be on Thanksgiving.
- You have to attend another section and do second lab between Oct. 4 and Oct. 14.
- Two tutorial sessions are the same (a re-run). Attend one that you like.

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FAQ

- Can I use the second edition of the book?
  - Yes.
  - Little difference between 2nd and 3rd edition
  - My references to an equation or a problem in the book are based on 3rd edition.
- Do I need the CD?
  - No, we have the CAD tool on the machines in the lab
- Is there programming in this course?
  - We cover a little of a hardware description language called VHDL
- Will you post your slides?
  - I will do my best to post the slides for each chapter before we start that chapter