

NAME _____

STUDENT NUMBER _____

COMPUTER ENGINEERING 3DR4

DAY CLASS

DURATION OF EXAMINATION: 3 Hours

McMaster University Final Examination

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This examination paper includes 6 pages, 7 questions (including a bounce question) and “MIPS Reference Data”. You are responsible for ensuring that your copy of the paper is complete. Bring any discrepancy to the attention of your invigilator.

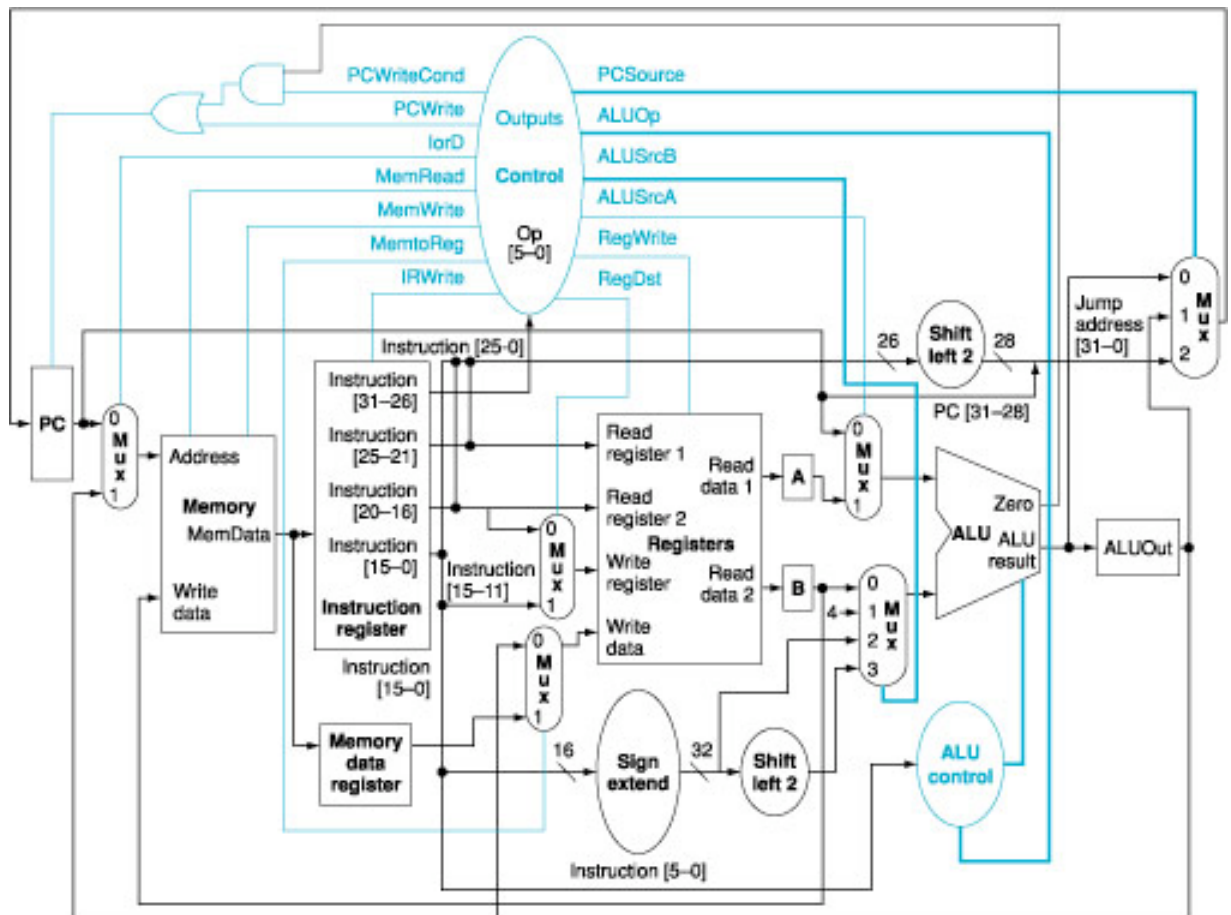
SPECIAL INSTRUCTIONS:

Write your name and student number at the top of every page. Answer all questions in the **ANSWER BOOKLET ONLY**. This is a **closed book** examination. No reference materials of any kind are permitted. Any calculators may be used.

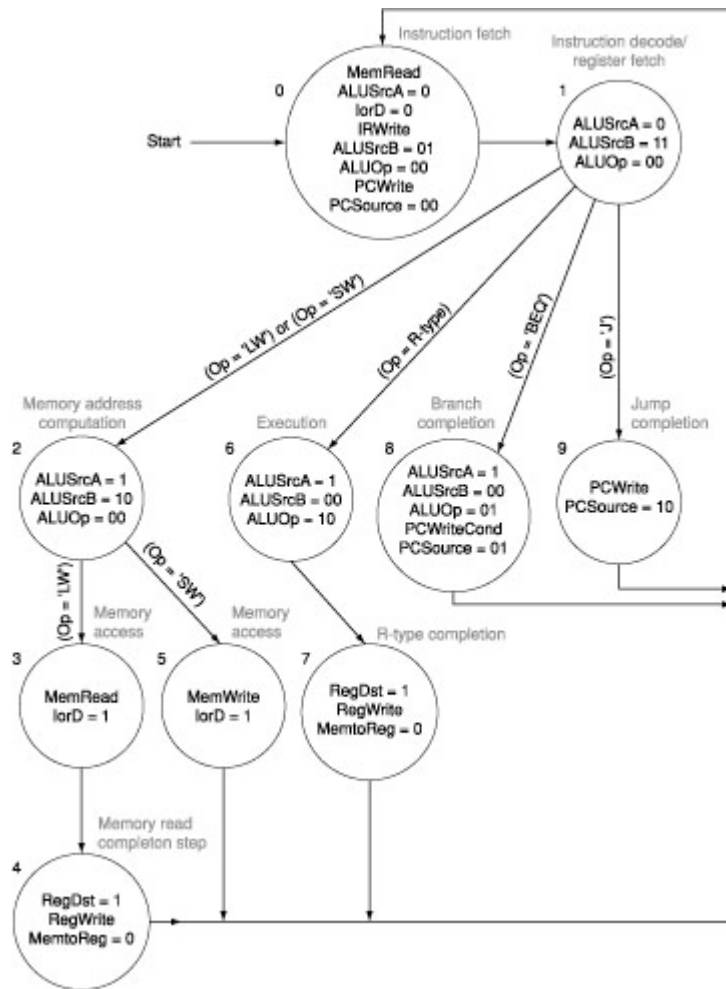
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Question 1 (5 points)

We wish to add a new instruction, wai (where am I), which puts the instruction's location (the value of the PC when the instruction was fetched) into a register specified by the rt field of the machine language instruction to the multicycle implementation of MIPS processor. Assume that the datapath hasn't changed and that, as usual, the clock cycle is too short to allow an ALU operation and a register file access in a single clock cycle if one of them is dependent on the results of the other. Show the necessary modifications to the finite state machine (given below).



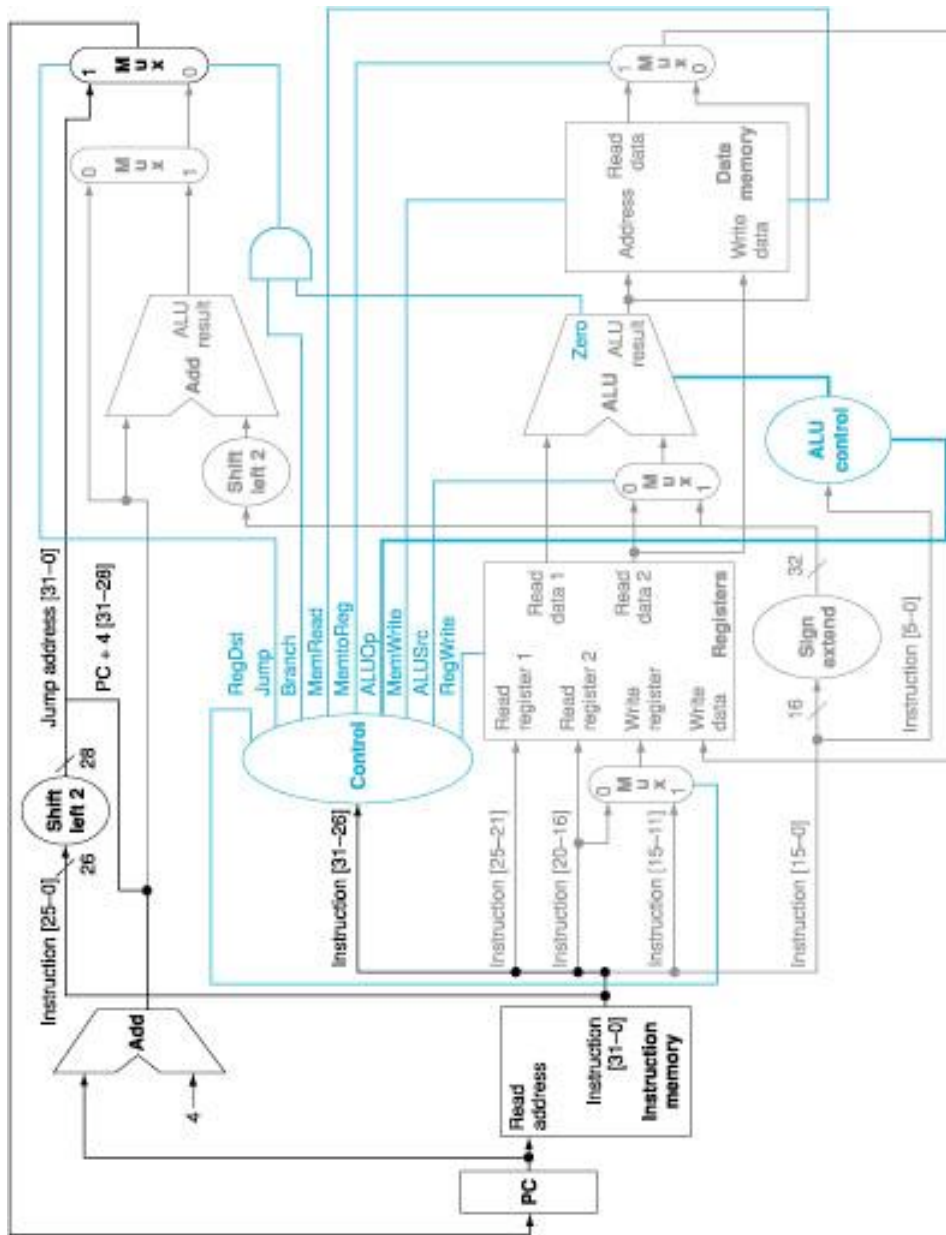
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Question 2 (5 points)

We wish to implement a new instruction `ldi` (load immediate) that loads a 32-bit immediate value from the memory location following the instruction address to the single-cycle datapath. Add any necessary datapaths and control signals to the single-cycle datapath (shown below) and show the necessary additions to the control line table (given below).

Instruction	RegDst	ALUSrc	MemtoReg	Reg	Memread	Mem	Branc	ALUO	ALUO
R-format	1	0	0	1	0	0	0	1	0
lw	0	1	1	1	1	0	0	0	0
sw	x	1	x	0	0	1	0	0	0
beq	x	0	x	0	0	0	1	0	1



Question 3 (5 points)

Consider three processors with different cache configurations:

Cache 1: direct-mapped with one word blocks

Cache 2: direct mapped with four word blocks

Cache 3: two-way set associative with four word blocks

The following miss rate measurements have been made

Cache 1: instruction miss rate is 4%, data miss rate is 6%

Cache 2: instruction miss rate is 2%, data miss rate is 4%

Cache 3: instruction miss rate is 2%, data miss rate is 3%

For these processors, one half of the instructions contain a data reference. Assume that the cache miss penalty is 6+ block size in words. The CPI for this workload was measured on a processor with cache 1 and was found to be 2.0 (this is a measured value and includes cache misses).

1. Determine which processor spends the most cycles on cache misses.
2. The cycle times for processors one, two and three are 420, 420 and 310 ps, respectively. Determine which one is the fastest and which is the slowest.

Question 4 (5 points)

Consider executing the following code on the MIPS pipeline datapath:

lw \$4, 100(\$2)

sub \$6,\$4,\$3

add \$2,\$3, \$5

add \$5,\$3,\$7

add \$7,\$6,\$1

1. At the end of the fifth cycle of execution, which registers are being read and which registers will be written?
2. Explain what the forwarding unit is doing during fifth cycle of execution. If any comparisons are being made, mention them.
3. Explain what the hazard detection unit is doing during fifth cycle of execution. If any comparisons are being made, mention them.

Question 5 (5 points)

Consider a virtual memory system with the following properties:

40-bit virtual byte address

16 KB pages

36-bit physical byte address

What is the total size of the page table for each process on this processor, assuming that the valid, protection, dirty and use bits take a total of 4 bits and that all the virtual pages are in use? (Assume that disk addresses are not stored in the page table).

Continued on Page 6

Question 6 (5 points)

Here are two different I/O systems intended for use in transaction processing:

System A can support 1500 I/O operations per second

System B can support 1000 I/O operations per second

The systems use the same processor that executes 500 million instructions per second. Assume that each transaction requires 5 I/O operations and that each I/O operation requires 10,000 instructions. Ignore response time and assume that transactions may be arbitrarily overlapped. What is the maximum transaction-per-second rate that each machine can sustain?

Bounce Question (5 points)

Suppose there were a MIPS instruction called `bcmp`, that compares two blocks of words in two memory addresses. Assume that this instruction requires that the starting address of the first block is in register `$t1` and the starting address of the second block is in `$t2` and the number of words to compare is in `$t3` (which is $t3 > 0$). Assume that the instruction can leave the result (the address of the first mismatch or zero if a complete match) in `$t1` and/or `t2`. Furthermore, assume that the values of these registers as well as registers `$t4` and `$t5` can be destroyed in executing this instruction.

1. Write the MIPS assembly language program to implement block compare.
2. How many instructions will be execute to compare two 100-word blocks?
3. How many cycles are needed for 100-word block compare? (Assume that CPI for R-type instructions is 4, for `lw` is 5, for `sw` is 4 and for branch and jump is 3)

"THE END"