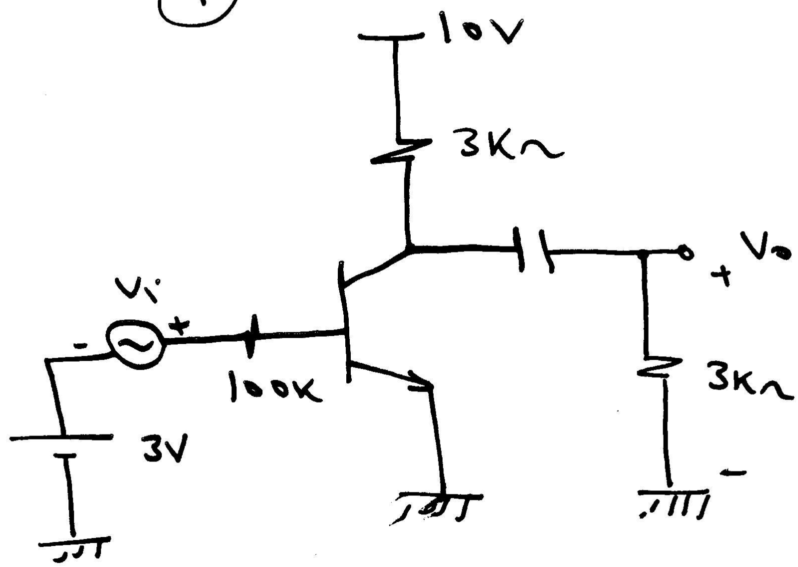
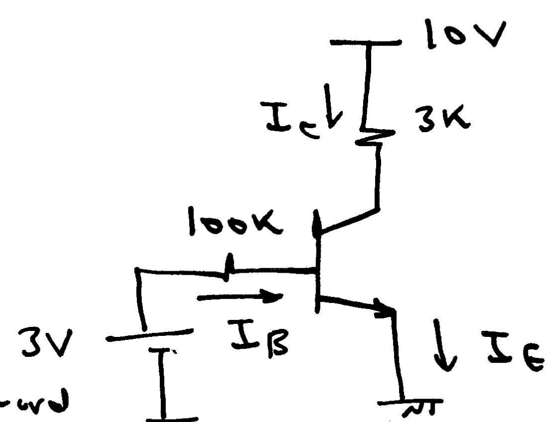
(1)



if $\beta = 100$, what is $\frac{V_o}{V_i}$?

ANSWER: WE START BY THE DC analysis



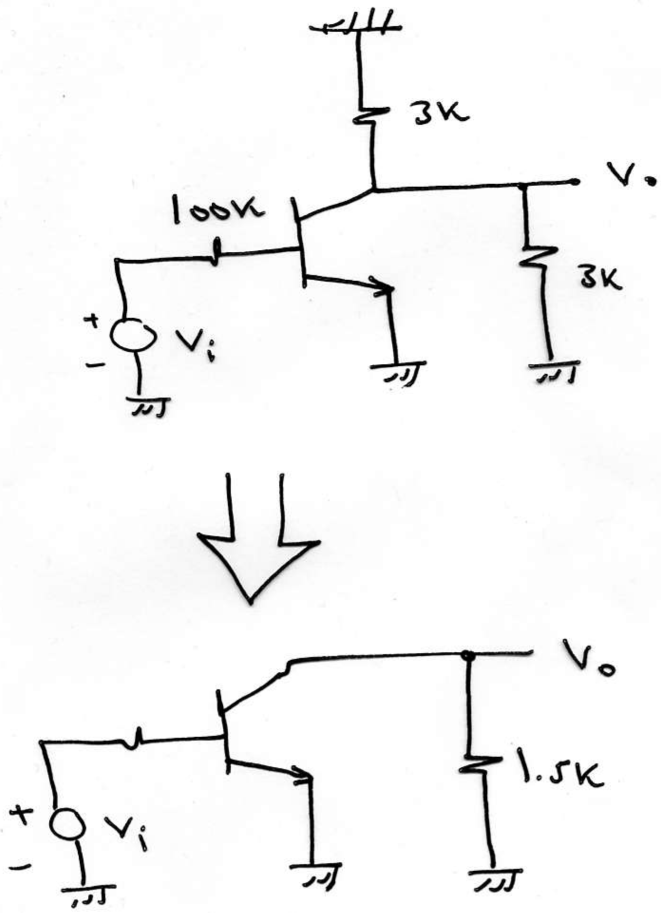
Assuming Forward active region

$$I_B = \frac{3-0.7}{100K} = 23\mu A$$

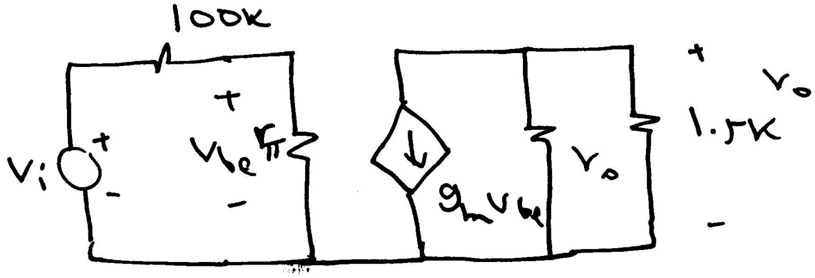
$$\therefore I_c = \beta I_B = 2.3mA \Longrightarrow V_c = 10 - 6.9$$
$$= 3.1V$$

$\therefore$ $V_C > V_B$ and our assumption is valid

AC Analysis



(3)



$$g_m = \frac{I_C}{V_T} = \frac{2.3}{25} = 0.092\ \text{A/V}$$

$$r_o = \frac{V_A}{I_C} = \infty$$

$$r_\pi = \frac{\beta}{g_m} = \frac{100}{0.092} = 1.086\ \text{k}\Omega$$

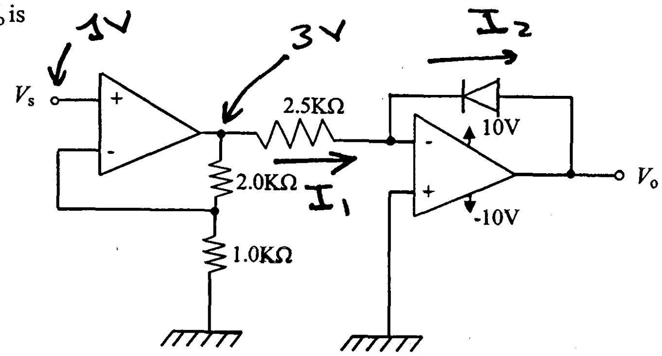
$$\therefore \quad \frac{V_o}{V_i} = -g_m * 1.5K * \frac{r_\pi}{r_\pi + 100K}$$

$$\frac{V_o}{V_i} = -0.092 * 1.5e3 * \frac{1.086}{1.086 + 100K}$$

$$\therefore \quad \frac{V_o}{V_i} = -1.48$$

Student Name: ID Number:

1) For the shown circuit the diode reverse saturation current is $I_s = 10^{-15}$ A. If $V_s = 1.0$ V, V_o is



a) 0.6852 V
b) -0.6852 V
c) 0.755 V
d) -0.755V
e) -10V

$$as\ I_1 = I_2$$

$$\therefore I_2 = 0$$

$$V^- = 3V,\ V^+ = 0V \Rightarrow V_o = -10V$$

2) If the input in problem (1) is V_s=-1.0 V, the output voltage V_o is equal to

a) 0.6852 V
b) -0.6852 V
c) 0.755 V
d) -0.755V
e) -10V

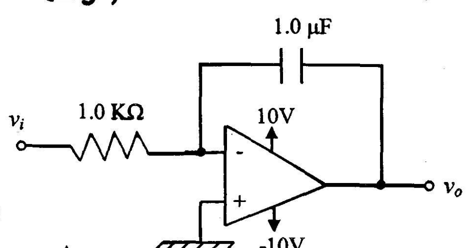
$$V_{o1} = -3V \Rightarrow I_1 = \frac{-3}{2.5K} = -1.2mA$$

$$\therefore I_D = 1.2mA.$$

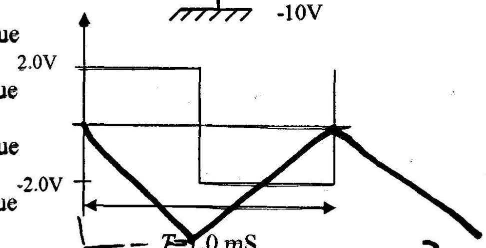
$$\therefore V_D = V_T \ln\left(\frac{I_D}{I_s}\right) = 0.6952V$$

$$V_o = V_D$$

3) The input to the shown circuit is a square waveform with an amplitude of 2.0 V. The output v_o as observed on the scope is



a) a triangular waveform with a peak-to-peak value of 1.0 V and frequency 1.0 KHz.
b) a triangular waveform with a peak-to-peak value of 2.0 V and frequency 1.0 KHz.
c) a triangular waveform with a peak-to-peak value of 2.0 V and frequency 2.0 KHz.
d) a triangular waveform with a peak-to-peak value of 2.0 V and frequency 0.5 KHz.
e) a triangular waveform with a peak-to-peak value of 0.5 V and frequency 1.0 KHz.

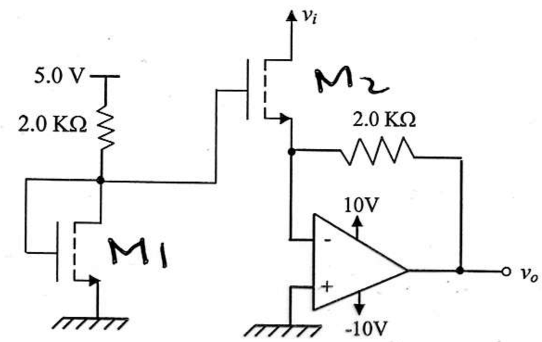


$$V_c = \frac{1}{C}\int i\,dt = \frac{i\Delta t}{C} = \frac{2.0\times10^{-3}\times0.5\times10^{-3}}{1.0\times10^{-6}} = 1V$$

$$\therefore V_o = -V_c$$

Student Name: ID Number:

4) The enhancement NMOS transistors in the shown circuit have K_n=1.0 mA/V^2, V_{TN}= 1.0 V and λ = 0 V^{-1}. If V_i is equal to 3.0 V, then V_o is equal to



a) 2.43 V
b) -2.43 V
c) 0 V
d) -1.21 V
e) -10 V

$V_{GS2} = V_{GS1}$

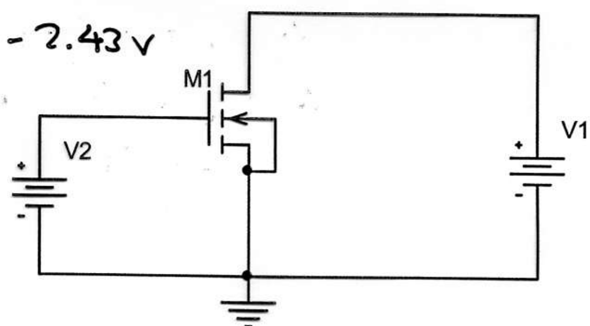
$$\frac{5 - V_{GS}}{2K} = 0.5*10^{-3}(V_{GS} - 1)^2$$

$5 - V_{GS} = (V_{GS} - 1)^2 \Rightarrow V_{GS} = 2.56$ V

$I_{DS1} = 1.219$ mA

$V_o = -I_{DS2}*2K = -2.43$ V

5) The shown circuit is connected in the lab to determine the characteristics of the MOS transistor. The current measurements are shown in the table below. The threshold voltage and transistor transconductances are



a) 1.0 V, 1.0e-3
b) 1.0 V, 2.0e-3
c) -1.0 V, 1.0e-3
d) -1.0 V, 2.0e-3
e) 0.5 V, 2.0e-3

	VGS=2V	VGS=3V
VDS=0 V	0 A	0A
VDS=1 V	0.5 mA	1.5 mA
VDS=2 V	0.5 mA	2.0 mA
VDS=3 V	0.5 mA	2.0 mA
VDS=4 V	0.5 mA	2.0 mA

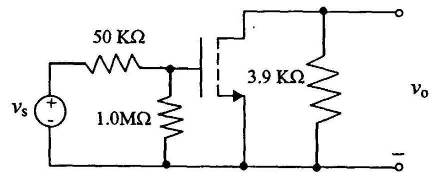
$$0.5 = \frac{K_n}{2}(2 - V_{TN})^2$$

$$2.0 = \frac{K_n}{2}(3 - V_{TN})^2$$

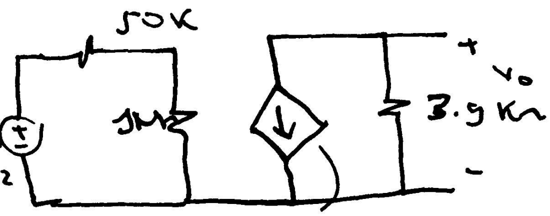
Solve to get $V_{TN} = 1.0$ V, $K_n = 1.0e\text{-}3$

Student Name: ID Number:

6) The figure to the right shows the ac equivalent circuit of an NMOS amplifier with K_n=1.0 mA/V^2, V_{TN}=1.0 V and λ=0 V^{-1}. The operating point is (I_{DS}, V_{DS})=(2.0 mA ,7.5 V). If the ac source is v_s=0.1 sin(2π×10^3t)V, the maximum and minimum values of the total drain-to-source voltage v_{DS} are approximately



a) 0.74 V, -0.74 V
b) 8.24 V, 7.76 V
c) 8.24 V, 6.76 V
d) ~~7.76 V, 6.76 V~~
e) None of the above



$g_m = \sqrt{2K_n I_{Dr}} = 2mA/V^2$

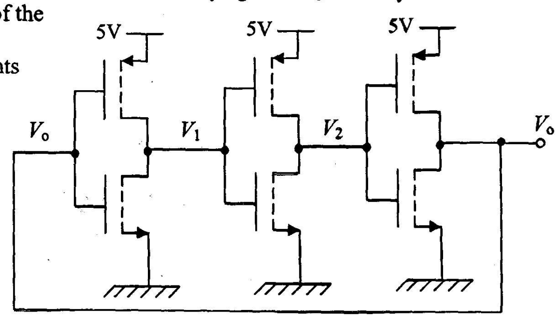
$A_v = -g_m * 3.9K * \frac{1M}{1M+50K}$

$A_v = -7.4$

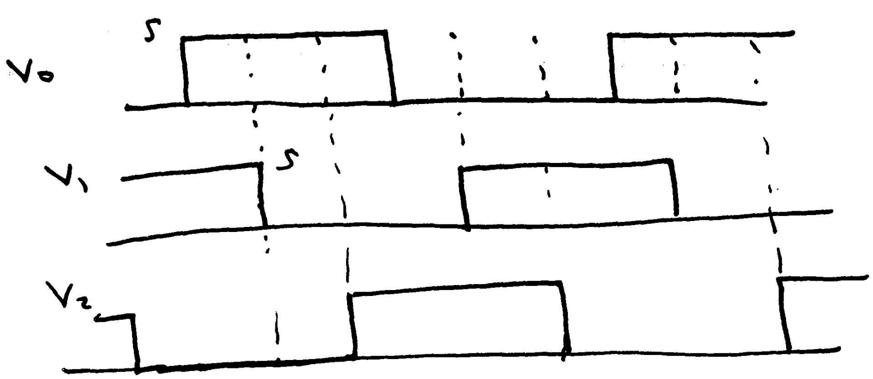
$V_o = -0.74 \sin\omega t \Longrightarrow 7.5+0.74$

$7.5-0.74$

7) The propagation delay in each one of the inverter stages in the shown circuit is t_p. Which one of the following statements is correct?

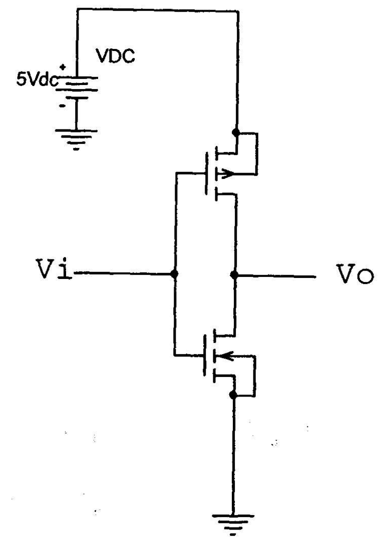


a) $V_1(t)=V_o(t-2t_p)$
b) $V_1(t)=V_2(t+2t_p)$
c) $V_o(t)=V_2(t-2t_p)$
d) $V_o(t)=V_1(t-2t_p)$
e) $V_2(t)=V_1(t-2t_p)$

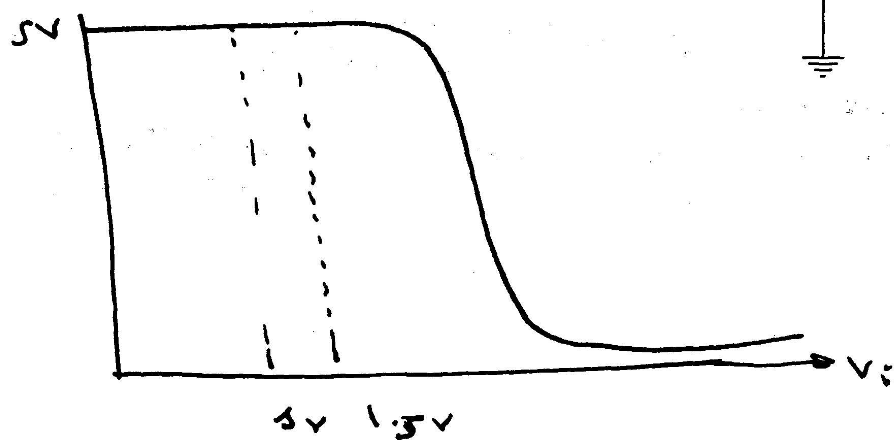


Student Name: ID Number:

8) The circuit to the left shows a circuit diagram of a CMOS inverter. The threshold voltages for the NMOS and PMOS transistors are 1.0 V and -1.0 V, respectively. Their transconductances are $K_n = K_p = 2.0$ mA/V^2. If $V_i = 1.5$ V, which one of the following statements is true?



a) The NMOS transistor is saturated and the PMOS transistor is saturated
b) The NMOS transistor is in the linear region and the PMOS transistor is saturated
c) The NMOS transistor is saturated and the PMOS transistor is in the linear region.
d) The NMOS transistor is on and the PMOS transistor is off
e) None of the above



or let $I_{DS} = \frac{K_n}{2}(1.5-1)^2$

& solve $I_{SD} = I_{DS} = K_p\left(V_{SG}+V_{Tp}+\frac{V_{SD}}{2}\right)V$