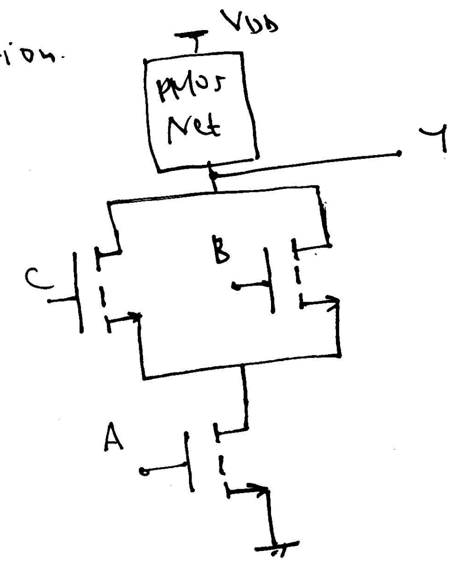
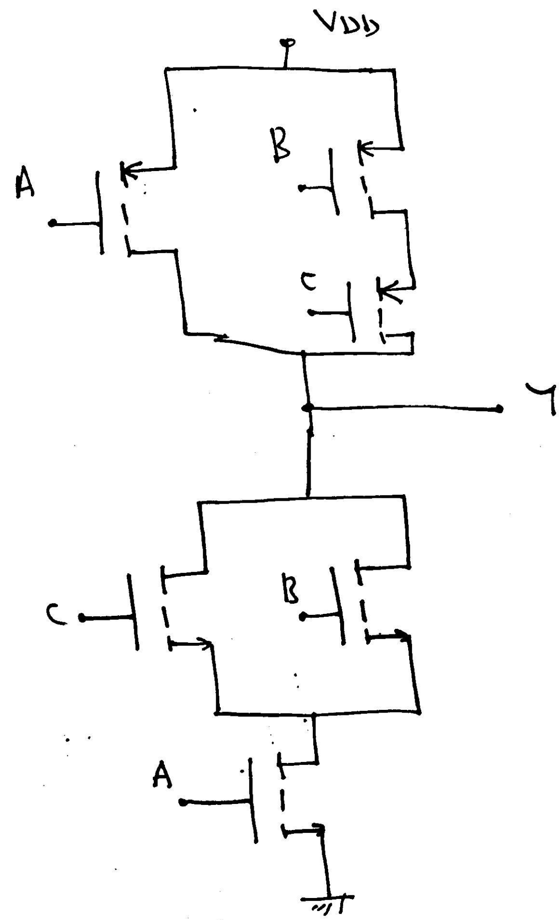
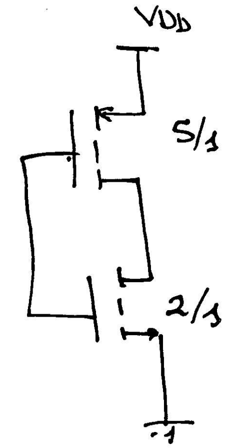
* Design a CMOS Logic gate that implements the logic function $Y = \overline{AB + AC}$. Design the differe delays in the circuit to match that of a reference inverter.

<u>ANSWER</u> NMOS network supplies the Zeros of the function.



Connections are reversed for the PMOS Network





$$R_{on,n} = R_{on1} + R_{on2}$$

$$\frac{1}{\left(\frac{W}{L}\right)_{eq}} = \frac{1}{\left(\frac{W}{L}\right)_1} + \frac{1}{\left(\frac{W}{L}\right)_2}$$

$$\frac{1}{(2/1)} = \frac{1}{\left(\frac{W}{L}\right)_1} + \frac{1}{\left(\frac{W}{L}\right)_2}$$

$$\Longrightarrow \left(\frac{W}{L}\right)_{A,N} = \left(\frac{W}{L}\right)_{B,N} = \left(\frac{W}{L}\right)_{C,N} = 4/1$$

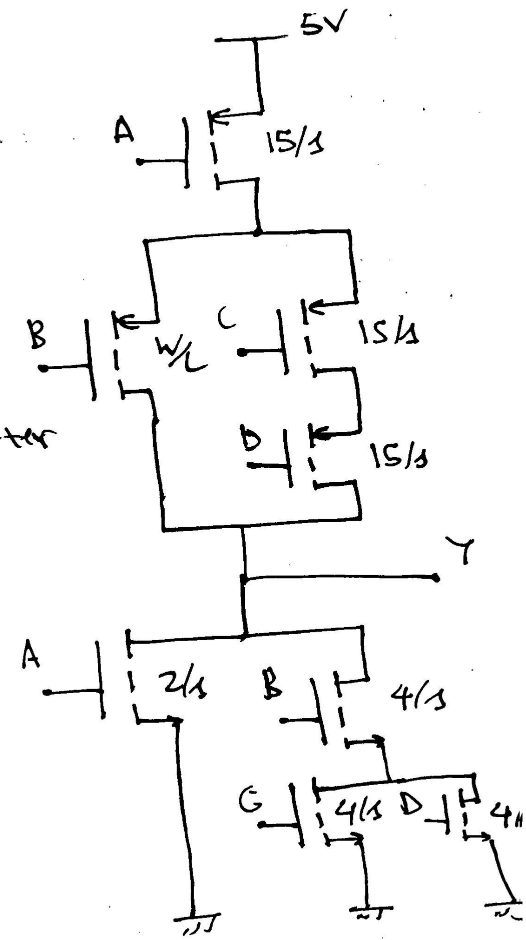
for the PMOS part, we have

$$\frac{1}{\left(\frac{W}{L}\right)_{eq}} = \frac{1}{\left(\frac{W}{L}\right)_1} + \frac{1}{\left(\frac{W}{L}\right)_2}$$

$$\frac{1}{(5/1)} = \frac{1}{\left(\frac{W}{L}\right)_1} + \frac{1}{\left(\frac{W}{L}\right)_2} \Rightarrow \left(\frac{W}{L}\right)_{A,p} = \left(\frac{W}{L}\right)_{B,p} = \left(\frac{W}{L}\right)_{C,p} = 10/1$$

---

* What is the logic function implemented by the shown gate?
* What is W/L to have a worst case delay equal to that of a reference CMOS Inverter



---

* Zeros of the function determine its nature

$$Y = \overline{A + BC + BD}$$

* To get worst case delay equivalent to that of a reference inverter, we must have

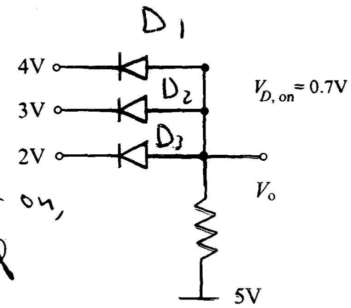
$$\frac{1}{(5/1)} = \frac{1}{(\frac{W}{L})_A} + \frac{1}{(\frac{W}{L})_B}$$

$$\frac{1}{(5/1)} = \frac{1}{(15/1)} + \frac{1}{(\frac{W}{L})_B}$$

$$\frac{1}{(\frac{W}{L})_B} = \frac{1}{(15/2)} = \frac{1}{(7.5/1)}$$

Student Name: ID:

1) The value of V_o for the shown circuit is

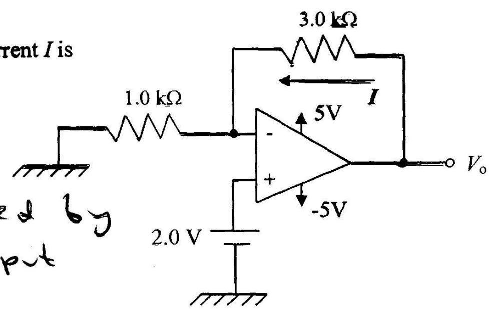


a) 5.0 V
b) 4.7 V
c) 3.7 V
d) 3.3 V
e) 2.7 V

The only consistent state is that D_3 is on, D_1 and D_2 are off

$\Rightarrow V_o = 2.7V$

2) In the shown circuit, the value of the current *I* is



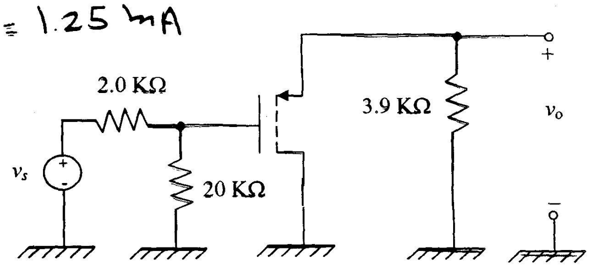
a) -1.25 mA
b) 2.0 mA
c) 1.25 mA
d) -2.0 mA
e) -1.5 mA

The output is saturated by the 2V input

$\Rightarrow V_o = 5V$

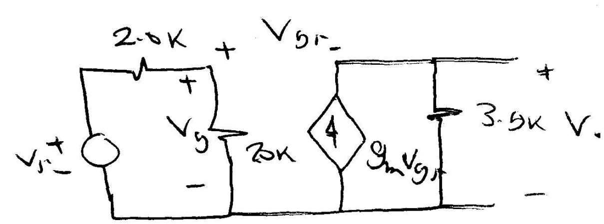
$\therefore I = \frac{5}{4K} = 1.25\ mA$

3) The circuit to the right shows the ac equivalent circuit of an amplifier. The transistor has an operating point (I_{SD}, V_{SD})=(2.0 mA, 6.0 V). The parameters of the transistor are K_p=1.0 mA/V^2, λ=0 V^{-1} and V_{TP}=-1.0 V. The small signal gain v_o/v_s is equal to



a) 7.800
b) -7.800
c) 0.886
d) 0.805
e) 0.655

$g_m = 2mA/V$



$V_o = g_m V_{gs} * 3.9K$

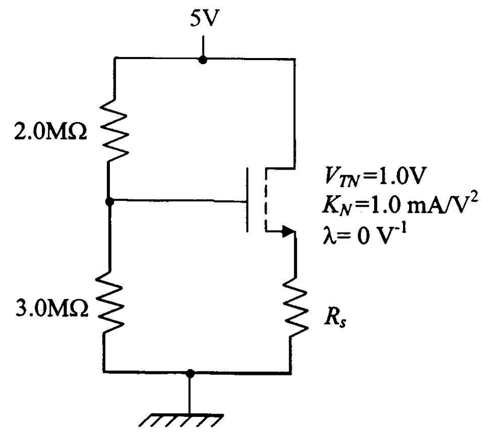
$= g_m (V_g - V_o) * 3.9K$

$8.8 V_o = 7.8 V_g \Rightarrow V_o = \frac{7.8}{8.8} V_g$

$\Rightarrow V_o = \frac{7.8}{8.8} * \frac{20}{22} V_s \Rightarrow A_v = 0.805$

Student Name: ID:

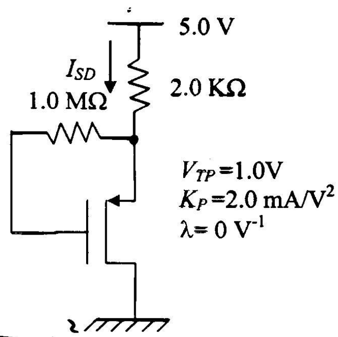
4) What is the largest value of R_s such that the transistor remains on and saturated?



a) 1.5 KΩ
b) 2.5 KΩ
c) 3.5 KΩ
d) 4.5 KΩ
e) None of the above

transistor is always on and saturated

5) The current I_{SD} is equal to



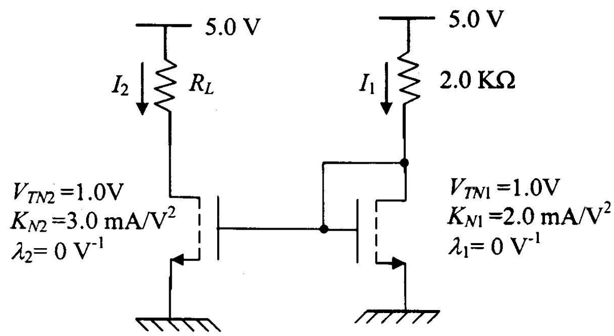
a) 0 mA
b) 1.0 mA
c) 1.5 mA
d) 2.5 mA
e) None of the above

$V_{SG} = 0 > -V_{TP}$

∴ transistor is on

$$I_{SD} = \frac{K_P}{2}(V_{SG} + V_{TP})^2$$
$$= 1.0\times10^{-3}(1)^2 = 1.0\text{mA}$$

6) For the shown circuit, if the resistor R_L is small enough, the current I_2 is



a) 1.406 mA
b) 2.110 mA
c) 2.855 mA
d) 1.000 mA
e) 3.367 mA

~~Ans~~ $\frac{5 - V_{GS}}{2.0K} = \frac{K_N}{2}(V_{GS} - V_{TN})^2$

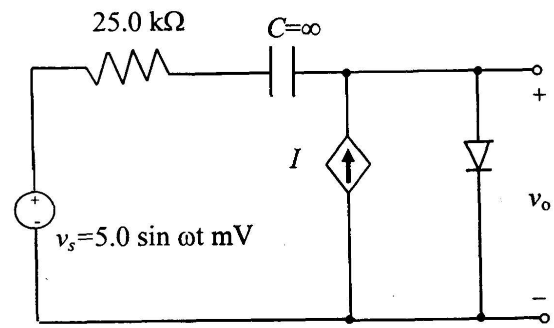
$$\frac{5 - V_{GS}}{2K} = 10^{-3}(V_{GS} - 1)^2$$

$$5 - V_{GS} = 2(V_{GS} - 1)^2 \Rightarrow V_{GS} = 2.186\text{ V}$$

$I_1 = 1.406\text{mA}$ $I_2 = 2.11\text{mA}$

Student Name: ID:

7) The diode in the shown circuit has a reverse current I_s=1.0e-12 A.
If the DC current I is equal to 1.0 μA, the total voltage v_o appearing across the diode is



a) 0.345+0.0025 sinωt V
b) 0.707 +0.0025 sinωt V
c) 0.345-0.0025 sinωt V
d) 0.707 -0.0025 sinωt V
e) 0.345+0.003 sinωt V

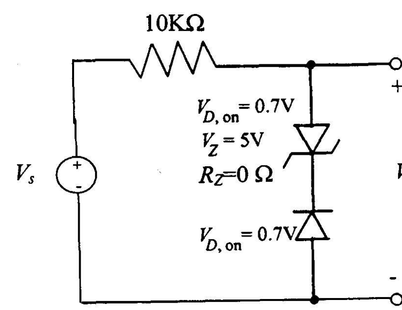
DC Analysis $I = I_s \exp\left(\frac{V_D}{V_T}\right) \Rightarrow V_D = V_T \ln \frac{I}{I_s}$

$V_D = 0.345 V$

$\frac{\partial I}{\partial V_D} = \frac{I_s \exp\left(\frac{V_D}{V_T}\right)}{V_T} \Rightarrow R_D = \left(\frac{\partial I}{\partial V_D}\right)^{-1} = \frac{V_T}{I_D}$

$R_D = \frac{0.025}{10^{-6}} = 25K \Rightarrow V_o = 0.345 + 2.5 \sin\omega t$ mA

8) The source V_s is a sinusoidal source with an amplitude of 10 volts. The minimum and maximum values of the output voltage V_o are, respectively,



a) -1.4 V, 4.3V
b) -4.3 V, 10 V
c) -5.7 V, 10V
d) -5.7 V, 1.4V
e) -1.4 V, 5.7V

for positive voltage both diodes are off and $V_{o,max} = 10V$

$< -5.7V$

for negative voltage Zener is breakdown and diode is forward biased

$V_{o,min} = -5.7V$