Testing of First and Second Order Delta-Sigma Converters for Catastrophic Faults

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***Abstract*—Delta-Sigma analog to digital converters are vital components for mixed-signal systems. So, testing this type of converters is extremely important. This paper studies the low-cost testing of first-order and second-order delta-sigma ADCs. Moreover; only catastrophic faults are considered such as open/short passive components and stuck-at faults in digital components. It is proven that the minimal test set consists of only two values that detect all faults in the assumed fault set. The effect of using different types of counters in the digital subcircuit is investigated and it is found that the two-value test set still detects all faults. Finally, the effect of passive component tolerances is analyzed. All the results are analytically proven and verified by simulations.**

***Index Terms*—Delta-Sigma ADC, mixed signal circuit, testing, fault model, second order ADC.**

I. Introduction

Unlike Nyquist rate converters, such as successive approximation ADCs [1] and flash ADCs [2], which provide low to medium resolution for high bandwidth, delta-sigma converters can achieve high resolution for low to medium bandwidths. Although the delta-sigma conversion method has been known for many years, its importance increased after the exceptionally high speeds achieved with modern VLSI technologies [3].

A delta-sigma ADC simplifies system integration with modern technologies as it, in contrast to other conversion types, does not depend on a bulky analog circuit. It does not need the anti-aliasing filters nor the sample and hold circuitry found in other types. Another advantage is the low-cost conversion as it can convert analog signals to the digital domain using only 1-bit ADC and a simple analog circuit [4].

Because of the importance of the delta-sigma ADC, it is crucial to develop a high-quality low-cost test procedure. Unlike the Built-In Self-Test (BIST) techniques as the one described in [5], a low cost test method was described in [6] for a simple implementation of a first-order delta-sigma ADC. The test set consisted of only two test values. In addition, no BIST circuitry was required. In this paper, a different implementation of the first-order delta-sigma is studied and it will be shown that the same two test values mentioned in [6] still detect all the faults in the assumed fault set. The effect of passive component tolerances is then investigated and it is found that the suggested test set can still detect all faults for certain combinations of component values. Finally, an implementation of a second-order delta-sigma ADC is analyzed and it will be proven that the same two test values detect all the faults in the assumed fault set even if the passive components deviate somehow from their nominal values due to the inherent tolerances.

This paper is organized as follows. Section II describes the operation of a basic first-order delta-sigma converter and previous work in the context of testing. Section III studies a slightly different implementation of this ADC and investigates components tolerances. In section IV, testing a second order version of delta-sigma ADC is explained. Finally, the work is concluded in section V.

II. Previous Work

Basic Delta-sigma ADC Operation

The basic first order delta-sigma ADC is shown in Figure 1. The heart of this conversion is the modulator. The modulator is a feedback loop that has a quantizer and a low pass filter. The analog input voltage signal is connected to the input of an integrator, producing a voltage slope at the output corresponding to the magnitude of the input. This ramping voltage is then compared with a ground potential by a comparator. The comparator acts as a one-bit ADC, producing a one-bit output depending on whether the integrator output is positive or negative. The comparator output is then latched in a D-type flip-flop. The output of the D-FF is then converted into analog form through the feedback to be subtracted from the input and drive the integrator again.

The output of the D-FF is used to enable a counter that provides a final digital output proportional to the D-FF output pulse width.

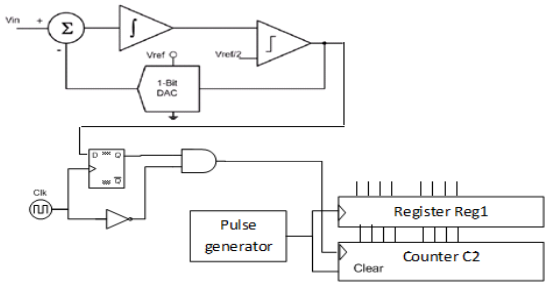

Figure 1: First Order Delta-sigma ADC tested in [6]

In [6], it was shown that all the faults in the analog part of the circuit could be detected with one analog input value,

namely Vcc/2. Applying an input value of Vcc/2 to the Delta-sigma converter under test will produce a digital output of (11000000) for the fault-free case. This value is different from all the faulty outputs considered; hence, all faults are detectable.

Concerning the digital part, all the faulty outputs corresponding to an analog input of Vcc/2 are also different from the fault-free output (11000000) except Q7-stuck-at-1 fault (Q7 being the most significant bit of the counter). Therefore, this fault cannot be detected using the analog input Vcc/2. Another analog test value (–Vcc/2 as an example) had to be applied to detect this fault.

All the results were derived analytically and the entire circuit was simulated using Orcad simulator. The analytical proofs and the simulation results were identical. The fault set consisted of the following catastrophic faults: open (short) resistors and capacitors, stuck-at-Vcc and stuck-at-(–Vcc) for the op-amp and stuck-at-1(0) faults for digital components [7]. Only a single fault was assumed at a time.

So, in [6], a 46-fault set was assumed. One analog input value (Vcc/2) was proven to detect the entire fault set except for one fault. For the 8-bit delta-sigma ADC under test, the coverage was 97.83%. If the number of bits were increased, there would have been only one undetectable fault (the counter's MSB stuck-at-1), which means a higher coverage. If the full coverage is required, an additional analog test input is required.

III. Different Implementation of the First-Order Delta-sigma ADC

In this section, a slightly different implementation of the delta-sigma ADC is investigated and passive component tolerances are studied.

The digital subcircuit is implemented using a synchronous counter [8], shown in Figure 2, instead of the asynchronous counter in [6] to study the effect of this implementation on the minimal test set. The Q output of the flip-flop is used to gate the clock such that the number of output clock pulses depends on the active periods of the Q output. The fault set will be augmented by the faults in the AND gates.

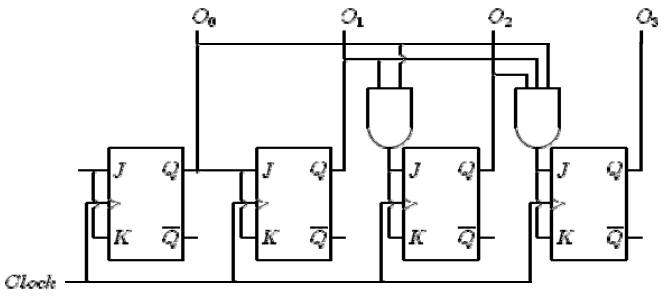

Figure 2: 4-bit Synchronous Counter

Each AND gate has two potential faults: its output stuck-at-0 or stuck-at-1 (see Table I). If the output of the first AND gate (call it AND1) is stuck-at-1, then Q2 will toggle every clock pulse and hence the six most significant bits (Q1 to Q7) will act as a 6-bit counter separate from Q0 and Q1. This will change the correct output of 11000000 which corresponds to 192 clock pulses to be (00000000). As the first two bits Q1Q0 will have the correct value of 00 and the remaining 6-bit counter (Q2 to Q7) will count 192 counts which correspond to (000000). The same case exists if the outputs of AND2, AND3, AND4 or AND5 are stuck-at-1.

If the output of AND1 is stuck-at-0, Q2 will retain its old value with no change. Hence the input to the fourth flip-flop will be '0' keeping Q3 with no change and so on. Assuming initially that all the flip-flops were cleared, then the output will be always 00000000. The same case also exists if the output of AND2, AND3, AND4, or AND5 is stuck-at-0.

If the output of AND6 is stuck-at-1, then Q7 will toggle for 192 counts which means it will be finally a '0', while (Q0 to Q6) will have the correct value of (1000000). This leads to a final faulty output of (01000000).

If the output of AND6 is stuck-at-0, Q7 will retain its old value with no change which is initially a '0'. (Q0 to Q6) will have the correct value of (1000000). This leads to a final faulty output of (01000000).

Table 1: Test results in synchronous implementation

Fault	output
Output of AND1 stuck-at-0	00000000
Output of AND1 stuck-at-1	00000000
Output of AND2 stuck-at-0	00000000
Output of AND2 stuck-at-1	00000000
Output of AND3 stuck-at-0	00000000
Output of AND3 stuck-at-1	00000000
Output of AND4 stuck-at-0	00000000
Output of AND4 stuck-at-1	00000000
Output of AND5 stuck-at-0	00000000
Output of AND5 stuck-at-1	00000000
Output of AND6 stuck-at-0	01000000
Output of AND6 stuck-at-1	01000000

In the analog subcircuit, the effect of component tolerances is investigated next. In an attempt to study the effect of component tolerances on the testing procedure under study in this research, the circuit is investigated with all the passive components' values reduced by 20% from their nominal values. This is part of the well-known vertex analysis [9]. The circuit is then investigated with the components' values increased by 20% from their nominal values. In both cases, it is found that the delta-sigma ADC behaves correctly for the fault-free case and the test set remains the same.

IV. Testing of a Second Order Delta-Sigma ADC

One way of improving the signal to noise ratio (SNR) is to increase the order of the ADC. Usually, it is considered in delta-sigma ADCs that orders higher than two have a stability problem [4]. In this section, a basic design of a second order delta-sigma ADC is studied and tested. It will be shown that the analog input of Vcc/2 is still sufficient to detect all faults of the analog part for the second order delta-sigma ADC shown in Figure 3 [10]. Table II shows possible faults and their erroneous output corresponding to an input of Vcc/2. In

the following paragraphs, the analytical proofs of the faults shown in Table II are described in more details.

If the output of op-amp 1 is stuck-at-Vcc, the output of the first integrator will keep discharging to –Vcc. The output of subtractor (op-amp 3) is: v3=−(v2+v5) and v5=–Vcc assuming that the D-FF is initially reset. Hence, v3 will be –2Vcc which is impossible, so it saturates at –Vcc. The second integrator will also discharge to –Vcc, resulting in a comparator's output of Vcc and Q=1. In the feedback path, v5 will toggle to Vcc making the op-amp 3 output equal to 0V. A zero input to the integrator will not change its output and the D-FF will keep its value '1', resulting in a final digital output of (11111111). The same scenario applies if op-amp2 is stuck-at-(–Vcc).

On the other hand, if op-amp 1 is stuck-at-(–Vcc), the output of op-amp 2 will charge to Vcc. Output op-amp 3 (the subtractor) will be zero which will not change the integrator's output, v4, keeping the initial state of Q=0. The digital output in this case is (00000000). The same scenario applies if op-amp 2 is stuck-at-Vcc.

If the output of op-amp 3 is stuck-at-Vcc, the integrator op-amp 4 will discharge to –Vcc leading to a comparator output of Vcc and Q=1. The final digital output will be (11111111). The same scenario applies if op-amp 4 is stuck-at-(–Vcc) or if op-amp 5 is stuck-at-Vcc.

The opposite of this scenario happens if op-amp 4 is stuck-at-Vcc or if op-amp 5 is stuck-at-0V. In this case, the digital output will be (00000000).

If op-amp 6 is stuck-at-Vcc, the output of the first subtractor (op-amp1) will be (v1=Vcc/2 – Vcc= –Vcc/2). This negative value will make v2 charge to Vcc. This is similar to the case of op-amp 2 output stuck-at-Vcc; hence, the digital output is (00000000).

If op-amp 6 is stuck-at-(–Vcc), the output of the first subtractor (op-amp1) will be (v1=Vcc/2 + Vcc= 3Vcc/2), which is impossible, so v1 will saturate to Vcc. This is also similar to op-amp 1 output stuck-at-Vcc scenario; hence, the digital output is (11111111).

If R1 is short-circuited, op-amp 1 will be a scaled subtractor whose output is: v1= 2Vin–v5, which will initially saturate at Vcc and v3 will discharge to –Vcc. The second subtractor output will be: v3= – (–Vcc–Vcc)= 2Vcc, which is impossible and hence saturates at Vcc. v4 will discharge to –Vcc resulting in a comparator's output of Vcc and Q=1. In the feedback path, v5 will toggle to Vcc making v1 equal to zero. This will not change the integrator output as stated before. The digital output will be (11111111). The same scenario exists if R2 is open-circuited.

If R1 is open-circuited, the first subtractor equation will be v1=–v5 which implies that v1=Vcc initially. v2 will discharge to –Vcc. The second subtractor output will be: v3=−(–Vcc–Vcc)= 2Vcc, which is impossible and hence saturates at Vcc. v4 will discharge to –Vcc resulting in a comparator's output of Vcc and Q=1. In the feedback path, v5 will toggle to Vcc, hence v1 will toggle to –Vcc and the whole situation is reversed leading to Q=0. Q will alternate between 0 and 1 and the final digital output will be half of the full range (i.e., 10000000). The same scenario exists if R2 is short-circuited.

Table II: Test results of the analog subcircuit for a second order delta-sigma ADC

Fault	output
Op-amp 1 stuck at Vcc	11111111
Op-amp 1 stuck-at-(–Vcc)	00000000
Op-amp 2 stuck-at-Vcc	00000000
Op-amp 2 stuck-at-(–Vcc)	11111111
Op-amp 3 stuck-at-Vcc	11111111
Op-amp 3 stuck-at-(–Vcc)	00000000
Op-amp 4 stuck-at-Vcc	00000000
Op-amp 4 stuck-at-(–Vcc)	11111111
Op-amp 5 stuck-at-Vcc	11111111
Op-amp 5 stuck-at-0	00000000
Op-amp 6 stuck-at-Vcc	00000000
Op-amp 6 stuck-at-(–Vcc)	11111111
R1 short circuit	11111111
R1 open circuit	10000000
R2 short circuit	10000000
R2 open circuit	11111111
R3 short circuit	11111111
R3 open circuit	10000000
R4 short circuit	10000000
R4 open circuit	11111111
R5 short circuit	10000000
R5 open circuit	Noise-Dependent
R6 short circuit	00000000
R6 open circuit	10000000
R7 short circuit	10000000
R7 open circuit	10000000
R8 short circuit	10000000
R8 open circuit	10000000
R9 short circuit	10000000
R9 open circuit	Noise-dependent
C1 short circuit	10000000
C1 open circuit	10000000
C2 short circuit	00000000
C2 open circuit	10000000

If R3 is short-circuited, op-amp1 will behave like a buffer, v1=Vcc/4. The first integrator will charge to –Vcc. This case is similar to op-amp 2 is stuck at –Vcc and the final output is (11111111). The same scenario applies if R4 is open-circuited.

If R5 is short-circuited or C1 is open-circuited, op-amp 2 will behave like a comparator. Similarly, if R9 is short-circuited or C2 is open-circuited op-amp4 will behaves like a comparator. In both cases, the final output will be (10000000).

If R5 is open-circuited, op-amp2 will be a comparator with a floating inverting input. The noise on this floating point will force v2 to be Vcc or –Vcc. In both cases the output will be noise-dependent and the possibility of the system output being equal to the error-free case is very low; hence, it is considered to be a detectable fault. The same scenario happens with op-amp4 if R9 is open-circuited.

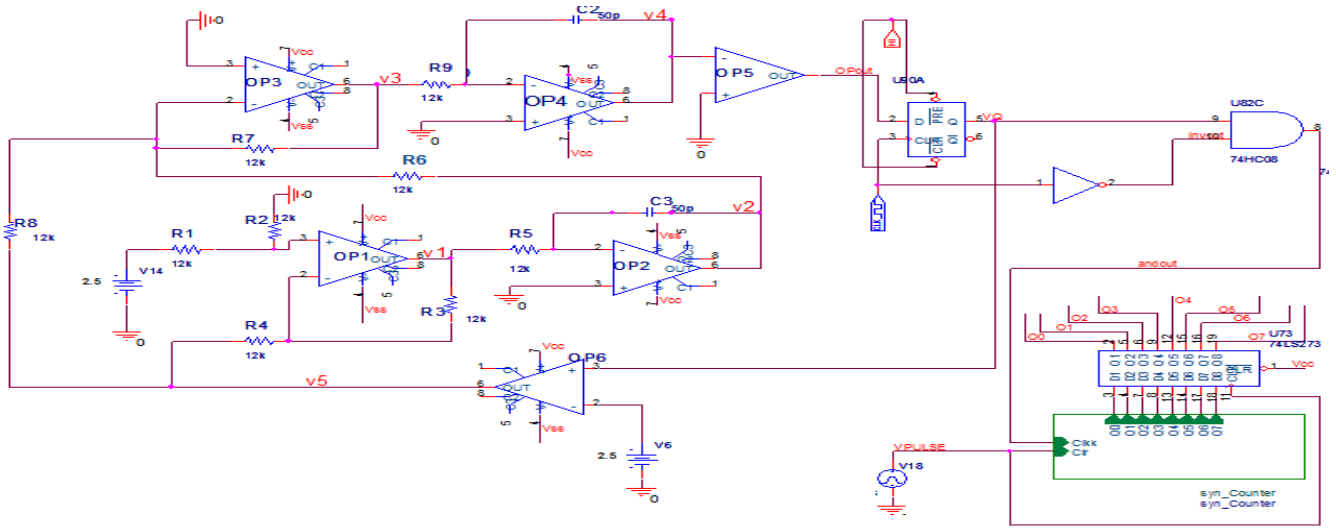

Figure 3: A second order delta-sigma ADC

If R6 is short-circuited, op-amp 3 will be a buffer with a zero output. The input of the integrator is zero, which will not change its output; the digital output is (00000000).

If R6 is open-circuited, op-amp 3 will act as a comparator with an initial output of Vcc, results in Q=1. In the feedback path, v5 will toggle and op-amp3 becomes –Vcc resulting in Q=0 and so on. The digital output is (10000000). The same scenario exists if R8 or R7 is short-circuited.

If R7 is open-circuited the second subtractor's equation will be v3=–v5. Initially, v3 is Vcc; this produces Q=1 which will toggle v5 and v3 will be –Vcc producing Q=0 and so on. The digital output is (10000000).

If R8 is open-circuited, the second subtractor's equation will be v3=–v2. A scenario similar to the previous one exists and the digital output is (1000000).

If C1 is short-circuited, op-amp 2 acts as a buffer and v2=0. v3=−v5 which will be Vcc initially, leading to Q=1, v5 will then toggle to Vcc and v3 becomes −Vcc and the whole case is reversed and Q=0 and so on. The digital output will be (10000000).

If C2 is short circuited, op-amp 4 acts as a buffer and v4=0. The comparator op-amp5 has both inputs grounded. Ideally, when both inputs of the comparator are equal, the output will be zero and the final digital output is (00000000). However, considering practical comparators, the output will be noise-dependent and the possibility of the system output being equal to the error-free case is very low.

As the digital subcircuit of the Delta-Sigma ADC for the first order and the second order are the same, all faults will be detected by Vcc/2 and –Vcc/2.

All the results are verified by simulations. The simulation results and the analytical analysis are identical.

Finally, the issue of passive component tolerances is studied. Fault-free circuits are analyzed with all passive component nominal values increased by 20% then decreased by 20%; in both cases, the fault-free circuit operates correctly and the two test values detect all faults.

V. Conclusions and Future Work

In this paper, it is proven, for one fault at a time, that two test values can detect all catastrophic faults in a first-order delta-sigma ADC with a synchronous counter used in the digital subcircuit. These two values are Vcc/2 and –Vcc/2. Moreover, if the passive components are all 20% over (or under) their nominal values, the circuit will operate correctly in the fault-free case and all faults will be detected by Vcc/2 and –Vcc/2.

Next, a second-order delta-sigma ADC is investigated. The same catastrophic fault set is assumed and again, one fault at a time. It is found that the same test set (Vcc/2 and –Vcc/2) detects all faults in the assumed fault set. Also, passive component tolerances of 20% are investigated; it is observed that if all components are above (below) their nominal values by 20%, the circuit behaves correctly in the fault-free case and the two test values detect all faults.

The same procedure presented in this paper is currently being investigated for switched-capacitor delta-sigma ADC implementations.

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