Comp Eng 4DM4 - Computer Architecture

September – December, 2013

Lectures:	Mon, Thur.,	12:30-1:20,	JHE/A102
	Tues,	1:30-2:20,	JHE/A102
Tutorials :	Wed.,	9:30-10:20,	ETB 224
Labs:	Thurs, Fri.,	2:30-5:20,	ITB 157. EOW

Prof's Office Hours: TBA.

Instructor:
Professor Ted Szymanski
Department of Electrical and Computer Engineering
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(All emails to the Prof should begin with 4DM4 in the subject to be recognized by spam filtering programs)

Teaching Assistants :
Maryam Rezaei: <rezaeem at mcmaster dot ca>

Course Web Site:
http://mail.ece.mcmaster.ca/faculty/teds/COURSES

Course Objective: The 4DM4 course covers advanced topics in the field of computer architecture, including: multicore processors (i.e., the Intel and ARM processors), static and dynamic scheduling, vector machines including the Graphics Processing Units (GPUs), Networks-on-Chips, and cloud-based data-centers. Our laboratories will focus on the development of Networks-on-Chips (NOCs) in the VHDL hardware description language, using the Altera Quartus CAD tool. You should be well prepared for a career in which you will likely encounter microprocessors, HDL cores and warehouse-scale cloud data-centers on a regular basis. You will also have a solid basis for a continuation of your studies in graduate school.

Audience: Computer Architecture 4DM4 is an advanced level course suitable for students with previous exposure to computer architecture and digital systems. We use the latest advanced textbook written by John Hennessy (the president of Stanford University) and David Patterson:

TextBook: "*Computer Architecture: A Quantitative Approach*", Fifth Edition, John Hennessy and David Patterson, Elsevier Publishers (Morgan-Kaufmann), 2012, ISBN 978-0-12-383872-8 (paperback)

The same authors have an entry-level textbook called "*Computer Organization and Design - The Hardware/Software Interface*", which is a good introduction to the field.

The textbooks by Patterson and Hennessey are considered to be among the most comprehensive books on computer architecture available today. My 4DM4 notes will be made available electronically on the web. The tentative course outline follows:

Outline of Topics: (weight)

1.	Fundamentals of VHDL (VHDL constructs, Moore's Law)	1 week
2.	Cloud Computing and Multiprocessors A Network-on-Chip (NOC) Lab. in VHDL (behavioural and structural VHDL)	 1 week
Ch. 3.	Instruction Level Parallelism Static scheduling, loop unrolling, dynamic scheduling, steady-state multiple issue, many examples multithreading, the Intel iCore 7 and ARM Cortex)	7-8 weeks total 2-3 weeks 3 weeks 2 weeks

The last few weeks are reserved for student presentations on these topics (students work in groups of 2, with 2 or 3 presentations per class.)

Ch. 4	Vector, SIMD and GPU Architectures SIMD instructions for multimedia, Loop-level parallelism	1 week
Ch. 7	Thread Level Parallelism (student presentations)	1 week
Ch. 6	Cloud Data-Centers and Cloud Computing (student presentations)	1 week

Tentative Marking Scheme:

Assignments (approx. 3)	approx. 12 %
Laboratories (approx. 3)	approx. 12 %
Class presentation	approx. 6 %
1 Scheduled Midterm Test	approx. 20 %
1 Final Exam	approx. 50 %

Weights may be shifted by +/- 10 % to reflect the work involved in each component, at the instructor's discretion. To achieve an A+ in this course, a student must achieve an A+ in the exam. To pass this course, a student must pass the final exam. (The prof. may allocate a few percentage points (ie up to 2 or 3%) for selected students who contribute a lot to class discussions.)

Class Participation/Pop Quizzes: Students who add to the class experience may get marks for participation, at the instructor's discretion. The "pop" quizzes may reflect attendance, and may be given at the instructor's discretion. These marks are firm.

Laboratories: The laboratories will involve the design of Network-on-Chip (NOC) in the VHDL hardware description language. All students should have had some previous exposure to VHDL or Verilog in the courses COE-2DI4 Logic Design or COE-3DQ5 Digital Systems Design. Some training videos will be supplied, to get you started.

Feedback to the Instructor: We want to make this course as exciting as possible for you. The lectures and labs will be revised in 2013 and we will try to present a lot of examples in class. If you have feedback for the prof, please drop by during office hours or right after the class and let us know.

Other Resources:

VHDL: You can obtain a student edition of the Altera Quartus CAD software at this web-site:
http://www.altera.com/support/licensing/lic-university.html
(Get the Quartus II Web-version; see the upper left hand side menu)

"Getting Started" Manual for Altera's Quartus CAD system is available at:
http://www.altera.com/support/software

Altera Application Notes: Available at
http://www.altera.com/literature/lit-an.html

Calculator requirement for tests and examinations: *the McMaster Standard Calculator (Casio fx991)*

Policy Reminders: *(include the following on all course outlines)*

Senate and the Faculty of Engineering require all course outlines to include the following reminders:

"The Faculty of Engineering is concerned with ensuring an environment that is free of all adverse discrimination. If there is a problem, that cannot be resolved by discussion among the persons concerned, individuals are reminded that they should contact the Department Chair, the Sexual Harassment Officer or the Human Rights Consultant, as soon as possible."

"Students are reminded that they should read and comply with the Statement on Academic Ethics and the Senate Resolutions on Academic Dishonesty as found in the Senate Policy Statements distributed at registration and available in the Senate Office."

"Academic dishonesty consists of misrepresentation by deception or by other fraudulent means and can result in serious consequences, e.g. the grade of zero on an assignment, loss of credit with a notation on the transcript (notation reads: "Grade of F assigned for academic dishonesty"), and/or suspension or expulsion from the university. It is your responsibility to understand what constitutes academic dishonesty. For information on the various kinds of academic dishonesty please refer to the Academic Integrity Policy, specifically Appendix 3, located at
http://www.mcmaster.ca/senate/academic/ac_integrity.htm

The following illustrates only three forms of academic dishonesty:

1. **Plagiarism, e.g. the submission of work that is not one's own or for which other credit has been obtained. (***Insert specific course information, e.g. style guide***)**
2. **Improper collaboration in group work. (***Insert specific course information***)**
3. **Copying or using unauthorized aids in tests and examinations.**

(*If applicable***) In this course we will be using a software package designed to reveal plagiarism. Students will be required to submit their work electronically and in hard copy so that it can be checked for academic dishonesty."**