Welcome to
4DM4 - Computer Architecture
Sept. 5- Dec. 5, 2013

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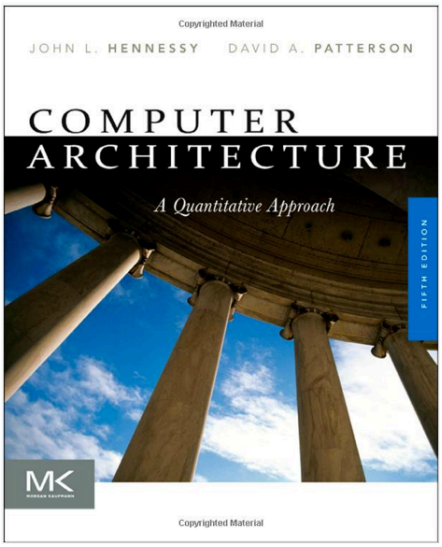
New Textbook - 5th Edition



- Why this book ? (1) Most recent book (2011/2012) by leaders of the field
- IT COVERS: (2) existing Intel Pentium and Itanium architectures, (3) the newest Vector, SIMD, GPU architectures, (4) multi-core processors with multiple threads, (5) Cloud computing systems

New Textbook - 5th Edition

- Book is available at McMaster textbook store

- Book also is available from Elsevier e-store (see next slide)

Your professor has selected a book from Elsevier as required or suggested reading for this course. From Aug. 15 to Oct. 15, we would like to offer you up to 40% discount on the materials when purchased from our online store. **Ebooks are eligible for a 40% discount, while print books are eligible for a 25% discount + free shipping.** Follow these easy steps to get the materials you need and claim your discount.

1. **Your Elsevier textbooks for this course include:**
Computer Architecture 5th edition by Hennessy (ISBN: 9780123838728)

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4DM4 Topics

- Week 1,2: Welcome, History of Computing (BBC video – Codebreakers-The Forgotten Heros), Moore's Law slides, Cloud Computing slides
- Week 1,2: Review of VHDL, FPGAs, Networks-on-Chip in VHDL

- Ch. 3. Instruction Level Parallelism (8 weeks) -
- Basic Pipelining; loop unrolling, static scheduling, (may include hazards, stalls, forwarding, branch delays, branch prediction, exceptions)
- Advanced Pipelining: dynamic scheduling, multiple issue, multithreading, the Intel iCore 7 and ARM Cortex-A8

- Class Presentations:
- Ch. 4. Data-Level Parallelism – Vector, SIMD and GPU Machines
- Ch. 5. Multi-Threading and Multi-Core machines
- Ch. 6. Warehouse Scale computing – Cloud computing

4DM4 Laboratories – NoC Design

- Design of a Network-on-a-Chip (NoC) using VHDL
- The latest Graphics Processor Units (GPUs) typically have 512 processors on one chip, interconnected with a Network-on-Chip (NoC)
- We will design a simple NoC in VHDL on an Altera FPGA, for the labs
- Class will use VHDL language for functional specifications. Labs use the ALTERA QUARTUS VHDL Compilers for FPGA synthesis.
- Please download the student edition of QUARTUS for Windows OS:
- http://www.altera.com/support/licensing/lic-university.html
- Manual at:
- http://www.altera.com/support/software/sof-maxplus2.html
- Altera Application Notes: Available at
- http://www.altera.com/literature/lit-an.html

4DM4 Laboratories – The NOC

- Design of a pipelined NOC router/switch using VHDL
- Interconnect the routers/switches into a Network Topology
- Router may use 100,000 - 200,000 logic gates, and should be compiled and downloadable onto an Altera FPGA and clock at 100 … 500 MHZ
- Will use VHDL language for functional specifications. Labs use the ALTERA QUARTUS VHDL Compilers for FPGA synthesis.

- Work in groups on 2 for labs and assignments

4DM4 Laboratory Access

- Labs will be in room ITB 157, according to registrar's sections
- LAB ACCESS: you will be able to access the lab after hours (7 AM - 9 PM) using an electronic pass card - details to be provided in class

- Our 4DM4 TA Maryam Rezaee is a graduate student working with the prof. She is an expert in VHDL, FPGAs and System-on-Chip (SoC) design.
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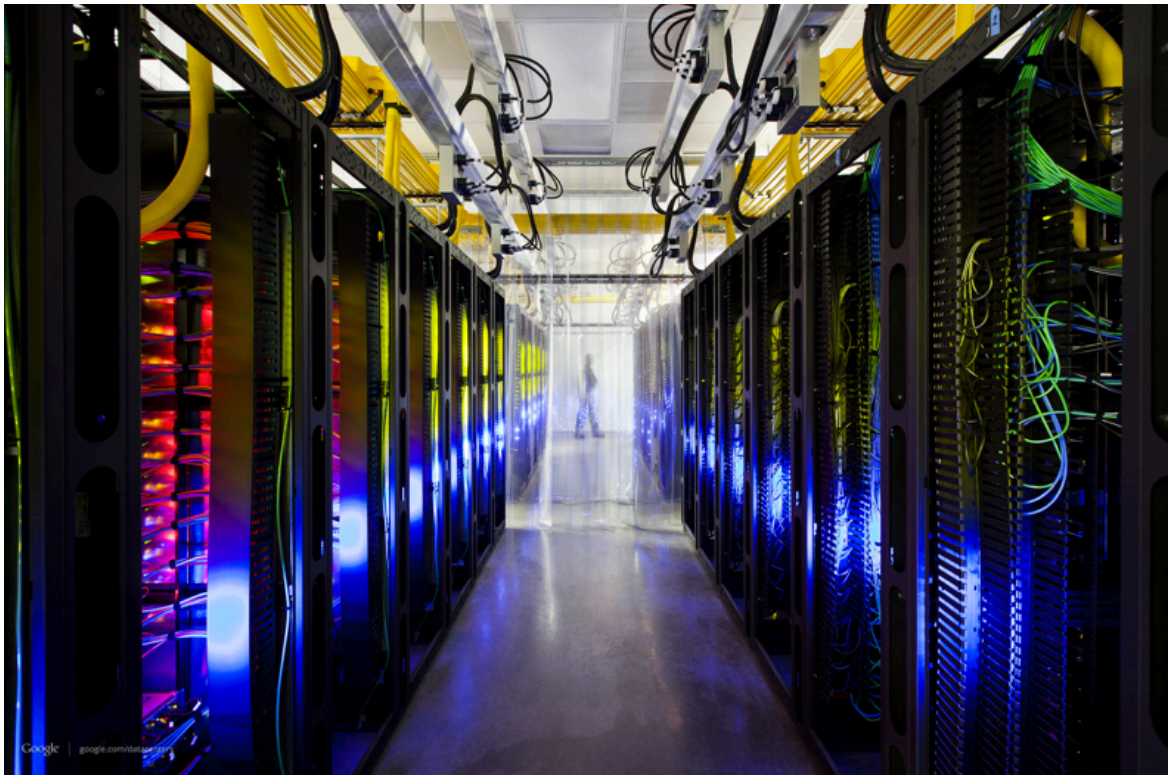
Marking Scheme

- Assignments (approx. 3) approx. 12 %
- Laboratories (approx. 3) approx. 12 %
- Class Presentation approx. 6 %
- 1 Scheduled Midterm Test approx. 20 %
- 1 Final Exam approx. 50 %
- Grades may change by +/- 10%, depending upon difficulty (at instructor's discretion)
- A few marks may be awarded to selected students for contributions to class participation/discussions (up to 2-3 %)

Class Presentations

- Depending upon class size, can be done individually or in small groups (say 2 students)
- Select a topic from the class text, create a 15 minute presentation (say 15 slides, summarizing the most important points)
- You may consult with prof to help plan your presentation
- You may use figures from textbook (see next 2 slides)
- Augment textbook material with other recent material that you find on the web (the textbook material is typically 1-2 years old, and there may be new advances in the field)
- These presentations are a good way to find out the latest in the field
- Presentations will focus on multicore processors, GPUs, the Cloud, Cloud data-centers, Networks-on-Chip (NoCs), Exascale Computers, the Cray Titan, the Tianhe-2, etc

Pictures: A Google DataCenter



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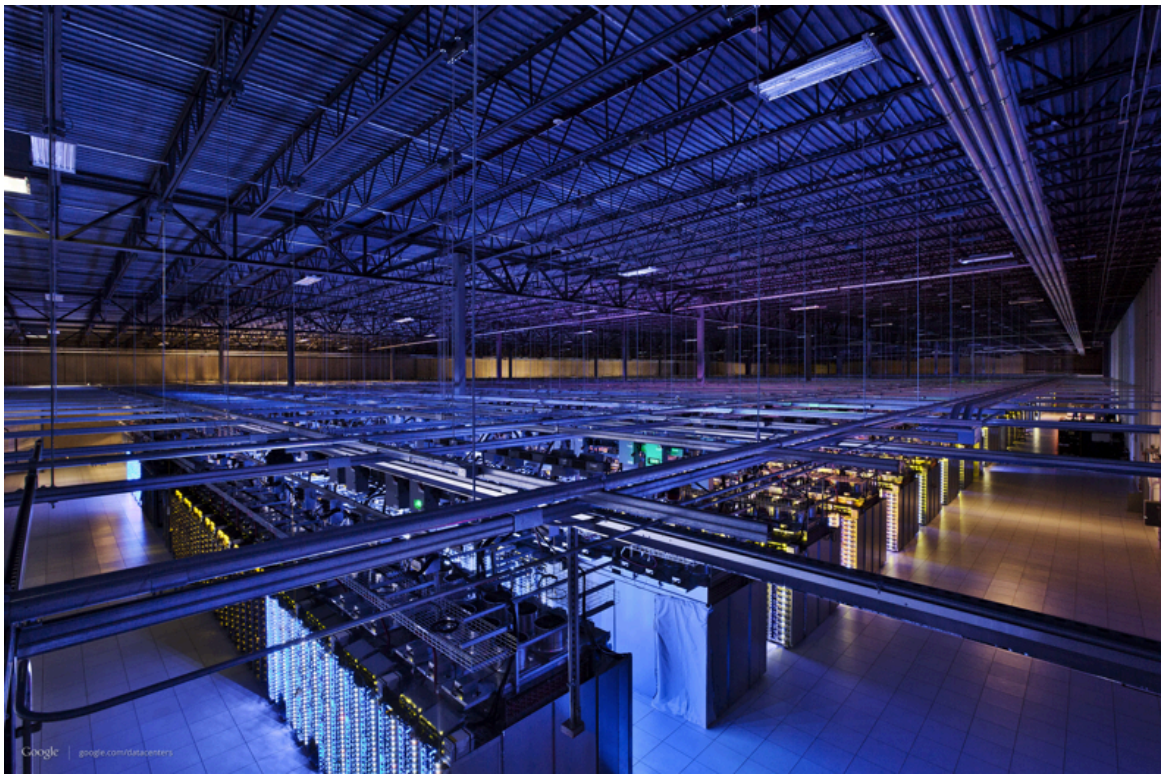


Google Data-Center Shipping Container

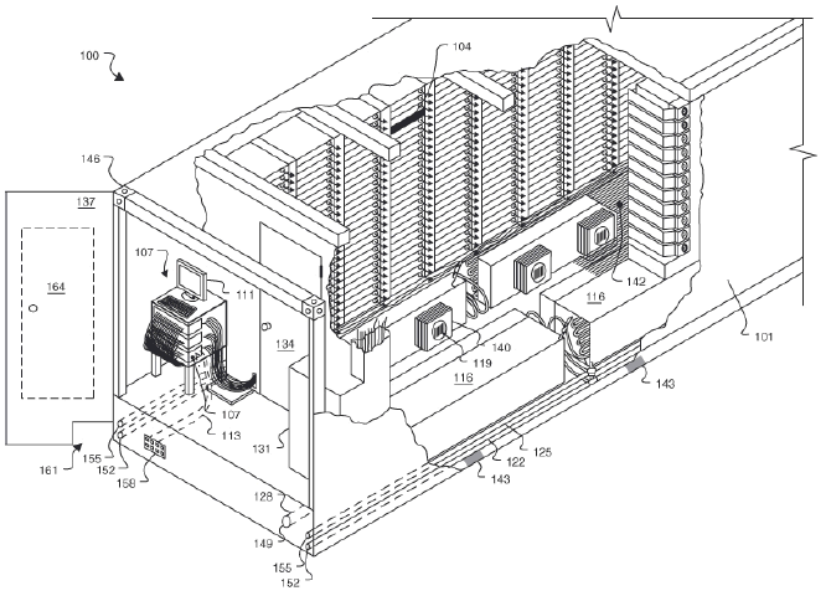
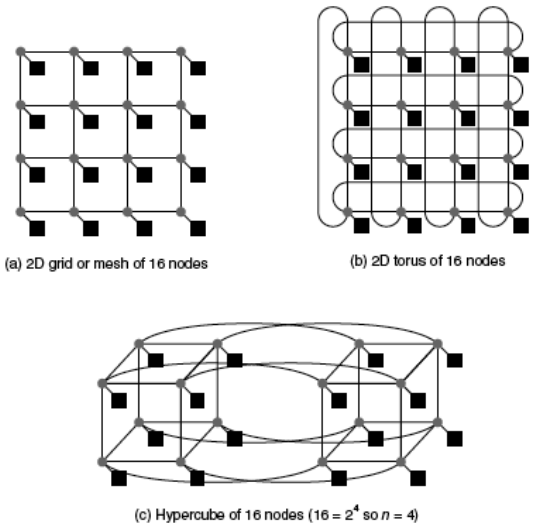


Figure 6.19 Google customizes a standard 1AAA container: 40 x 8 x 9.5 feet (12.2 x 2.4 x 2.9 meters). The servers are stack

Cray Titan Supercomputer (20 PetaFlops)

Tianhe-2 Supercomputer (33 PetaFlops)

Networks for Data-Centers & NoCs



(a) 2D grid or mesh of 16 nodes

(b) 2D torus of 16 nodes

(c) Hypercube of 16 nodes ($16 = 2^4$ so $n = 4$)

Figure F.14 Direct network topologies that have appeared in commercial systems, mostly supercomputers. The shaded circles represent switches, and the black squares represent end node devices. Switches have many bidirectional network links, but at

Questions ?