Field-programmable smart-pixel arrays: design, VLSI implementation, and applications

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A smart-pixel array is a two-dimensional array of optoelectronic devices that combine optical inputs and outputs with electronic processing circuitry. A field-programmable smart-pixel array (FP-SPA) is a smart-pixel array capable of having its electronic functionality dynamically programmed in the field. Such devices could be used in a diverse range of applications, including optical switching, optical digital signal processing, and optical image processing. We describe the design, VLSI implementation, and applications of a first-generation FP-SPA implemented with the 0.8-μm complementary metal-oxide semiconductor–self-electro-optic effect device technology made available through the Lucent Technologies–Advanced Research Projects Agency Cooperative (Lucent/ARPA/COOP) program. We report SPICE simulations and experimental results of two sample applications: In the first application, we configure this FP-SPA as an array of free-space optical binary switches that can be used in optical multistage networks. In the second, we configure the device as an optoelectronic transceiver for a dynamically reconfigurable free-space intelligent optical backplane called the hyperplane. We also describe the testing setup and the electrical and the optical tests that demonstrate the correct functionality of the fabricated device. Such devices have the potential to reduce significantly the need for custom design and fabrication of application-specific optoelectronic devices in the same manner that field-programmable gate arrays have largely eliminated the need for custom design and fabrication of application-specific gate arrays, except in the most demanding applications.

OCIS codes: 200.2610, 200.3050, 250.0250, 250.3140.

1. Introduction

For taking advantage of the high space–bandwidth product of optics, free-space digital optical technologies that consist of optically interconnected two-dimensional arrays of smart pixels have emerged as an attractive interconnection platform.[1] A smart pixel is an optoelectronic device that combines optical inputs, outputs, or both with electronic processing circuitry and can be integrated into two-dimensional arrays. A field-programmable smart pixel is a smart pixel capable of having its electronic circuitry dynamically programmed in the field.[2–4] Because of their functional versatility, field-programmable smart-pixel arrays (FP-SPA's) can implement a wide range of optical interconnection architectures and functions, which is not possible with custom-designed application-specific smart-pixel arrays.

The flexibility of FP-SPA's, as with most other programmable devices, has some economic advantages. FP-SPA's can eliminate the need for the custom digital and VLSI design of an application-specific optoelectronic smart-pixel array, which is costly. FP-SPA's can also eliminate months of turnaround time associated with the fabrication of such a device. Currently, the design of a custom optoelectronic device can require six months, and the fabrication can require a year and cost of the order of $10,000 (depending on the die size). In contrast, the functionality of a FP-SPA device can be programmed dynamically in the field in a matter of minutes, typically by the downloading of a control bit pattern into the device. FP-SPA's can also be batch fabricated, leading to a significant cost reduction. In addition, they can also be made compatible with standardized

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I/O pitches, packaging assemblies, and optomechanical support structures.[2,3] Field-programmable smart pixels that integrate optical I/O onto complementary metal-oxide semiconductor (CMOS) substrates were proposed in 1994 (Ref. 2) and have since generally been accepted as both feasible and practical. However, to date no integrated field-programmable optoelectronic device has yet been demonstrated. This paper addresses issues in the design, fabrication, and testing of the first, to our knowledge, integrated field-programmable optoelectronic device yet demonstrated.

More recently, integrated optoelectronic devices containing some programmable functions were considered in Ref. 5–7. An alternative to the integrated optoelectronic devices considered in this paper is to use conventional electronic Xilinx integrated circuits interconnected with LED's, which was considered in Ref. 8. However, this approach does not overcome the electronic bandwidth bottleneck of conventional electronic field-programmable gate arrays (FPGA's). Merging optical I/O directly onto the CMOS substrate permits the potential to exist to create programmable devices that can process vast amounts of optical data.

In this paper we describe the design, VLSI implementation, and free-space optical interconnect applications of a first-generation 4 × 3 FP-SPA,[4] implemented in the CMOS–self-electro-optic effect device (–SEED) optoelectronic technology made available through the 1995–1996 Lucent Technologies–Advanced Research Projects Agency Cooperative (Lucent/ARPA/COOP) workshop.[9] We report SPICE simulation results in which we configure this FP-SPA in two sample applications: first as an array of free-space optical binary switches that can be used in an optical multistage network such as a Benes or a Clos network, and second as an optoelectronic transceiver for a dynamically reconfigurable free-space optical backplane architecture called the hyperplane.[10] We also describe the testing setup and the results of electrical and optical tests that demonstrate the correct functionality of the fabricated FP-SPA device.

2. Field-Programmable Smart-Pixel Array Design

The 1995 Lucent/ARPA/COOP workshop required that all designs be submitted as a 2 mm × 2 mm die of 0.8-μm CMOS. By use of the existing Tanner Research standard cell library[11] for electronic I/O pads and Lucent Technologies' standard cells for optical I/O, the CMOS substrate supported approximately 200 optical diodes and 40 electronic I/O pins. Hence our first-generation device was designed to fit within these parameters. In this collaborative project the digital and the VLSI design and implementation were performed at the Microelectronics and Computer Systems Laboratory at McGill University, Montreal, while the optoelectronic testing was done at the University of Colorado at Boulder, Colorado.

The first-generation FP-SPA was designed to demonstrate a proof of concept, demonstrating that programmable optoelectronic devices with of the order of 1000 transistors per optical I/O are feasible. The first-generation FP-SPA device consisted of a 4 × 3 array of programmable smart pixels and a control RAM for storing the control bits that determine the functionality of the device. With reference to Fig. 1, every smart pixel has 15 electrical I/O. Each pixel has two 1-bit electrical connections to each of its four neighbors in the north, east, south, and west (N, E, S, and W, respectively) directions. For example, each pixel has two connections, called N.in and N.out, with its northern neighbor as shown in Fig. 1. Each pixel in a row receives a horizontal-broadcast signal, denoted H.B, which is supplied to the device from the external world. Each pixel in a column also receives a vertical-broadcast signal, denoted V.B, which similarly is supplied to the device from the external world. The logical functions of the rows and the columns can be modified by external adjustment of the H.B or the V.B signals, which are then distributed to those rows and columns, respectively. Finally, each pixel also receives three global control signals, called the FF1-Clock, the FF2-Clock, and the Reset.

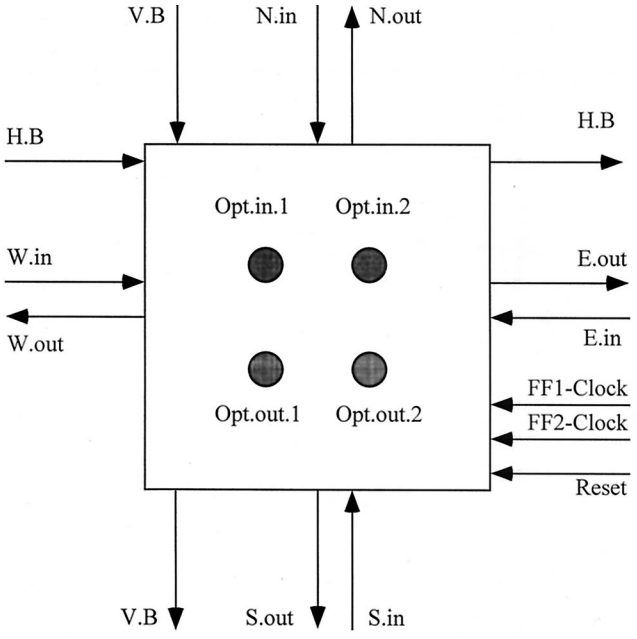

Fig. 1. I/O ports of a single programmable pixel.

Each pixel also has two optical input bits, denoted Opt.in.1 and Opt.in.2, and two optical output bits, denoted Opt.out.1 and Opt.out.2. We form a large two-dimensional array of pixels on the FP-SPA by abutting neighboring pixels on the CMOS substrate and connecting their electrical I/O appropriately.

A. Field-Programmable Smart-Pixel Array Internal Structure

Each field-programmable smart pixel is actually a finite-state machine with electronic I/O, optical I/O, and internal state information stored in *D* flip flops (FF's), as shown in Fig. 2.

FP-SPA programmability is achieved by use of pro-

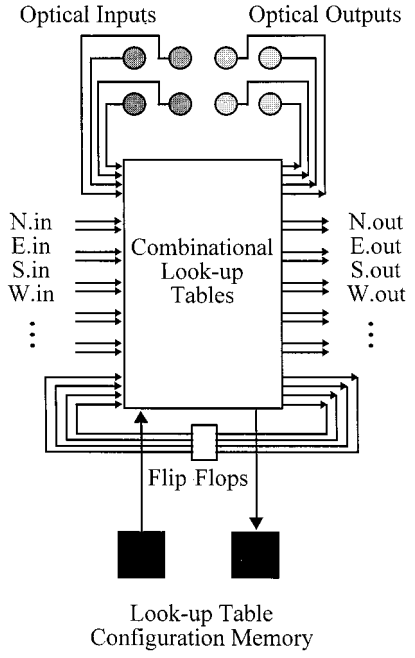

Fig. 2. Finite-state machine representation of the FP-SPA.

grammable truth tables, as shown in Figs. 2 and 3. Each programmable truth table is essentially a combinational lookup table (LUT) that computes a single logical output bit given three logical input bits. By use of conventional FPGA terminology, our programmability is achieved with several three-input LUT's in each smart pixel. Each three-input LUT is implemented with an eight-to-one multiplexer (MUX) that has three select lines, eight input lines and one output line. Each MUX can realize an arbitrary combinational logic function of the three logic values appearing on its three select lines. Each distinct combination of the three logic values represents one row of a truth table, and the logical output bit associated with each row of the truth table is made available to the MUX inputs. Hence the function of the three logical variables is determined by the 8 bits appearing on the MUX's input lines, where each input corresponds to one row of a truth table.

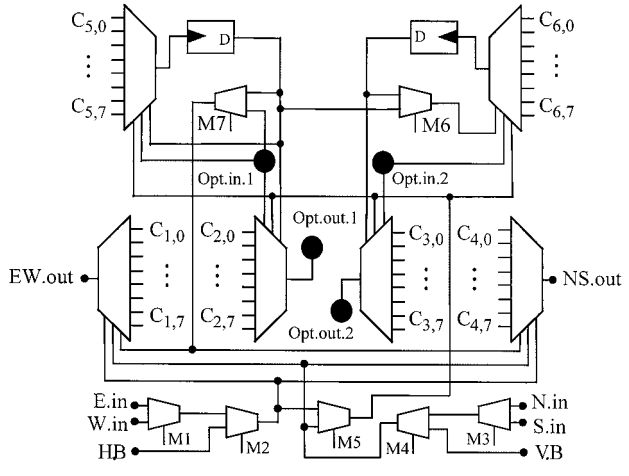

Fig. 3. Schematic of a single programmable pixel. $C_{i,j}$ denotes the jth control bit for the ith LUT or the eight-to-one MUX. M_i denotes the control bit for the ith two-to-one MUX. Each pixel has 55 control bits.

As shown in Figs. 2 and 3, each field-programmable smart pixel can be represented as an arbitrary finite-state machine with two *D* FF's, several three-input LUT's, and several binary MUX's for routing control signals to the LUT's. In each pixel the logical values on the four electrical output ports going to the four nearest neighbors, N.out, E.out, S.out, and W.out, are determined by LUT's. In our first-generation design a single LUT computes a logical value called NS.out, which appears on the N.out and the S.out ports of the pixel, i.e., the N.out and the S.out ports share a single LUT to conserve hardware. Another LUT computes a logical value called EW.out, which appears on the E.Out and the W.out ports of the pixel.

The logical values appearing on each of the optical outputs, Opt.out.1 and Opt.out.2, are determined by separate three-input LUT's. Each pixel also has 2 bits of memory, FF-1 and FF-2, for the finite-state machine. The logical values stored in each FF are determined by separate three-input LUT's.

Several binary MUX's (M1–M7 in Fig. 3) are used to route certain signals to the select lines of the LUT's. Hence the three logic variables in each programmable LUT can be determined to a certain extent by the user by the programming of the binary MUX's M1–M7.

B. Field-Programmable Smart-Pixel Array Programming

In the first-generation FP-SPA 55 bits are needed to program the functionality of each pixel. With reference to Fig. 3, there are 8 bits per LUT times 6 LUT's and 7 bits for the binary MUX's (M1–M7) select lines. All the pixels in the odd-numbered columns (1 and 3) are programmed with the same control RAM bits, and programming is similar for the even-numbered columns (2 and 4). Therefore a total of 110 bits are required to program the entire device. Pairs of adjacent pixels can be programmed to realize a larger finite-state machine than an individual pixel is capable of.

The control RAM is implemented by 110 *D* FF's, which are connected to form an internal 110-bit shift register. Similar to programming static-RAM-based FPGA's, when programming the FP-SPA a set of 110 control bits are serially shifted into the control RAM. A programming clock must also be applied externally to activate the *D* FF's. Dynamic reconfiguration of FP-SPA functionality is possible by means of loading a new set of control bits. If we assume a 2-MHz clock rate, a complete reconfiguration requires approximately 50 μs.

To test the device, we mounted the FP-SPA chip on a prototypical printed circuit board with an Altera FLEX Model 81500 FPGA. Programming is accomplished under computer control through the parallel port of a PC workstation. The Altera FPGA supplies a programming-clock signal and a serial data path to

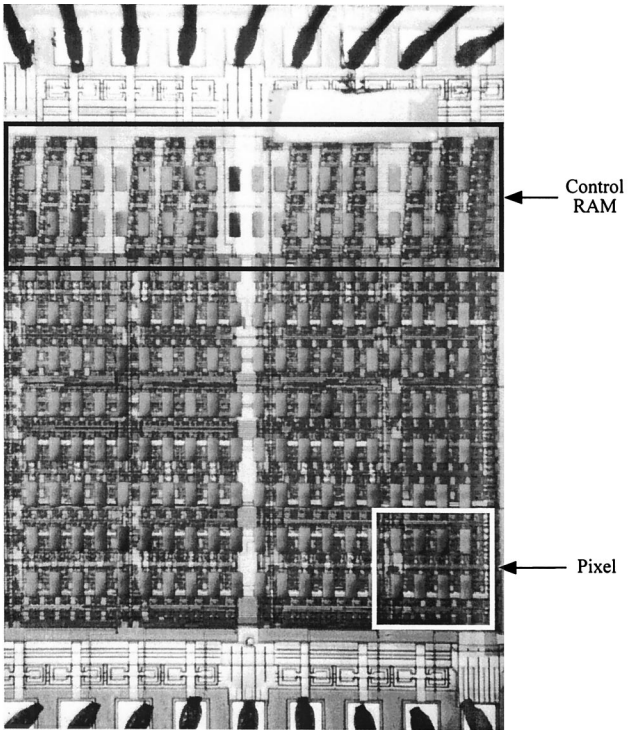

Fig. 4. Photograph of the FP-SPA VLSI die. The control RAM is at the top of the integrated circuit. The 4 × 3 array of pixels is underneath the control RAM.

the field-programmable smart pixel to load the control RAM. It also provides several serial datapaths to the N, E, S, and W data inputs of the device and to the V.B and the H.B signals of the device.

Software supervises the transfer of data between the PC and the FPGA with parity checking. In one upload or download transaction 128 bits can be transferred. The data stream is divided into 16 blocks of 8 bits. In each block, 7 bits are used for control RAM data, and 1 bit is reserved for even parity. Hence the effective data-carrying capacity of each transaction is 16 × 7 = 112 bits, which allows the entire control RAM contents to be transferred from the PC to the FPGA and then to the FP-SPA in a single transaction.

This simple and versatile programming setup can easily be adapted for future generations of FP-SPA's with larger control RAM capacities. We successfully achieved a programming speed of 2 MHz. The Altera FPGA utilizes 1160 of 1296 logic cells (89% utilization) to implement the logic needed to program the FP-SPA. The logic is easily extended to program devices with much larger control RAM's.

3. Field-Programmable Smart-Pixel Array VLSI Implementation

The FP-SPA design is implemented by use of Lucent Technologies' CMOS–SEED optoelectronic VLSI technology. A single pixel is implemented with approximately 670 transistors. The dimension of the silicon die, shown in Fig. 4, is 2 mm × 2 mm. It has a total number of approximately 10,000 transistors,

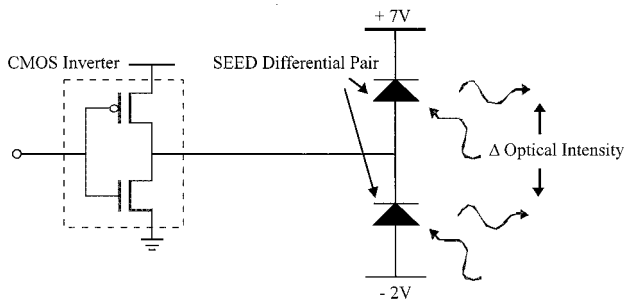

Fig. 5. Differential optical signaling scheme.

which is equivalent to a density of approximately 250,000 transistors/cm^2.

A. Complementary Metal-Oxide Semiconductor–Self-Electro-Optic Effect Device Technology

The CMOS–SEED technology combines silicon CMOS circuitry with GaAs multiple-quantum-well SEED's by means of flip-chip bonding. The CMOS circuitry contains a small (~15-μm) bonding pad at each location at which an electrical contact to a SEED is needed for optical detection and modulation. A substrate containing an array of SEED's (with contacts positioned according to the CMOS contacts) is flip-chip bonded to the CMOS substrate. A final step removes the SEED substrate and leaves behind an array of isolated SEED's, each electrically attached to the CMOS circuitry. This technology can currently integrate dense silicon CMOS (0.8-μm CMOS) with dense GaAs optoelectronics (28,000 SEED's/cm^2) and operate at rates greater than 500 Mbits/s.[9]

B. Optical Windows Implementation

The FP-SPA's optical input and output windows are implemented by use of SEED's. These SEED's are used as high-efficiency optical detectors or optical modulators. In operation optical power from an off-chip laser is modulated by the SEED's that are connected to the smart-pixel transmitters. This modulated optical power is then detected by the SEED's that are connected to the smart-pixel receivers. To improve the FP-SPA's optical detection capability, we increase its optical signals' contrast ratio by using differential optical signaling. In this signaling scheme, shown in Fig. 5, the logic value at an optical window is determined by the difference in optical intensity at a differential SEED pair. To implement four optical windows per pixel requires 8 SEED's/pixel; thus our device has a density of 7300 SEED's/cm^2.

4. Field-Programmable Applications

We demonstrate the programmability of the described FP-SPA by configuring it in two sample applications. In the first application the FP-SPA is programmed to implement an array of free-space optical binary switches, which can be used in an optical

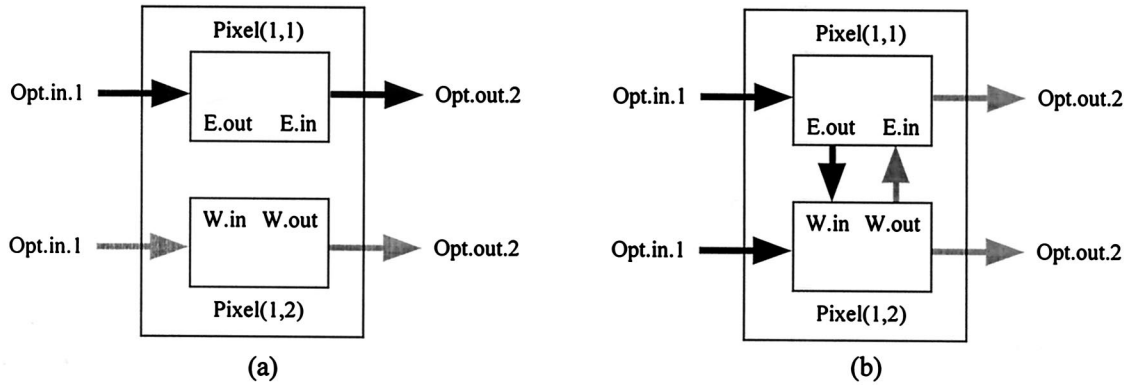

Fig. 6. (a) Bar state of a two-input, two-output binary switch. (b) Cross state of a two-input, two-output binary switch.

multistage network such as a Benes or a Clos network. In the second application the FP-SPA is programmed to implement an optoelectronic transceiver for a reconfigurable intelligent optical backplane called the hyperplane. We report SPICE simulation results for these two configurations.

A. Array of Optical Binary Switches

SPICE simulation results of using two adjacent field-programmable smart pixels as a free-space optical binary switch are reported. An optical binary switch has two optical inputs, two optical outputs, and two states, as shown in Fig. 6. In the *bar* state each optical input is routed straight through to its associated optical output. In the *cross* state the data appearing at the optical inputs are exchanged and then appear in the optical outputs.

In this application two neighboring pixels together implement a binary switch, as shown in Fig. 6. In the bar state each pixel simply propagates the data appearing on the optical input Opt.In.1 to its optical output Opt.out.2. In the cross state each pixel propagates the data appearing on the optical input Opt.In.1 to its neighboring pixel. It also simultaneously accepts the data from its neighbor and propagates it to its optical output Opt.out.2.

SPICE simulations are shown in Figs. 7 and 8. In Fig. 7 the optical input Opt.in.1 of one pixel is directed to the optical output Opt.out.2 of the same pixel. Two adjacent pixels thus implement the bar state, as shown in Fig. 6. From Fig. 7 we can see that there is a 7-ns latency between the time the optical data is received on Opt.in.1 (bold curve) and the time it appears on the optical output Opt.out.2 of the same pixel (dotted curve). In Fig. 8 the optical input Opt.in.1 of one pixel is directed to the optical output Opt.out.2 of its adjacent pixel. Two adjacent pixels thus implement the cross state. From Fig. 8 we can see that there is a 9-ns latency between the time the optical data is received on Opt.in.1 (bold curve) and the time it appears on the optical output Opt.out.2 of the neighboring pixel (dotted curve). The latency shown in Fig. 8 is larger than that shown in Fig. 7 because the optical signal must travel through additional LUT's when it is transferred to the neighboring pixel. These SPICE simulations indicate that a clock period of 10 ns should be sufficient to allow the LUT's to stabilize in each pixel, correspond-

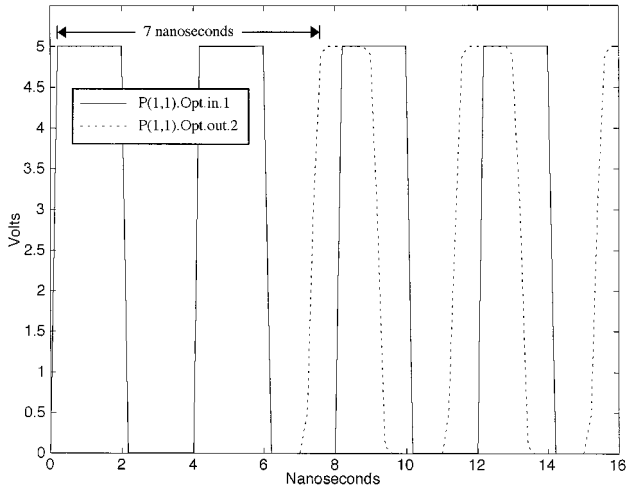

Fig. 7. FP-SPA configured as an optical binary switch in the bar state.

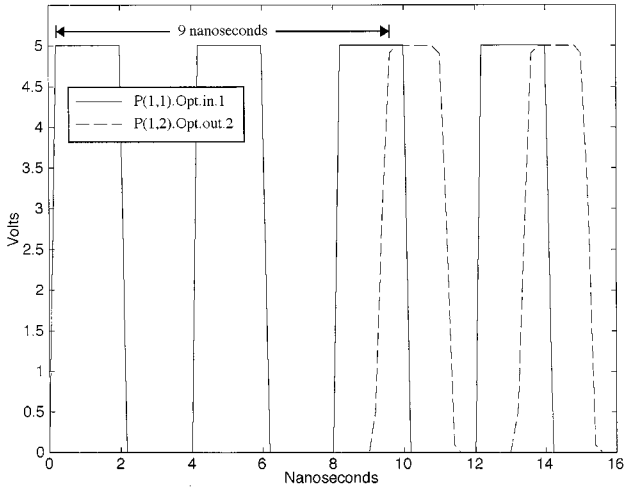

Fig. 8. FP-SPA configured as an optical binary switch in the cross state.

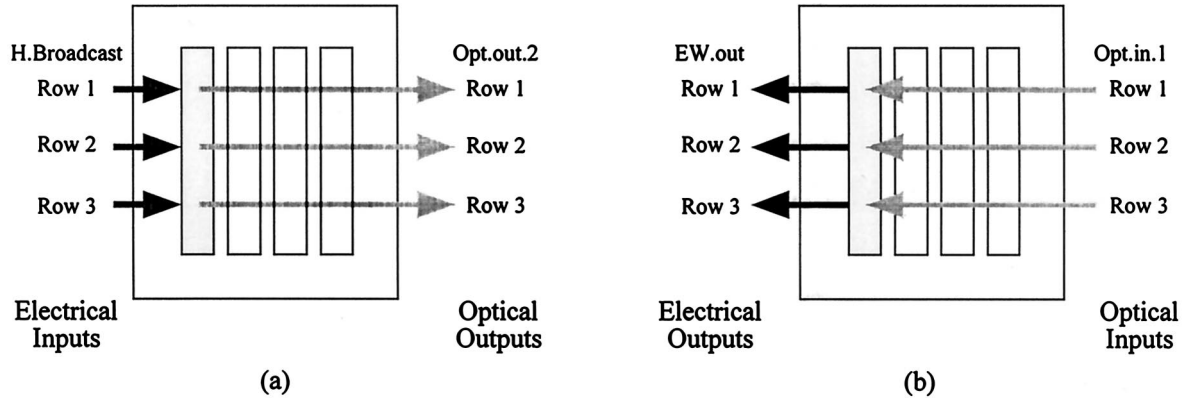

Fig. 9. FP-SPAs configured to implement the hyperplane optical backplane: (a) injection of electrical data onto one optical channel and (b) extraction of electrical data from one optical channel.

ing to a maximum clock rate of approximately 100 MHz.

B. Hyperplane Architecture

The hyperplane is a dynamically reconfigurable free-space intelligent optical backplane architecture.[10] A free-space optical backplane is a collection of bit-parallel optical communication channels (OCC's) created by optically interconnected smart-pixel arrays. Electrical printed circuit boards interconnected by this backplane inject electrical signals into the OCC's through the smart-pixel arrays. These signals are transferred optically to the destination module, where they are extracted and converted back to electrical form by the destination smart-pixel arrays. In addition to injecting the data into and extracting the data from the OCC's, each smart-pixel array must be able to regenerate any incoming signal, allowing it to be directed to the optical inputs of the next smart-pixel array in the path of propagation.

Dynamic programmability gives the hyperplane architecture its power. The hyperplane architecture allows any electrical input to be directed to any OCC and any OCC to be directed to any electrical output channel, without having to resolder the input leads. Also, as a result of the programmability of these smart-pixel arrays, the OCC's can be reconfigured at any time. This provides a dynamic backplane that can be reconfigured on the basis of the application needs at any point. A detailed description and analysis of the hyperplane architecture is given in Ref. 10. Reference 12 describes one potential organization for the optical I/O for the devices for such a backplane, and Ref. 13 describes a custom CMOS design for a hyperplane smart-pixel array.

Figure 9 illustrates the two configurations used to implement the backplane functions. In this application the 4×3 array of pixels is viewed as four columns, each containing 3 bits. In Fig. 9(a) electrical data are injected into the optical backplane by use of the three H.B electrical input pins. These three electrical bits appear on the three optical outputs Opt.out.2 of the pixels in column 1. These optical bits are optically transferred to the neighboring FP-SPA, where they are imaged into the optical inputs Opt.in.1 of column 1. The data are converted to electrical form and routed out of the FP-SPA on the three electrical output pads, EW.out. The optical data are also regenerated and propagated out over the optical outputs, Opt.out.2, of column 1, where they normally would continue to travel down the backplane to the next smart-pixel array.

SPICE simulation results of simple hyperplane-architecture operations are now reported. In Fig. 10 the H.B electrical input data is injected into the Opt.out.2 optical output port of one pixel. This case can be considered as a data-injection operation in which electrical data are injected into the backplane. Figure 10 indicates that 5 ns are sufficient to perform the electrical-to-optical injection operation. In Fig. 11 the optical input data Opt.in.1 of a pixel are directed simultaneously to the E.W.out electrical output pad of the FP-SPA chip and to the Opt.out.2 optical output port. This case can be considered as the data-extraction–data-regeneration operation in which optical data are extracted from the backplane and removed from the chip in electrical form; the same optical data are also propagated down the backplane

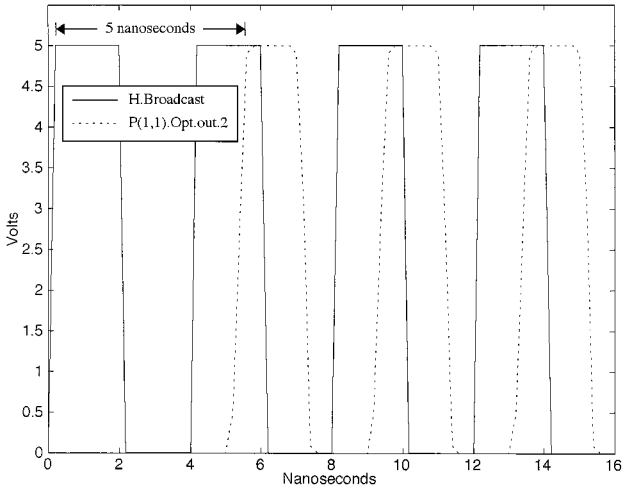

Fig. 10. FP-SPA as a hyperplane: electrical data injection.

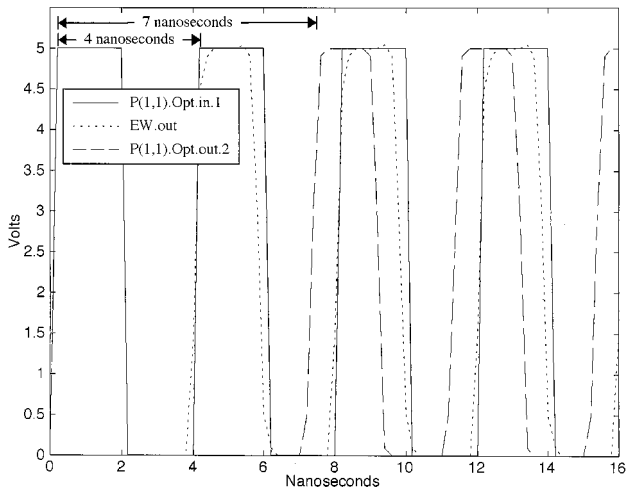

Fig. 11. FP-SPA as a hyperplane: electrical data extraction and optical data regeneration.

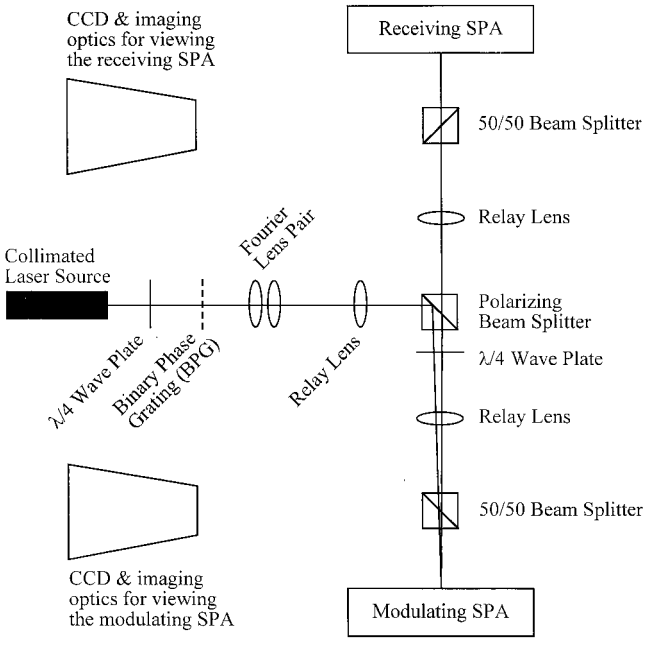

Fig. 12. Simplified optical testing setup.

in optical form. Figure 11 indicates that 4 ns are sufficient for the optical-to-electrical conversion and extraction and that 7 ns are sufficient for the optical signal to be received, regenerated, and propagated forward optically. These SPICE simulations again indicate that a clock period of 10 ns should be sufficient to allow all the LUT's to stabilize in each pixel, corresponding to a maximum clock rate of approximately 100 MHz. Although our SPICE simulations indicate only 1-bit signals, it should be noted that the FP-SPA's treat each channel as an array of parallel bits.

C. Other Applications: Optical ATM Cell Processing

A FP-SPA can be used to implement any digital circuit if its control bits are programmed appropriately. The current prototype is based on a small 2 mm $\times$ 2 mm substrate and contains a 4 $\times$ 3 array of pixels in its interior. If we scaled the design to an approximately 1 cm $\times$ 1 cm CMOS substrate and compressed the layout, the FP-SPA could contain a 24 $\times$ 24 array of programmable pixels and thus would be comparable with the complexity of some commercially available FPGA's. Electrical FPGA's currently offer as many as 250,000 programmable logic gates, and by use of comparable CMOS technology FP-SPA's will also be able to offer approximately the same density of programmable logic gates. Such a field-programmable optoelectronic device would be capable of performing complex logical operations on arrays of optical bits. For example, consider the hyperplane optical backplane application described in Subsection 4.B. Such a chip could be dynamically programmed to transfer ATM cells across an optical backplane. The FP-SPA's could also be programmed to implement logical operations on the ATM cell headers for error control, header translation, or even ATM router functions.[10]

5. Testing Setup and Results

Electrical data are injected into the FP-SPA with a 24-channel data generator (Tektronix, Model DG2020), and electrical outputs are measured with a logic analyzer (Hewlett-Packard, Model 1661C) and a 500-MHz oscilloscope (Hewlett-Packard, Model 54610B). The external optical power source is provided by an 852-nm wavelength, 100-mW laser diode (Model SDL-5712-H1) manufactured by SDL. A binary phase grating is used to produce the desired number of laser spots on the differential SEED pairs in the smart pixels. Spindler and Hoyer Nanobench optomechanics were used to construct the optical testing setup shown in Fig. 12. The distance separating the two FP-SPA's is approximately 20 cm.

The configurations described in Figs. 6–11 were implemented on the FP-SPA's. Our tests indicate that the FP-SPA functions correctly. The functions of each pixel can be programmed by means of downloading the control-bit pattern. Recall that our SPICE measurements indicated that a clock period of approximately 10 ns should be sufficient to allow all the LUT's to stabilize. The SPICE measurements thus predict a maximum clock rate of approximately 100 MHz. Unfortunately, our first-generation devices did not clock at 100 MHz for various reasons. First, the Tanner Research standard cells for the electronic I/O pads used in our design (the TR_PadOut cells) do not support high clock rates. Tanner Research did not supply specifications for its electrical output pads and recommended that users simulate the output pads with SPICE to determine specifications.[11] We simulated the Tanner output pads with a typical 80-pF capacitive load. According to our SPICE simulations the Tanner pads have a maximum output clock rate of approximately 30 MHz; above 30 MHz,

the output resembled a sine wave, and the logic transitions were no longer sharp enough to be useful for digital processing. We are unaware of any confirmed reports of smart-pixel arrays made through the 1995–1996 Lucent/ARPA/COOP with clock at rates exceeding 30 MHz.

Second, because of limitations on design time, we were forced to make some VLSI routing decisions that may have affected the clock rate. The Tanner standard cells all used metal 1 and metal 2 for power and ground, respectively. Normally, the Tanner standard cell design methodology uses metal 3 to route signals between standard cells. However, all optoelectronic design submissions to the Lucent/ARPA/COOP workshop had to reserve metal 3 for the bonding pads for the SEED optical modulators. As a result, we did not have a spare metal layer available for routing signals between standard cells in the locality of the metal 3 bonding pads (normally metal 3 would be used for this purpose). As a result, we were forced to use polysilicon to route some signals between some standard cells, which resulted in larger capacitance and higher resistance when compared with metal 3. Our experimental measurements indicated a maximum clock rate of between 3 and 6 MHz.

We note, however, that the limitation on the use of metal 3 is not unique to our design; rather, it is an inherent constraint when using the CMOS–SEED technology, which uses metal 3 for the flip-chip bonding of the optical I/O onto the CMOS die. There are several ways to design around this constraint. For example, computer-aided-design tools can use metal 3 to route signals between standard cells as long as the optical I/O are not nearby, and we exploited this attribute. However, if the optical I/O are nearby and are using the metal 3 layer, the standard cells underneath the optical I/O must use only two layers of metal. Our FP-SPA design is quite dense, and considerable logic was placed underneath the optical I/O; these standard cells already use metal 1 and metal 2 for power and ground, respectively. Thus these layers cannot be used for routing signals between standard cells beneath the optical I/O. Polysilicon was used to interconnect these standard cells, which has resulted in the lower clock rate.

In general, an optoelectronic technology would be more versatile if an additional layer of metal were made available for routing signals between standard cells to replace the metal 3 layer lost to the flip-chip-bonding process. The latest CMOS processes offer as many as six layers of metal, which would simplify the interconnections of the standard cells. Alternatively, an optoelectronic technology would be more versatile if the standard cells were redesigned to leave two layers of metal free, so that one layer of metal could be used for flip-chip bonding of optical I/O, and the second layer of metal could be used for routing signals between standard cells.

6. Conclusion

In this paper we have described the design, the VLSI implementation, and the optical applications of a first-generation CMOS–SEED FP-SPA. To the best of our knowledge, this device is the first fully operational field-programmable optoelectronic device yet demonstrated. We have reported SPICE simulation results in which we configured this FP-SPA in two sample applications: first as an array of free-space optical binary switches suitable for use in an optical multistage network such as a Benes or a Clos network, and second as an array of dynamically reconfigurable free-space optical switches for a backplane architecture called the hyperplane. We have also described the testing setup and the results of electrical and optical tests that demonstrated the correct functionality of the fabricated FP-SPA device. This device establishes the feasibility of dynamically programmable optoelectronic devices with thousands of transistors per optical I/O bit. Such devices have the potential to reduce significantly the need for the custom design and fabrication of application-specific optoelectronic devices in the same manner that FPGA's have largely eliminated the need for custom device and fabrication of application-specific gate arrays, except in the most demanding applications.

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