1.2V CMOS 1-10GHz Traveling Wave Amplifiers Using Coplanar Waveguides as On-Chip Inductors

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***Abstract* — The feasibility of using standard 0.18µm CMOS technology for low cost wideband radio frequency integrated circuits (RFICs) at ~10GHz is demonstrated. Two different designs of coplanar waveguides (CPWs) have been fabricated for loss comparison and the low-loss design has been identified. The measured loss for the 0.5mm long low-loss design is 0.32dB at 10GHz. A monolithically integrated four-stage traveling wave amplifier (TWA) with n-FET cascode gain cells is proposed, with CPWs as the on-chip inductive elements, and is being fabricated. Simulated results indicate a 10dB gain at 1GHz and unity-gain frequency of 12GHz. This TWA is also compared with measured results of a previously reported five-stage TWA with single n-FET gain cells. A new design for a distributed oscillator using a TWA is proposed and is currently being fabricated.**

***Index Terms* — CMOS RFIC, microwave integrated circuits, coplanar waveguides, MOSFETs, traveling wave amplifiers, temperature effects, distributed oscillator.**

I. Introduction

Traveling wave amplifiers (TWAs) can be used to achieve wide bandwidth for high speed applications, such as 10Gb/s digital and wireless communication systems. Also, since it is difficult to realize inductors on silicon beyond several GHz, they can be replaced by coplanar waveguides (CPW) as on-chip inductive elements as reported in [1], [2], [3].

This paper compares the experimental loss of two different designs of CPWs, first reported in [1] and [2], to identify the low-loss design. The CPW design discussed in [1] uses non-standard 0.18µm CMOS process with four extra-thick Al-Cu metal for ground layers (hereafter called the "multi-layer" CPW). The CPW design reported in [2] used only the top metal of a six metal 0.18µm standard CMOS process (hereafter called the "single-layer" CPW). In both of our CPW designs, the central signal conductor between two ground planes was made of the top metal layer of a six-metal 0.18µm CMOS process. The top metal layer offers low resistivity and a large separation from the lossy silicon substrate as reported in [3]. The multi-layer CPW experimentally exhibits the lowest loss, and was subsequently used in the proposed TWA designs.

Our proposed TWA uses n-FET cascode gain cells and the multi-layer CPWs, as shown in Fig. 1. In contrast, the TWA of [1] uses coplanar striplines (CPS) rather than CPWs. The TWA of [2] uses complex four-transistor gain cells and operates at 10V rather than 1.8V. The TWA of [3] uses single-transistor gain cells. S-parameter simulations in the ADS simulator have been used for circuit design. We have used the TSMC 0.18µm CMOS process ADS model for n-FETs and ADS CPW model for simulations of the circuits. To facilitate comparison, experimental results of the TWA reported in [3] are included, and compared against simulated results for the proposed TWA. From simulations, the proposed TWA improves upon the TWA in [3] by exhibiting a smoother gain slope versus frequency. The TWA is currently being fabricated.

Finally, this paper examines the use of TWAs with low-loss CPWs in three distributed oscillators. The first distributed oscillator based on [3] is similar to that reported in [1] except for the use of CPW over CPS. According to simulations in 0.18µm CMOS, this oscillator shows an oscillation frequency of 14.75 GHz. It has been fabricated and is currently under test and measurement. In contrast, the second oscillator reported in [1] has a measured oscillation frequency of 16.6 GHz and lower output power at the expense of non-standard 0.18µm CMOS process with extra-thick Al-Cu metal layers. The third distributed oscillator considered here, a new design, uses the proposed TWA of Fig. 1 with five stages of cascode gain cells. It exhibits a simulated oscillation frequency of 10.5 GHz. This oscillator is currently being fabricated. It will be shown that the proposed oscillator has higher output power levels, likely due to the use of cascode gain cells.

II. Design of TWA

In a TWA, the FET gain cells are connected with series

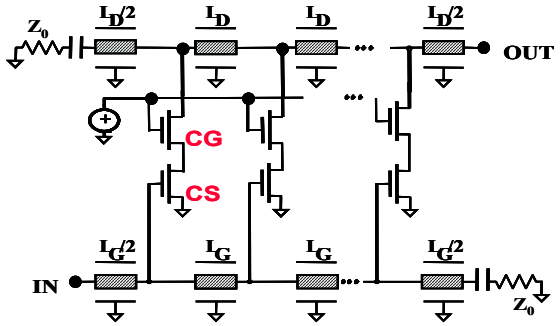

Fig. 1. Schematic of proposed TWA using cascodes.

inductive elements L_G and L_D at the gate and drain terminals, as shown in Fig. 1. These series inductive elements, with shunt capacitances C_g and C_d in the gate and drain nodes of the transistors, form the input and output transmission lines which are coupled by the transconductance of the gain cells [3], [4].

Due to parasitic elements, the performance of the MOSFETs degrades at microwave frequencies, creating challenges for the RFIC designers. C_g and C_d along with the series inductive coplanar transmission line elements periodically form T-type low pass filter structures, L_G-C_g-L_G and L_D-C_d-L_D respectively for the input and output transmission lines [3], [4].

The cut-off frequency of the transmission lines and the line impedances [1] are given by

$$f_c = 1/\pi(LC)^{1/2} \quad , \tag{1}$$

$$Z_{line} = \sqrt{\frac{L_{line}}{C_{line}}} \quad , \tag{2}$$

where L_{line} and C_{line} are the inductance and the capacitance per unit length of the coplanar transmission line.

The characteristic impedance Z_{line} of coplanar transmission lines is selected higher than the desired input and output impedances Z for TWA, because the FET capacitance coming parallel is added to C_{line} , as shown in Eq.(3).

$$Z = \sqrt{\frac{L_{line}}{C_{line}+C_{FET}}} = \frac{Z_{line}}{\sqrt{1+\frac{C_{FET}}{C_{line}}}} = Z_0 = 50\Omega \tag{3}$$

Eq.(3) implies that to achieve a matched condition to an external load Z_0, the intrinsic characteristic impedance of the coplanar transmission line Z_{line} needs to be greater than Z_0. For a 50 Ω matched line when n-FET's loading is included, CPWs of Z_{line}=70 Ω are used [1], [2].

The required inductance L_D of the CPWs in the drain line can be obtained from the value of C_d and the desired cut-off frequency f_{cd} of the periodic LC filter structure as follows [1]

$$L_D = 1/C_d(\pi f_{cd})^2 \quad , \tag{4}$$

$$L_D = Z_o^2 C_d \quad , \tag{5}$$

$$f_{cd}/f_{cg} = 0.8 \quad , \tag{6}$$

$$L_G = 0.8\, L_D \text{ and } \quad C_g = 0.8 C_d \tag{7}$$

In order to obtain a wider bandwidth of the TWA, the phase shift should be a linear function of the frequency to higher frequencies. This can be obtained by the staggering technique [5], in which the cut-off frequencies of the drain and gate lines are different. With the higher cut-off frequency of gate line, the drain line determines the phase shift of the TWA at low frequencies. At higher frequencies, where the phase shift in the drain line is saturated, the gate line determines how the phase of TWA changes with the frequency. Since the TWA's phase shift is the sum of the two phases, it has relative linear dependence on frequency over a wider frequency band.

The optimized staggering factor from ADS optimization is 0.8 as compared to 0.7 [5] as shown in Eq.(6) and is used in Eq.(7). The TWA gain is proportional to N, whereas the bandwidth is limited by the cut-off frequency of the LC filters.

However, when using lossy transmission lines, the optimum number of MOSFET gain cells for the maximization of gain in TWA is given by N_{opt} [3] as

$$N_{opt} = \frac{\ln(A_d/A_g)}{A_d - A_g} \quad , \tag{8}$$

where A_d and A_g are the attenuations per section in Nepers of the input and output lines, respectively. There is no improvement for adding extra n-MOSFET beyond N_{opt} since the loss of the extra waveguides exceeds the gain of the n-FET. The optimum number of MOSFET gain cells for the proposed TWA is four where as it was five in the TWA of [3].

The gate resistance is minimized using multiple finger, double-side connected gates in our designs, which improves the frequency performance and decreases the noise figure of MOSFET.

Multiple finger, double-side connected gates with finger width of 5 μm are connected in parallel for the 50μm channel width of each transistor in the proposed cascode TWA. This is similar to the previously reported five stage TWA of [3] with single n-FET gain cells. The cascode configuration consists of a common-source-connected n-FET feeding into a common-gate-connected n-FET. The proposed TWA layout in Cadence was made with four stages of cascode gain cells, connected along with CPWs, as shown in Fig. 2.

III. Design of CPW

The input impedance Z_{in} of a terminated transmission line is

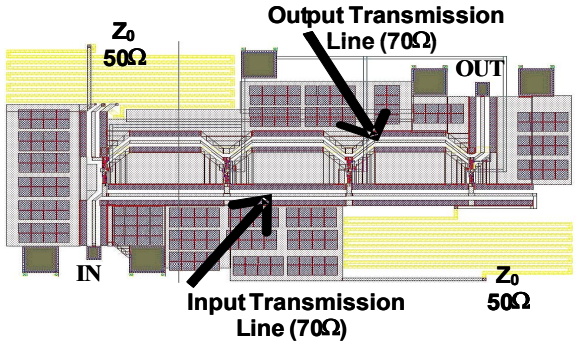

Fig. 2. Layout of the proposed TWA (top view) in 0.18μm CMOS.

a periodic function of line length, and it repeats for multiples of half wavelength, Z_{in} can take all values between inductive to capacitive while varying the line length ℓ . An inductive Z_{in} of the terminated transmission line can be generated if the length ℓ is less than a quarter wavelength λ/4. The lengths of the different CPWs in the layout are close to 0.5mm.

All six metal layers from M1 to M6 are interconnected by vias for the coplanar grounds for the "multi-layer" design of Fig. 3, and finally connected to substrate ground along the whole length of the line [1]. For loss comparison a "single-layer" CPW of Fig. 4 has been fabricated where the coplanar grounds are made of only one metal (M6) [2].

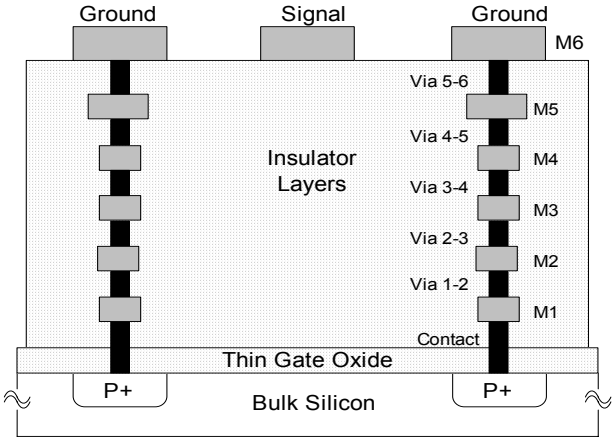

Fig. 3. Cross-sectional schematic of the "multi-layer" CPW design with all metals connected by vias for ground [1].

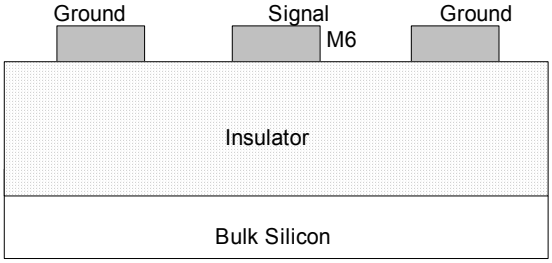

Fig. 4. Cross-sectional schematic of the "single-layer" CPW design with only metal-6 for ground. The insulator thickness is the same (not shown in exact scale) for the designs of Figs. 3 and 4 [2].

IV. Measurements of CPW and TWA

For comparison purposes, measured scattering (S) parameters of CPWs and the TWA reported in [3] are given here along with the simulated results of the proposed TWA.

The loss of the two CPWs considered is shown in Fig. 5. The multi-layer CPW in Fig. 3 has the lowest loss, equal to 0.32dB measured at 10GHz for 0.5mm long design (converted to dB/mm).

The gain $|S_{21}|$ of the single n-FET cells TWA of [3] is repeated here in Fig. 6 for comparison purposes with the gain of the proposed TWA of Fig. 1. The gain of [3] is in good agreement with measured results for CMOS TWAs mentioned in [1], [2]. The simulated gain of the proposed cascode TWA shows no abrupt fall in the gain curve against frequency over 1-12 GHz as shown in Fig. 6 with solid circles (simulated with V_{DS} = 1.8V, V_{GS} = 1.2V and gate voltage for common gate stages is 1.8V).

According to [3], at higher temperatures, a decrease in transconductance g_m and an increase in the terminating resistance value and reflection coefficient (Γ) occurs. The net effect is a small drop of ~ 10% in the measured gain at 25°C versus 75°C [3]. We expect that the proposed cascode TWA will exhibit similar temperature stability because of similar architecture, but measurements are yet to be made. From the measurement and simulations of the stability factor (μ), both of these TWAs are unconditionally stable for any passive load in 1-12GHz range.

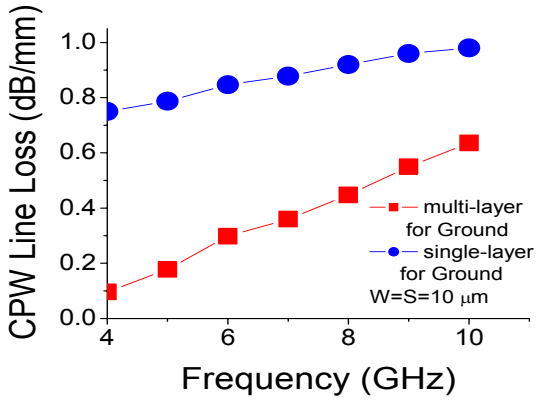

Fig. 5. Loss Comparison of CPWs of the designs of Figs. 3 and 4.

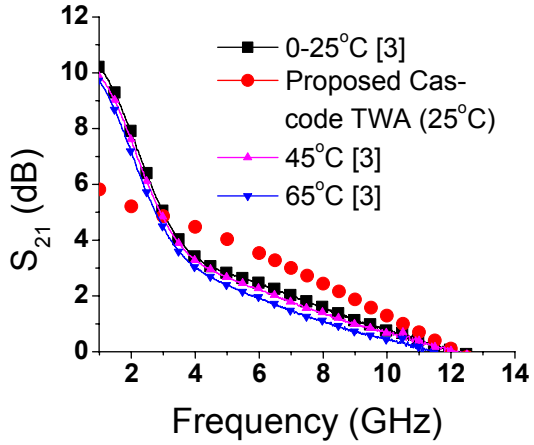

Fig. 6. Simulated gain of the proposed cascode TWA (solid circles) measured gain of the TWA of [3] with temperature effect.

V. Proposed Distributed Oscillator

Two oscillators using CPWs are considered and simulated in the ADS simulator, by connecting the output of the TWA back to the input as illustrated in Figs. 7 and 9. The oscillator proposed at Stanford uses CPS rather than CPW and is similar to the oscillator of Fig. 7 [1]. A new oscillator design is introduced in Fig. 9 by replacing the n-FET cells in Fig. 7 by n-FET cascode cells. Both the oscillators are made of five transistor stages. The feed back connection between the input and the output is critical for the operation of this oscillator. Ideally, the feed back connection should have zero loss and zero delay [1]. This was approximated by folding the gate and drain transmission lines in a U-shape for both the oscillators. The inner U-shape routing is for the gate line while the outer U-shape routing is for the drain line, as shown in the chip layout of Fig. 8 for the oscillator of Fig. 7. This brings the output in the drain line close to the input in the gate line. The

transistors were placed between the inner gate lines and outer drain lines.

From simulations, the oscillation frequency for the oscillator in Fig. 7 is determined to be 14.75 GHz, at drain bias of 1.8V using n-FET width of 60µm as shown in Fig. 10. The simulated phase noise is -110 dBc/Hz at 3MHz offset. The signal power in the harmonics is very low, it is -30 dBm in the 2nd harmonic.

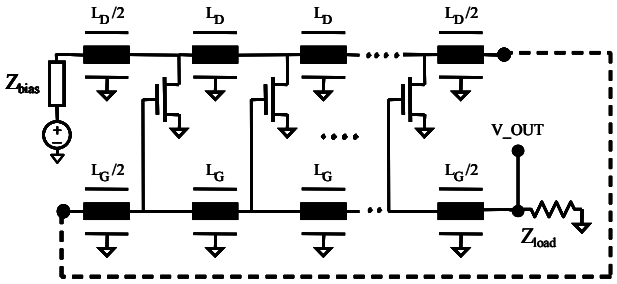

Fig. 7. Schematic of distributed oscillator.

The width of the n-FETs in the oscillator of Fig. 9 was determined to be 50µm from ADS harmonic balance simulations. Using cascodes, we expect a advantage of high output level due to a large impedance at the output, and a higher output power of 2.32 dBm has been noted in simulations at an oscillation frequency of 10.5 GHz, as shown in Fig. 10. The above simulation results of the two oscillator designs of Figs. 7 and 9 are compared in Fig. 10 with V_{DD} = 1.8V. The design of Fig.7 shows a higher oscillation frequency and the design of Fig. 9 has higher output power.

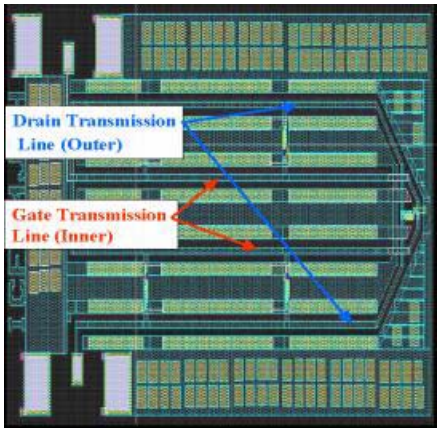

Fig. 8 Layout of oscillator of Fig. 7, chip size 1.5x0.65mm^2.

VI. Conclusion

In this paper, we have proposed a "cascode TWA" using n-FET cascode gain cells, based on a standard 0.18 micron CMOS process. It was shown that based on gain and stability considerations, the proposed cascode TWA can be used as a broad-band amplifier up to 10GHz. The staggering technique for TWAs [5] was implemented for better phase linearity. We have identified the 'multi-layer' CPWs first proposed in [1][2] as low-loss structures (0.32 dB at 10 GHz for 0.5 mm long lines), which take advantage of low metal resistivity and the large separation from the lossy silicon substrate. The cascode TWA also converted into a distributed oscillator with good

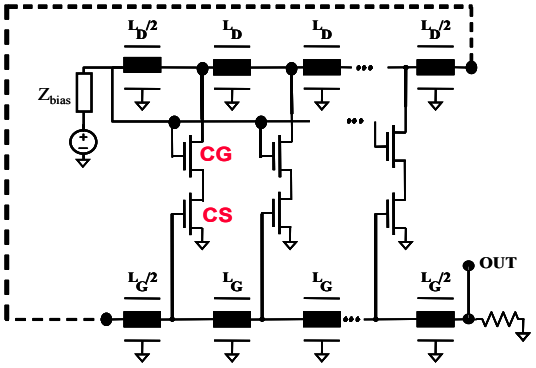

Fig. 9. Proposed distributed oscillator with cascode cells.

harmonic suppression at a high oscillation frequency of around 10 GHz. In comparison, a distributed oscillator using the TWA of [3] exhibited a higher frequency (~15 GHz) but lower output power.

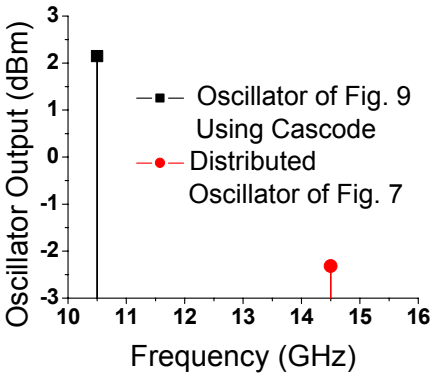

Fig. 10. Oscillator output (dBm) with frequency in GHz.

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REFERENCES

[1] Bendik Kleveland, "CMOS interconnects beyond 10 GHz," *PhD thesis*, Stanford University, California, August 2000.

[2] Brian.M.Frank et al, "Performance of 1-10 GHz TWA in 0.18µm CMOS," *IEEE Microwave and Wireless Ccomponents Letters*, vol. 12, No. 9, pp. 327-329, September 2002.

[3] Kalyan Bhattacharyya and M. Jamal Deen, "Microwave CMOS traveling wave amplifiers – performance and temperature effects," *IEEE Microwave and Wireless Components Letters*, vol. 14, No. 1, pp. 16-18, January 2004.

[4] James.B.Beyer et al, "MESFET distributed amplifier design guidelines," *IEEE Transactions on Microwave Theory and Technique*, vol. MTT-32, No 3, pp 268-275, March 1984.

[5] Brian M.Ballweber et al, "A fully integrated 0.5-5.5 GHz CMOS distributed amplifier," IEEE transactions on SSC, vol. 35, No 2, February 2000, pp 231-239.