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Deep and Narrow Binary Content-Addressable Memories using FPGA-based BRAMs

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Binary Content-Addressable Memories (BCAMs)

Hardware-based Single-Cycle Parallel Search Engines

Write
Stores new data at specific address

Store 'B' in '0' →

0:	B
1:	C
2:	D
3:	A

BCAM

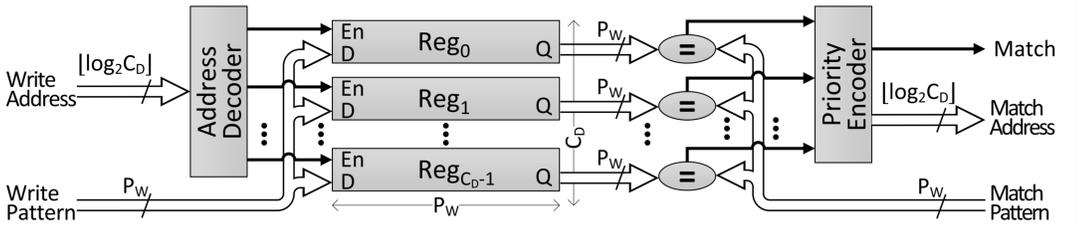
Match
Search all addresses for a given data (pattern)

Search for 'D' →

0:	B
1:	C
2:	D
3:	A

Found in '2'
BCAM

Register-based BCAM: Concurrent register read and compare



Single-cycle Limited resources Complex routing Fits small BCAMs

Traditional Approach: Brute-Force Transposed-Indicators-RAM (TIRAM)

Key idea: Transposed RAM – data becomes address

Write
Write '0' to location 'B'

'0' to 'B' →

A:	3
B:	0
C:	1
D:	2

BCAM

Match
Read location 'D' for match

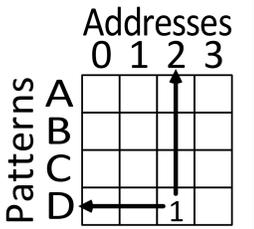
'D' →

A:	3
B:	0
C:	1
D:	2

→ '2'
BCAM

Store data to multiple addresses:

- Specify addresses using one-hot coding
- Each bit indicates a match or "store at location"



Details given in paper, similar to implementations provided by FPGA vendors

SRAM-based BCAM

Single-cycle match / two-cycles write

Depth of CAM is limited by RAM data width

Segmented-Transposed-Indicators (STIRAM)

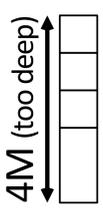
Key contribution:

Support very deep BCAMs

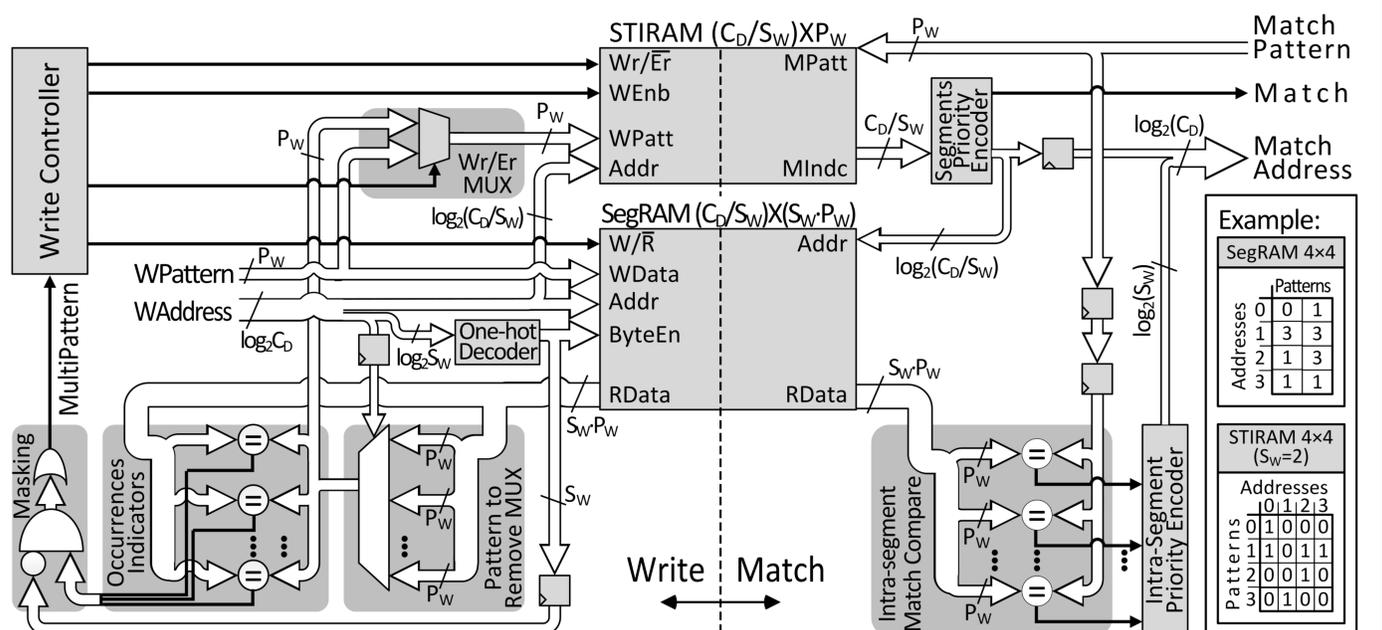
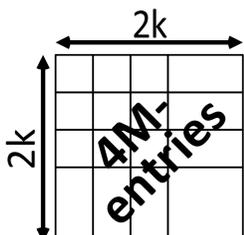
Key idea: Hierarchical search

- Divide address space into segments
- Find a row (segment) with match using a 1D BCAM (e.g. TIRAM)
- Search this row (segment) in parallel for a specific match

1D BCAM



2D BCAM

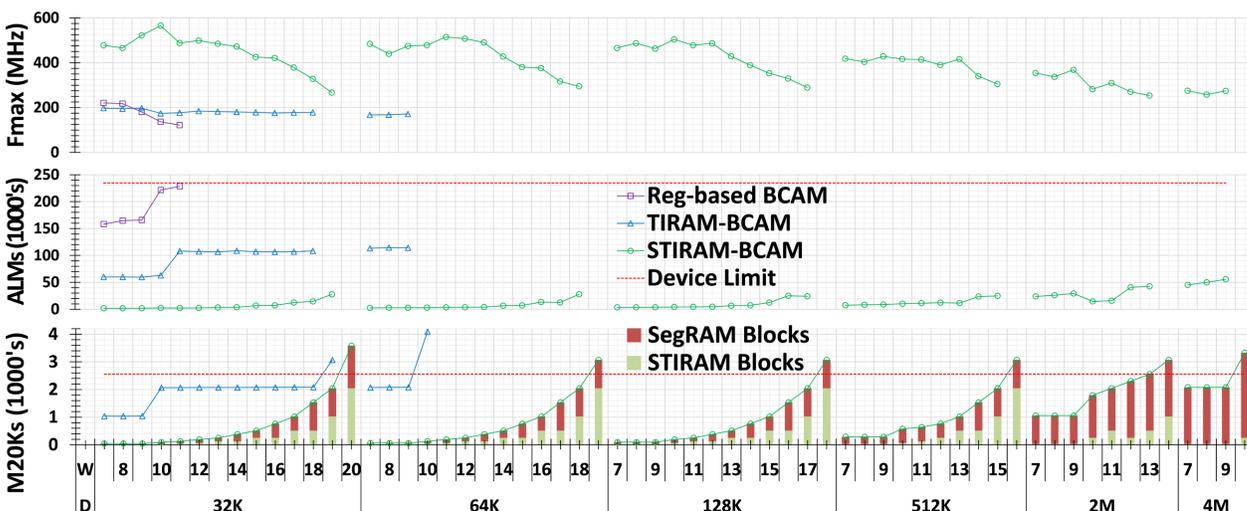


Example:

SegRAM 4x4	
Addresses	Patterns
0	0 1
1	3 3
2	1 3
3	1 1

STIRAM 4x4 (Sw=2)	
Addresses	Patterns
0	1 0 0 0
1	1 0 1 1
2	0 0 1 0
3	0 1 0 0

Experimental Results



Altera's high-performance Stratix V device with 235k ALMs and 2560 M20K blocks

Write : 2 cycles throughput / latency

Match: 1 cycle throughput / 2 cycles latency

Most efficient for deep and narrow CAMs

Can implement a 4M-line CAM

Completely dominates past designs in area, Fmax and compile-time

BRAM consumption is exponential to pattern width



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