Simon Fraser University
School of Engineering Science

ENSC350: Digital System Design
Facts Sheet - Spring 2018

Calendar description:
Presents advanced topics in digital design such as advanced state machine concepts, asynchronous design, hardware description languages, bus interfacing and DSP architecture. It also covers both the architecture and programming or field programmable logic devices.

Prerequisites: (ENSC 215 and either ENSC 250 or CMPT 250) or (ENSC 252 and ENSC 254)
* ENSC 252 and ENSC 254 will be crucial to your success in ENSC 350

Workload: ENSC350 is a 4 credit course

Course Objectives:
This course concentrates on the skills required and challenges encountered when designing digital hardware systems. Digital hardware is becoming increasingly prevalent in society – from the computer used to write this document to the portable devices that we all carry around every day. Digital hardware designers are being required to implement increasingly complex circuitry with decreasing turnaround times. We are using Field-Programmable Gate Arrays (FPGAs) to implement the designs for your labs. The focus is on how to create and test a design from an algorithm along with introducing the FPGA architecture and Computer Aided Design (CAD) Flow. Upon completing this course, you should have developed some of the fundamental skills required by all hardware designers. Topics include:

- Digital design and implementation techniques
- Hardware Description Languages (HDLs) and simulation
- State machines
- Asynchronous design
- Field Programmable Gate Array (FPGA) synthesis, architecture, and technology (Altera, Xilinx)
- Bus interfacing

(See **Appendix A: Tentative Lectures schedule** for more details)

Course Staff:
Instructor:

Dr. Ameer Abdelhadi	<aabdelha@sfu.ca>	Office Hours: Tu 4:30PM–5:30PM, ASB 10827

Teaching Assistants:

Eric Matthews	<eric_matthews@sfu.ca>	Office Hours: Th 4:30PM–5:30PM, ASB 10810*
Maryam RasouliDanesh	<rasoulid@sfu.ca>	Office Hours: Fr 1:00PM–2:00PM, ASB 10810*

Scheduled Activities:
Lectures:

D100	Tu 2:30 PM – 4:20 PM AQ 3181, Burnaby
D100	Th 2:30 PM – 4:20 PM SSCB 9200, Burnaby

Labs:

LA01	Fr 8:30 AM – 10:20 AM ASB 10810*, Burnaby
LA02	Fr 10:30 AM – 12:20 PM ASB 10810*, Burnaby
LA04	Fr 2:30 PM – 4:20 PM ASB 10810*, Burnaby

(See **Appendix B: Semester Schedule** for more details)

* The Digital Hardware Laboratory has two doors numbered ASB 10810 and ASB 10808.
The card reader is associated with ASB 10808. Please enter through this door.

Course Web Page:

The course web page is hosted on canvas, https://canvas.sfu.ca/courses/37182. Handouts will be posted on Canvas before each lecture so that you can print them out before class. We will be using Canvas for the discussion board and information dissemination. Your grades will be posted on Canvas.

Labs:

There will be a significant lab component to this course requiring students to create HDL designs using the Altera DE2-115 boards. You will sign out these boards for the term. The appropriate software has been installed in the Digital Design Lab. Each lab group will consist of two individuals.

You should already be familiar with the lab tools and equipment from ENSC 252/263. The lab component will be comprised of a series of design challenges that will be used to reinforce concepts introduced in lecture. Each group will be responsible for ***all of the design components*** and will be questioned individually on the functionality and operation of their design during its demonstration. Further details on each of these labs will be given in separate handouts.

Throughout the semester, students are required to follow the lab policies outlined by the School of Engineering Science along with those provided in the lab handouts. Please read them carefully.

Each lab assignment will span two weeks. The first week is intended to be a work-week, where you spend the lab working on the tasks. A TA will be available to help you if you run into problems. The second week is primarily for marking (you should not expect help from the TA during the second week). You should expect that you must do some work on your own (at home or in the lab outside of lab hours) as well. You most certainly cannot finish the lab if you don't start until the marking week.

Tentative labs outline:

Lab 1 (Jan. 12: working, Jan. 19: marking): State Machines and the LCD - a simple LCD driver
Lab 2 (Jan. 26: working, Feb. 2: marking): Datapaths – an implementation of a Roulette engine
Lab 3 (Feb. 9: working, Feb. 23: marking): VGA Controller / Drawing Lines – a VGA adapter embedded core
Lab 4 (Mar. 2: working, Mar. 9: marking): Sound and Timers – a sound generator
Lab 5 (Mar. 16: working, Mar. 23: marking): Memory, Scheduling, & Decryption – an RC4 Decryption circuit
Lab 6 (Apr. 6: working & marking): System Bus & Custom Instructions - interfacing & manipulating RISCV ISA

You are responsible for treating the lab equipment with proper care and respect – the same as you would any of your own possessions!! Failure to do so will affect your grade!

Software Requirements:

- You will require the use of software circuit design tools. The primary tools will be the integrated FPGA development environment (IDE), Quartus Prme. and the industry standard VHDL simulator, ModelSim-Altera. Fully-functional professional versions are installed in ASB 10808/10.
- You should download and install the free Quartus Prime Lite Edition, available from the Altera website. (www.altera.com)
- You should download the accompanying DE2-115 CD-ROM (NXP USB) Version 1.0.6 for the DE2-115 Development kit available from (www.terasic.com)
- A vector drawing program, Visio, by microsoft, is also available on most computers administered by the school of engineering science. Visio is extremely easy to use and will be immensely useful in preparing documents for this and future Ensc courses.
- Students may be able to acquire a license for Visio through the Schools MSDNAA using your DreamSpark Account. Please ask the school of engineering sciences IT services for further information. ensc-help@sfu.ca

Suggested HDL Reference Books:

Your ***textbook from 252 will work as an HDL reference***. For a VHDL to Verilog, there are Custom Courseware copies of Douglas J. Smith's HDL Chip Design: A Pracitical Guide for Designing, Synthesizing & Simulating ASICs and FPGAs Using VHDL or Verilog that should be available at the bookstore. Also, check for online materials (I'll try to post some on the course webpage).

Quizzes and Final Examination:

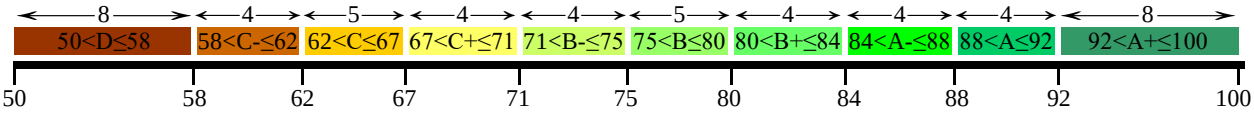
Short multiple-choice quizzes: You will have 16 short multiple-choice i-Clicker quizzes every lecture.
Design quizzes: You will have 6 design quizzes during lecture time every second week.
Final Examination: Your final exam is scheduled for Apr 17, 2018 3:30PM–6:30PM; Location: TBA.

Mark Breakdown:

Students' final grade will be assessed from quizzes, labwork and exam scores. The exact weighting will be set at the end of the semester however students may find the following tentative proposal useful when assessing one's priorities.

- 16 × i-Clicker quizzes 8 % (0.5% each)
- 6 × Design quizzes 18% (3% each)
- 6 × Lab experiments 24 % (4% each)
- Final Exam 50 %

Approximate letter grades conversion:



(FYI, see **Appendix C: Regrades and Penalties**)

Policy for Absences

The only acceptable documentation for medical absences, whether personal or for a family member, is a complete SFU Certificate of Illness, with Section 1 filled out. You must see the doctor while sick, and on the exam, quiz or lab date (or earlier, if the statement states that you can only return to studies/exams after the relevant date).
In all cases, if you do not qualify for an exemption, you receive a '0' for the work missed.
(See **Appendix D: Policy for Absences** for more details)

Academic Integrity:

SFU Code of Academic Integrity and Good Conduct: http://www.sfu.ca/policies/gazette/student/s10-01.html
Students must be aware that the University and the School of Engineering Science have a zero tolerance for cheating. Students in caught cheating may be subjected to any combination of the following penalties.

- failure in a particular assignment,
- failure in the course,
- a written record on file with the Director of Engineering Science,
- a written record on file with the SFU Registrar's office,
- an FD (Failed for Dishonesty) an annotation on their transcripts,
- suspension/expulsion from the university.

Students should note that the potential benefits of cheating are far outweighed by the potential penalties.

While I promote team work and helping each other, code copying and plagiarism will ***NOT*** be tolerated. Any individual found copying code from other class members or the web will receive an automatic ***0*** on the ***entire*** lab component. Similarly, anyone found copying during quizzes, midterms, or the final will receive a ***0*** for the ***entire*** testing component. Any code copying or plagiarism will result in an automatic ***0*** for the class participation bonus.

The lectures and displays (and all material) delivered or provided in this course (ensc350) by Dr. Abdelhadi, including any visual or audio recording thereof, are subject to copyright owned by Dr, Abdelhadi. ***It is prohibited to record or copy by any means, in any format, openly or surreptitiously, in whole or in part, in the absence of express written permission from Dr. Abdelhadi any of the lectures, materials provided or published in any form during or from this course.*** This copyright also applies to any guest lecturers invited to the class.

You must read and sign **Appendix E: A Statement of Expected Professional Integrity Standards & Consequences**. You will not be allowed to sign out or use any of the lab equipment until you have signed this form.

Appendix A: Tentative Lectures schedule

Date	Lecture #	Slide set #	Topic
Jan. 4	1	1	Introduction
Jan. 9	2	2	Review, Processes, and Lab 1
Jan. 11	3	2	Review, Processes, and Lab 1, cont'd.
Jan. 16	4	3	Synthesizable VHDL
Jan. 18	5	4	VHDL Types and Variables, and an Introduction to Datapaths
Jan. 23	6	5	Introduction to Lab 2 and Testbenches
Jan. 25	7	6	More VHDL Types, Loops, Generates, Tri-State
Jan. 30	8	7	More Complex Datapaths
Feb. 1	9	7	More Complex Datapaths, cont'd.
Feb. 6	10	8	Fractional Numbers
Feb. 8	11	9	On-Chip In-System Debug and Introduction to Lab 3
Feb. 20	12	9	On-Chip In-System Debug and Introduction to Lab 3, cont’d.
Feb. 22	13	10	Optimization and FPGA Architectures
Feb. 27	14	10	Optimization and FPGA Architectures, cont'd.
Mar. 1	15	11	Introduction to Lab 4
Mar. 6	16	12	On-Chip Memories: Application-Specific Memory Hierarchies & Scheduling
Mar. 8	17	13	Introduction to Lab 5
Mar. 13	18	15	Circuit Timing: Part 1: The Basics
Mar. 15	19	16	Circuit Timing: Part 2: Practical Issues
Mar. 20	20	17	Metastability and Synchronization
Mar. 22	21	18	Power
Mar. 27	22	19	Introduction to SoC Design and Lab 6
Mar. 29	23	20	Asynchronous State Machines
Apr. 3	24	21	Asynchronous Datapaths
Apr. 5	25	22	High-Level Synthesis
Apr. 10	26	23	Course review

Appendix B: Semester Schedule

	Sunday	Monday	Tuesday	Wednesday	Thursday	Friday	Saturday	
1		**1**	**2**	**3** Classes start	**4** Lecture 1* Eric's office hour†	**5**	**6**	January
2	**7**	**8**	**9** Lecture 2‡ Ameer's office hour§	**10**	**11** Lecture 3* Eric's office hour†	**12** Lab 1: Working** Maryam's office hour††	**13**	
3	**14**	**15**	**16** Lecture 4‡ i-Clicker quiz 1‡ Ameer's office hour§ Last day to drop	**17**	**18** Lecture 5* Design quiz 1* Eric's office hour†	**19** Lab 1: Marking** Maryam's office hour††	**20**	
4	**21**	**22**	**23** Lecture 6‡ i-Clicker quiz 2‡ Ameer's office hour§	**24**	**25** Lecture 7* i-Clicker quiz 3* Eric's office hour†	**26** Lab 2: Working** Maryam's office hour††	**27**	
5	**28**	**29**	**30** Lecture 8‡ i-Clicker quiz 4‡ Ameer's office hour§	**31**	**1** Lecture 9* Design quiz 2* Eric's office hour†	**2** Lab 2: Marking** Maryam's office hour††	**3**	February
6	**4**	**5**	**6** Lecture 10‡ i-Clicker quiz 5‡ Ameer's office hour§ Last day to drop/WD	**7**	**8** Lecture 11* i-Clicker quiz 6* Eric's office hour†	**9** Lab 3: Working** Maryam's office hour††	**10**	
7	**11**	**12** Family Day	**13** Reading break	**14** Reading break	**15** Reading break	**16** Reading break	**17** Reading break	
8	18 Reading break	**19**	**20** Lecture 12‡ i-Clicker quiz‡ Ameer's office hour§	**21**	**22** Lecture 13* Design quiz 3* Eric's office hour†	**23** Lab 3: Marking** Maryam's office hour††	**24**	
9	**25**	**26**	**27** Lecture 14‡ i-Clicker quiz 8‡ Ameer's office hour§	**28**	**1** Lecture 15* i-Clicker quiz 9* Eric's office hour†	**2** Lab 4: Working** Maryam's office hour††	**3**	March
10	**4**	**5**	**6** Lecture 16‡ i-Clicker quiz 10‡ Ameer's office hour§	**7**	**8** Lecture 17* Design quiz 4* Eric's office hour†	**9** Lab 4: Marking** Maryam's office hour††	**10**	
11	**11**	**12**	**13** Lecture 18‡ i-Clicker quiz 11‡ Ameer's office hour§	**14**	**15** Lecture 19* i-Clicker quiz 12* Eric's office hour†	**16** Lab 5: Working** Maryam's office hour††	**17**	
12	**18**	**19**	**20** Lecture 20‡ i-Clicker quiz 13‡ Ameer's office hour§	**21**	**22** Lecture 21* Design quiz 5* Eric's office hour†	**23** Lab 5: Marking** Maryam's office hour††	**24**	
13	**25**	**26**	**27** Lecture 22‡ i-Clicker quiz 14‡ Ameer's office hour§	**28**	**29** Lecture 23* i-Clicker quiz 15* Eric's office hour†	**30** Good Friday	**31**	
14	**1**	**2** Easter Monday	**3** Lecture 24‡ i-Clicker quiz 16‡ Ameer's office hour§	**4**	**5** Lecture 25* Design quiz 6* Eric's office hour†	**6** Lab 6: Working & Marking** Maryam's office hour††	**7**	April
15	**8**	**9**	**10** Lecture 26‡ Ameer's office hour§ Last day of classes Last day to drop/WE	**11**	**12** Eric's office hour†	**13** Maryam's office hour††	**14**	
16	**15**	**16**	**17** Final examination‡‡	**18**	**19**	**20** Final grade posting	**21**	
17	**22**	**23**	**24** Makeup exam§§	**25** Exam showing*	**26** Last day for appeals	**27** Appeals decision	**28**	

Legend:
Lectures | Office Hours | dates/deadlines
Quizzes/Exams | Labs | No Classes

* 2:30PM–4:20PM, SSCB 9200, Burnaby
† 4:30PM–5:30PM, ASB 10810, Burnaby (entrance through ASB 10808)
‡ 2:30PM–4:20PM, AQ 3181, Burnaby
§ 4:30PM–5:30PM, ASB 10827, Burnaby
** 8:30AM–10:20AM(LA01), 10:30AM–12:20PM(LA01), 2:30PM–4:20PM(LA01), ASB 10810 (entrance through ASB 10808)
†† 1:00PM–2:00PM, ASB 10810, Burnaby (entrance through ASB 10808)
‡‡ 3:30PM–6:30PM; Location: TBA
§§ Time and place TBD

Appendix C: Regrades and Penalties

You may request a regrade on quizzes and/or on the final exam, but not on labs.
If there is a mistake in totaling points, just show the responsible TA your exam and do not formally request a regrade. Your grade will be changed automatically.

To request more points on a particular question, you must do BOTH of the following:

- Submit your request to the responsible TA within three days from the first day when the test is available for viewing.
- Detail, in writing, where and why you believe there was an error. Generic statements such as, but not limited to, "my explanation was close" or "I deserve partial credit" do not satisfy this requirement: you must be specific about which parts of your answer deserve more credit and how they relate to a correct solution. If your request does not satisfy both of the above criteria, it will be rejected.

Make sure to include ALL disputed questions on your request: you can submit at most one request per test.
The professor or the TA will regrade the listed question(s): your score may increase, stay the same, or decrease. **You will also lose points if the Professor or the TA notices that too many points were awarded anywhere else on the exam.**

To discourage "fishing for points," the professor or the TA may deduct one point for each question[*] each time you do any of the following:

- Ask for regrading without justifiable explanation, such as, but not limited to, "my explanation was close", "I deserve partial credit", "I need at least C to get a co-op", "I need at least D to stay in school", or "I'm only one point shay of the next letter grade"
- Ask about exceptions to the formulae/policies stated in course documents. In particular, the weights of exams and the grading formula will not be modified, and personal circumstances will not be considered in determining final grades (unless an SFU health professional advises to the contrary).
- Ask the professor or the TA to reconsider your score for a lab. (This does not include asking for feedback, which you are encouraged to do, or for an explanation of your score.)

This policy aims to ensure that professor's and the TAs' time and energy are spent actually teaching (and evaluating) rather than dealing with avoidable administrative issues.

[*] Each part of a multi-part problem is a "question."

Appendix D: Policy for Absences

Please read this document before requesting an exemption.
Any documentation can be scanned and submitted via email.
The only acceptable documentation for medical absences, whether personal or for a family member, is a complete SFU Certificate of Illness, with Section 1 filled out. You must see the doctor while sick, and on the exam, quiz or lab date (or earlier, if the statement states that you can only return to studies/exams after the relevant date).
In all cases, if you do not qualify for an exemption, you receive a '0' for the work missed.
Valid reasons for missing a quiz or a lab

- Personal or family emergency (medical or accident): documentation required within ten calendar days of the quiz or lab*
- Documented reason that I approve at least seven days in advance (*e.g.* important event)

* If you miss class on a quiz date, you will not know whether you were supposed to take a quiz. It is your responsibility to ask promptly so that you can make the deadline.
If you missed a quiz, and either of the above conditions is met, your semester score will simply be computed ignoring the quiz that you missed. The weighing between the total quizzes portion and your final exam score will not be adjusted unless you are evaluated fewer times than twice during the semester. You will not have the option of a makeup.
If you missed a lab, and either of the above conditions is met, you must reschedule your lab marking with the responsible TA. It is your responsibility to ask for deferred grading. None of your lab grades will be ignored.

Valid Reasons for Missing the Final

- Personal* emergency (medical or accident): email the instructor within 24 hours of the start of the final AND provide documentation within 96 hours of start the final
- Religious reason: advise the instructor during the first week of classes

Please drop this course if you might miss the final for any other reason.

You are eligible for a makeup only if: i) one of the above conditions is satisfied, AND ii) you have a reasonable chance of passing the course, defined as having a D or better based on your semester score – the threshold will be announced before the final.
You must also submit, with 24 hours of the start of this course's final, a list of the other SFU courses that you are taking and the times of their final exams. The instructor chooses the time of the makeup, which can be any time that does not make you miss another SFU final or have three SFU final exams within a 24-hour period. **You may therefore have to change your travel plans or your work schedule. Any misrepresentation will result in a grade of F or FD.**

* Family situations are not acceptable for missing the final, unless they are medical in nature AND serious (not just a cold or a flu) AND unforeseeable (chronic illnesses only qualify if there are new developments).

Appendix E: A Statement of Expected Professional Integrity Standards & Consequences

While I promote team work and helping each other, unethical and unprofessional behaviour will not be tolerated. Specifically:

1. Code copying and plagiarism will ***NOT*** be tolerated. Any individual found using code from other class members or the web ***instead of their own design work*** will ***minimally*** receive an automatic ***0*** on the ***entire*** lab component (25% off their final mark). Furthermore, the instructor will recommend to the director that an FD (failure for academic dishonesty) be awarded.
2. Anyone found hacking into another lab group's machine OR distributing a teammate's code without their knowledge (i.e. actively stealing intellectual property that does not belong to them) will ***minimally*** receive an automatic ***0*** on the ***entire*** lab component (25% off their final mark). Furthermore, the instructor will recommend to the director that an FD (failure for academic dishonesty) be awarded.
3. Similarly, anyone found copying during tests will receive a ***0*** for the ***entire*** testing component (25% for the Midterm and 50% for the final). Furthermore, the instructor will recommend to the director that an FD (failure for academic dishonesty) be awarded.

In all cases of unethical and unprofessional behaviour, a letter will be added to the student's file recommending that they be ejected from the program should this behaviour be demonstrated a second time in a different course. Also, this behaviour will result in an automatic ***0*** for any class participation bonus.

Finally, the lectures and displays (and all other materials, including, but not limited to the labs and handouts) delivered or provided in this course (EnSc350) by Dr. Abdelhadi, including any visual or audio recording thereof, are subject to copyright owned by Dr. Abdelhadi. ***It is prohibited to record or copy by any means, in any format, openly or surreptitiously, in whole or in part, in the absence of express written permission from Dr. Abdelhadi any of the lectures, materials provided or published in any form during or from this course.*** This copyright also applies to any guest lecturers invited to the class and all source materials provided by Intel Corp.

By signing the following form, you agree to:

- recognize your Professional responsibilities for ethical behavior within this course, and
- Indemnify the instructor, Dr. Abdelhadi, and all of her employees, agents and representatives, and to hold them harmless from any and all claims and liabilities (including lawyers' fees) resulting from any unethical or unprofessional behavior exhibited during this course.

Please note: You will not be allowed to sign out or use any of the lab equipment until you have signed this form.

_____ _____

Student Name (Print) Student Number

_____ _____

Signature Date