MOSFET Modeling for Low Noise, RF Circuit Design

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RF Performance of MOSFETs

- DUTs are fabricated in 0.18 \( \mu m \) CMOS technology and measured at \( V_{DS} = 1.0 \) V.
- Maximum \( f_T \) is around 50 GHz and the best \( NF_{min} \) is about 0.5 dB at 2 GHz.
What's inside your Cellular Phone?

Diagram showing the components of a cellular phone:
- Diplexer
- Low frequency signal processing
- Band-pass filter
- LNA
- PA
- LO

The diagram illustrates the flow of signals through these components.
Outline

• RF Modeling of MOSFETs
  - Parasitic resistances and capacitances
  - Non-Quasi-Static (NQS) effects

• Noise Modeling of MOSFETs
  - What does the device noise look like?
  - Equivalent noise circuit model
  - Channel noise, Induced gate noise and their correlations
  - Noise modeling for RF IC applications

• Design Strategy of low noise amplifiers (LNA)
  - Selection of the device size, geometry and bias condition
  - Impact of the Accuracy of Noise Sources

• Conclusions
RF Model Including Parasitics

Gate Resistance

- At high frequencies, the effective gate resistance consists of the polysilicon resistance ($R_{g,poly}$) and distributed channel resistance ($R_{ch}$).

![Gate Resistance Diagram]

```plaintext
R_{g,poly}

R_{ch}
```
Source and Drain Resistances

\[ R_{s,d} = R_{\text{via}} + R_{\text{salicide}} + R_c + R_{\text{ldd}} \approx R_c + R_{\text{ldd}} \]

- The source and drain series resistances include the via resistance \( R_{\text{via}} \), the salicide resistance \( R_{\text{salicide}} \), the salicide-to-salicide contact resistance \( R_c \) and the sheet resistance in the LDD region \( R_{\text{ldd}} \).
• At high frequencies, the signal at the drain will be coupled to the source and the body terminals through the substrate resistances ($R_{db}$, $R_{sb}$ and $R_{dsb}$) and junction capacitances at drain and source.
Parasitic Capacitances

Diagram showing various capacitances such as $C_{FO}$, $C_{GSOL}$, $C_{F1}$, $C_{GSI}$, $C_{GDI}$, $C_{F1}$, $C_{GDOL}$, $C_{GDO}$, $C_{JS}$, $C_{JD}$, and labels for terminals $G$, $O$, $S$, $D$, $n^+$, and $xJ$. P-sub refers to the P-type substrate.
Results of $Y$- Parameter Fitting

$f_T$ vs. Bias Currents

$+$: $V_d=0.5V$
$o$: $V_d=1V$
$*$: $V_d=1.5V$

Solid lines: Model
Symbols: Measured data

IDS (A)

$I_{DS} (A)$

$f_T$ (GHz)
NQS Effects

Symbols: Measured data
Solid lines: Model with NQS
Dotted lines: Model without NQS

W=10x15µm
L=1.35µm

Vgs=1V
Vds=1V
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What does the Noise Look Like?

- Time
- Frequency
- Channel
- IDS
- 1/f noise
- White noise
- Induced gate noise
- Channel noise
- E lateral field

Diagram:

- Source
- Drain
- Gate
- Substrate (Body)
- V_G
- V_D
- V_o

Equation:

\[ I_{DS} = I_o \]

\[ g_{DS}(x) \Delta v(x) \]

\[ 1/f \text{ noise} \]

\[ \text{white noise} \]
Why the Device Noise Matters?

- The battery life time and the distance between the wireless components will be limited by the noise floor of the front-end amplifier.
AC Noise Model of MOSFETs

\[ y_m = g_m \times (1 - j\omega \tau) \]
Noise Source Extraction

RF & Noise Parameter Measurements

De-embedding of Pads and Interconnections

Intrinsic S-Parameters

Parameter Extraction & Verification

Y-Parameter Calculation at two-port (33'-44')

Intrinsic Noise Parameters

Noise Parameter Deembedding to ports 33' and 44'

Extracting $i_g^2$, $i_d^2$ and $i_g i_d^*$

Noise Parameter Verification

The noise sources are directly extracted from intrinsic noise parameters.

\( \dot{i_d}^2 \) is frequency independent and \( \dot{i_g}^2 \) is proportional to \( f^2 \).
Noise Sources vs. Frequency

- Cross-correlation $C$ is defined as $C = \frac{\langle i_g i_d^* \rangle}{\sqrt{\langle i_g^2 \rangle \langle i_d^2 \rangle}}$.
- $\bar{i_g i_d^*}$ is proportional to $f$, and $C$ is frequency independent.
Noise Parameters vs. Frequency

- The extracted noise sources are fed into the a.c. noise model for noise source verification.
- The induced gate noise has a great influence on the $\text{NF}_{\text{min}}$ of long channel devices but does not affect the equivalent noise resistance.
• **Channel-length modulation (CLM) effect** ⇒ higher local output conductance

\[ g_{DS}(x_0) \Rightarrow \overline{i_d^2} \] increased at higher \( V_{DS} \) for \( L = 0.18 \ \mu m \) devices.
noise parameters vs. models

- The channel noise equations $\overline{i^2_d} = 8kTg_m/3$ and $\overline{i^2_d} = 8kTg_{do}/3$ suggested for the long channel devices predict lower equivalent noise resistance $R_n$. 

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Sec. 11.1, IEEE CICC2002, Orlando, Florida
\[
\gamma, \delta \text{ and } \varepsilon \text{ are } \\
\gamma = \frac{\overline{I_d^2}}{4kTg_{do}}, \quad \delta = \frac{\overline{I_g \cdot g_{do}}}{4kT \omega^2 C_{GS}^2} \quad \text{and} \quad \varepsilon = \frac{\overline{I_g I_d^*}}{j4kT \omega C_{GS}}.
\]

- Coefficients vs. Channel Lengths
- \(W=10\times6\mu m\)
- \(V_{DS}=1.0V\)
- \(V_{GS}=1.2V\)
Cross Section of MOSFET Channel

- $V_{DS}$
- $V_{DS_{sat}}$
- $L_{elec}$
- $\Delta L$
- $L_{eff}$
- $E_{crit}$
- $v_{sat}$
- $x$
Channel Noise in Linear Region

- Noise current from the gradual channel region:

\[
\overline{i_d^2} = \frac{4kT_o}{L_{eff}^2} \mu_{eff}(-Q_{inv}) + \delta_{hot} \frac{4kT_o I_{ds}}{L_{eff}^2 E_{crit}^2} V_{DS}
\]

\[
Q_{inv} = -W_{eff} L_{eff} C_{ox} \cdot \left( V_{GT} - \frac{A_b V_{DS}}{2} + \frac{A_b^2 V_{DS}^2}{12 \cdot \left( V_{GT} - \frac{A_b V_{DS}}{2} \right)} \right)
\]

- \( \delta_{hot} \) is used to model the hot electron effect.
- \( V_{DS} \) becomes \( V_{DSsat} \) in the saturation mode.
- Using \( L_{elec} \) instead of \( L_{eff} \) in the saturation mode.
Channel Noise in Saturation Region

- Noise current from velocity saturation is zero [1]:
  - Thermal noise theory ($4kTR$) cannot be applied in the velocity saturation region.
  - Physical noise mechanism in the velocity saturation region is unknown - though a *drifting dipole layer model* [2] and a *diffusion noise model* [3] were proposed for the thermal noise modeling of FETs.
  - For a given voltage fluctuation, it generates zero noise fluctuation because of the local $g_{DS}(x_o) = 0$.

Channel Noise vs. $V_{GS}$ and $V_{DS}$

- Hot electron is not important ($\delta_{\text{hot}} = 0$) in the channel noise modeling.
- No noise current from velocity saturation (region II) is found.
- Using $L_{\text{elec}}$ to catch the increasing trend in the channel noise vs. $V_{DS}$ characteristics.
Simulated $\gamma$ for long channel devices $L = 10 \, \mu m$ is 0.68 at $V_{GS} = 1.8 \, V$ which is close to the theoretical value $2/3$.

The $\gamma$ value increases from 0.68 to 1.2 or 1.8 (depending on the $V_{GS}$ bias) when the channel length is decreased because of CLM effect.
Gate Noise and Correlation Noise

- Induced gate noise from position $x_o$ in region I:

$$\Delta i_g(x_o) = j\omega WL_{elec} C_{ox} \frac{C_{GS}}{I_{ds}} \left[ \frac{\Delta i_d(x_o)}{L_{elec}} \left\{ g(V_o) \Delta v(x_o) \right\} \right] \left[ V_{as} - V(x_o) \right]$$

where $V_{as} = V_{DS} - \frac{1}{2} (V_{GS} - V_{TH}) V_{DS} - \frac{1}{6} V_{DS}^2$

$$V_{GS} - V_{TH} - \frac{1}{2} V_{DS}$$

- Induced gate noise $\Delta i_g(x_o)$ is fully correlated with the channel thermal noise $\Delta i_d(x_o)$.

- $V_{DS}$ becomes $V_{DSSat}$ in the saturation mode.
Gate and Correlation Noise vs. $f$

- Induced gate noise $\overline{i_g^2}$ and its correlation with the channel noise $\overline{i_g i_d^*}$ are obtained by integrating $\Delta i_g(x)\Delta i_g(x)^*$ and $\Delta i_g(x)\Delta i_d(x)^*$ over region I only.

- No induced gate noise generated from the velocity saturation region because $\Delta i_d(x_o) = 0$ in region II.
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Choosing Device Sizes - Channel L

- **Channel length of devices reduced** => (1) $g_m$ increased (2) the peak value of $g_m$ happens at lower $V_{GS}$ value.

- The faster increase in $g_m$ makes (1) the $NF_{min}$ reduced and (2) the lowest $NF_{min}$ shifted to the lower $V_{GS}$ region.
Choosing DC Bias Conditions

- Higher $V_{DS}$ bias will increase $g_m$ at the higher $V_{GS}$ region.
- Higher $g_m$ will decrease $NF_{min}$ at higher $V_{GS}$ region.
- Decreased $NF_{min}$ at higher $V_{GS}$ region makes the lowest $NF_{min}$ less sensitive to $V_{GS}$ bias.
Device Geometry and Layout

\[ R_G = \left( \frac{1}{3} \right) R_{gsh} \times \frac{W}{L} \]

\[ R_G = \frac{1}{3} \times R_{gsh} \times \frac{W}{L} \times \frac{1}{2} = \frac{1}{3} \times 4 \times R_{gsh} \times \frac{W}{L} \]

\[ R_G = \frac{1}{3} \times R_{gsh} \times \frac{W/2}{L} \times \frac{1}{2} = \frac{1}{3} \times \frac{1}{4} \times R_{gsh} \times \frac{W}{L} \]

Two resistors connected in parallel
Each signal travels half of the distance \( W \)

\[ R_G = \frac{1}{3} \times R_{gsh} \times \frac{W/2}{L} \times \frac{1}{2} = \frac{1}{3} \times \frac{1}{4} \times R_{gsh} \times \frac{W}{L} \]

\[ n \] transistors
(width = \( W/n \))
Connected in parallel

\[ R_G = \frac{1}{3} \times R_{gsh} \times \frac{W}{n} \times \frac{1}{n} = \frac{R_{gsh} \cdot W}{3n^2 L} \]
Two-Port Network of LNAs

- Design considerations: Stability, Power Gain, Noise Figure (NF) and Linearity (IP3)
Schematic Diagram of an LNA

- **M1**: minimize noise; **M2**: maximize gain.

DC Bias & AC Open

- $L_d=7$ nH
- $L_g=8.3$ nH
- $L_s=2$ nH
- $R_b=10$ KΩ
- $C_c=40$ pF
- $L=0.3$ µm, $W=120$ µm, $I_{ds}=3$ mA
Impact of the Noise Sources

- Impact of the noise sources: (1) optimal frequency (2) $\Delta NF$ predicted

![Impact of the Noise Sources](image-url)
The peak $|S_{21}|$ and the lowest $NF$ don't happen at the same frequency.
Conclusions

- Substrate network => output matching network
- Parasitic capacitances => power & noise matching
- NQS effects => longer channel devices
- Channel noise modeling: CLM effect
- Induced gate noise modeling: $C_{GS}$ modeling
- LNA Design:
  - Channel length selection => noise budget
  - $V_{GS}$ bias => before peak $g_m$
  - $V_{DS}$ bias => sensitivity of $V_{GS}$ bias
  - Geometry => multi-finger with dual inputs