Analytical Modeling of MOSFETs Channel Noise and Noise Parameters

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***Abstract*—Simple analytical expressions for MOSFETs noise parameters are developed and experimentally verified. The expressions are based on analytical modeling of MOSFETs channel noise, are explicit functions of MOSFETs geometry and biasing conditions, and hence are useful for circuit design purposes. Good agreement between calculated and measured data is demonstrated. Moreover, it is shown that including induced gate noise in the modeling of MOSFETs noise parameters causes $\sim 5\,\%$ improvement in the accuracy of the simple expressions presented here, but at the expense of complicating the expressions.**

***Index Terms*—Analytical noise modeling, channel noise, induced gate noise, MOSFET noise, noise parameters.**

I. Introduction

CMOS TECHNOLOGY is being extensively used in analog and RF applications [1] because of the improved RF performance characteristics of downscaled MOS devices. To help circuit designers cope with the increasingly important issue of noise in devices and circuits, especially in short-channel MOSFETs, several MOSFET noise models have been developed in recent years [2]–[6]. The main focus of these models is the channel thermal noise of MOSFETs, since it is the dominant noise source in the device. However, these noise models are either physically questionable [7], or lack the ability to show the explicit dependence of MOSFETs noise on its terminal voltages and current in a simple form, hence making them not easy to use for circuit designers.

The goal of this paper is to develop simple MOSFET noise models that are suitable for circuit design purposes. In the second section of this paper, a simple, accurate analytical channel noise model for MOSFETs is developed. This model is based on the drain current model in [8] and is only a function of the MOSFETs geometry and biasing conditions. However, channel noise model per se is not enough for circuit design purposes. Therefore, in the third section of the paper, our model is used to develop simple analytical expressions for MOSFETs noise parameters, i.e., minimum noise figure, noise resistance, and optimum source admittance that are used by circuit designers to estimate the noise performance of MOS devices and circuits. To the best of the authors' knowledge, these are the first analytical expressions that explicitly show the effect of MOSFETs geometry and biasing on its noise performance in a simple form. Experimental verification of the models developed here is presented in Section IV. The effect of downscaling of MOSFETs channel length on its noise performance is discussed in the last section of the paper.

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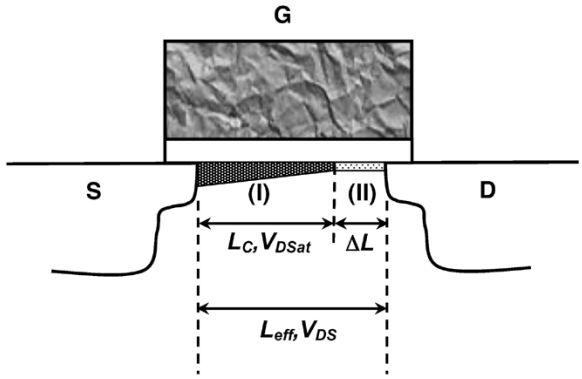

Fig. 1. Cross section of the channel of a MOSFET, divided into two regions: (I) gradual and (II) velocity saturation regions. L_C is the point in the channel where the channel field $E(x)$ is equal to the critical field E_C and the velocity of carriers is equal to their saturation velocity $v_{\rm sat}$.

II. Analytical Modeling of MOSFET Channel Noise

We start modeling the channel noise by dividing the channel into two sections: the linear and the velocity saturation regions (see Fig. 1). It is assumed that most of the drain current noise of the MOSFET is generated in the linear region, and the noise of the velocity saturation region is negligible. This is because of the fact that in this region, carriers travel at their saturation velocity and therefore they do not respond to the electric field fluctuations caused by the voltage fluctuation in the channel [6].

The MOSFETs drain current in strong inversion is dominated by the drift current and can be expressed at any point x in the channel as

$$I = -WQ(x)v(x) \tag{1}$$

where W is the width of the device, $Q(x)$ is the channel charge per unit area and $v(x)$ is the velocity of carriers in the channel. Although, in this paper, all of the equations are developed for n-channel devices, the same approach also applies for p-channel devices.

According to the BSIM model [8], the channel charge per unit area can be expressed as a function of the position in the channel x as

$$Q(x) = -C_{\rm ox}(V_{\rm GT} - \alpha V(x)), \tag{2}$$

where $C_{\rm ox}$ is gate capacitance per unit area, $V_{\rm GT} = V_{\rm GS} - V_{\rm th}$, and $V_{\rm th}$ is the threshold voltage, α is the bulk-charge effect coefficient (in this work, $\alpha = 1.2$ from (4) in [8]) and $V(x)$ is the source referenced quasi-Fermi potential that varies along the channel from 0 at the source side to $V_{\rm DS}$ at the drain side. The carrier velocity is given by a piecewise model [9] as

$$v(x) = \begin{cases} \dfrac{\mu_{\rm eff} E(x)}{1 + \frac{E(x)}{EC}} & E(x) < E_C \\ v_{\rm sat} & E(x) \geq E_C \end{cases} \tag{3}$$

where $E(x)$ is the longitudinal electric field along the channel, E_C is the critical field and equal to $2v_{\rm sat}/\mu_{\rm eff}$, $v_{\rm sat}$ is the saturation velocity of carriers and $\mu_{\rm eff}$ is the effective mobility that is only a function of the gate voltage. Substituting (2) and (3) in (1), one obtains in the linear region of the channel

$$I = \mu_{\rm eff} {\rm WC_{ox}} (V_{\rm GT} - \alpha V(x)) \frac{E(x)}{1 + \frac{E(x)}{E_C}}. \tag{4}$$

As the drain voltage of the device is increased, the longitudinal field increases gradually along the channel until it reaches to the critical field somewhere near the drain. This situation is depicted in Fig. 1. The point in the channel where $E = E_C$ is denoted as L_C, and V_C is the corresponding channel potential. Substituting $E(x) = dV(x)/dx$ in (4) yields

$$I = \mu_{\rm eff} {\rm WC_{ox}} (V_{\rm GT} - \alpha V(x)) \frac{\frac{dV(x)}{dx}}{1 + \frac{dV(x)}{E_C dx}}. \tag{5}$$

Integrating the above equation from 0 to x and solving for $V(x)$, one has

$$V(x) = \frac{1}{2\alpha} \times \left[(2V_{\rm GT} - V_0) - ((2V_{\rm GT} - V_0)^2 - 4\alpha E_C V_0 x)^{\frac{1}{2}} \right] \tag{6}$$

where $V_0 = I/({\rm WC_{ox}} v_{\rm sat})$. Using (6), $E(x)$ in the linear part of the channel is obtained as

$$E(x) = \frac{E_C V_0}{[(2V_{\rm GT} - V_0)^2 - 4\alpha E_C V_0 x]^{\frac{1}{2}}}. \tag{7}$$

Since the longitudinal electric field is continuous along the channel L_C can be obtained by equating $E(x)$ to E_C as

$$L_C = \frac{V_{\rm GT}(V_{\rm GT} - V_0)}{\alpha E_C V_0}. \tag{8}$$

It is assumed that at any point in the channel beyond L_C, carriers travel at their saturation velocity.

To calculate the drain current noise, the linear part of the channel is divided into small sections of length dx. Each section acts as a resistor of value dR, which can be obtained from (5) as

$$dR = \frac{dV}{I} = \frac{-dx}{\mu_{\rm eff} WQ(x) + \frac{I}{E_C}}. \tag{9}$$

The current noise $\overline{\Delta i^2(x)}$ generated from a small section of the channel located at x is the product of the square of the local conductance $g_{\rm DS}(x)$ and the voltage noise generated from each section $\overline{\Delta v^2(x)}$ [10]. Therefore

$$\overline{\Delta i^2(x)} = g_{\rm DS}^2(x) \overline{\Delta v^2(x)} = 4kT g_{\rm DS}^2(x) dR \Delta f. \tag{10}$$

The local conductance can be expressed in terms of the device parameters as [6]

$$g_{\rm DS}(x) = \frac{\mu_{\rm eff} {\rm WC_{ox}} (V_{\rm GT} - \alpha V(x))}{L_{\rm eff}} \cdot \frac{1}{\left(1 + \frac{E(x)}{E_C}\right)}. \tag{11}$$

The spectral density of the drain current noise, S_{iD}, is the sum of the drain current noise generated from each section. Therefore, one can write [11]

$$S_{iD} = 4kT \int_0^{L_C} g_{\rm DS}^2(x)\, dR. \tag{12}$$

Substituting for dR and $g_{\rm DS}$ and from (9) and (11), and using (7), the drain current noise spectral density of the device is obtained as

$$S_{iD} = 4kT \frac{4V_{\rm GT}^2 + V_0^2 - 2V_0 V_{\rm GT}}{3V_{\rm GT}^2 (V_{\rm GT} - V_0)} \alpha I. \tag{13}$$

It can be observed that the model presented in (13) is analytical and takes into account mobility degradation due to the channel electric field. Moreover, (13) is an explicit function of the device geometry and biasing conditions.

From (4), it is seen that at the point along the channel where the carrier velocity is saturated, i.e., $v(x) = v_{\rm sat}$, the drain current, I, is equal to $I = {\rm WC_{ox}}(V_{\rm GT} - \alpha V_{D\,\rm sat}) v_{\rm sat}$ [8]. Therefore, $V_0 = V_{\rm GT} - \alpha V_{D\,\rm Sat}$, where V_0 is defined after (6). Consequently, (13) can be simplified as

$$S_{iD} = 4kTI \left[\frac{1}{V_{D\,\rm sat}} + \frac{\alpha^2 V_{D\,\rm sat}}{3V_{\rm GT}^2} \right] = 4kTI\beta. \tag{14}$$

where $\beta = [1/V_{D\,\rm sat} + \alpha^2 V_{D\,\rm sat}/(3V_{\rm GT}^2)]$. Equation (14) is similar to the traditional channel noise expression, i.e., $S_{iD} = 4kT\gamma g_{d0}$ [12], where g_{d0} is the drain transconductance at $V_{\rm DS} = 0$ and γ is called the channel noise coefficient. In long-channel devices $g_{d0} = g_m$ and $\gamma = 2/3$. However, in the case of short-channel devices, both g_{d0} and γ are complicated functions of the device parameters [13]. Therefore, although (14) looks similar to the traditional channel noise expression, it is much simpler in the case of short-channel devices. In the following section, the channel noise model developed here will be used to develop analytical expressions for MOSFETs noise parameters, i.e., minimum noise figure, noise resistance, and optimum source admittance.

III. Modeling of MOSFET's Noise Parameters

A. Noise Parameters of a Two-Port Network

The minimum noise figure ${\rm NF_{min}}$, noise resistance R_n, and optimum source admittance $Y_{\rm opt}$, of a two-port network in terms of its noise correlation matrix entries C_{11}, C_{12}, C_{21}, and C_{22} are given by (15)–(17) from [14]. The matrix entries are given by (18)–(20) as functions of the input referred noise voltage, v_n^2,

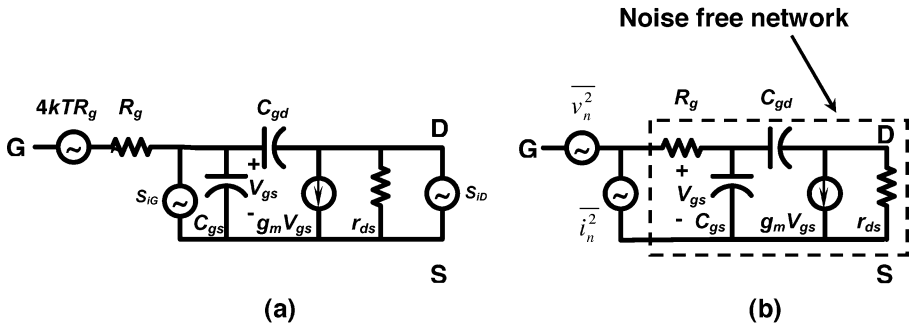

Fig. 2. (a) Equivalent compact circuit model of MOSFET with thermal noise sources, where S_{iD} and S_{iG} are drain current and induced gate noise and (b) the noise free MOSFET compact circuit model with input referred noise voltage and current.

and noise current, i_n^2, of the network as well as Y parameters of the noise free two-port network [14], [15] shown in Fig. 2(b)

$$R_n = C_{11} \tag{15}$$

$$Y_{\rm opt} = G_{\rm opt} + jB_{\rm opt} = \left[\frac{C_{22}}{C_{11}} - \left(\frac{{\rm Im}\{C_{12}\}}{C_{11}}\right)^2\right]^{\frac{1}{2}} + j\frac{{\rm Im}\{C_{12}\}}{C_{11}} \tag{16}$$

$${\rm NF}_{\rm min} = 1 + 2({\rm Re}\{C_{12}\} + C_{11}G_{\rm opt}) \tag{17}$$

$$C_{11} = \frac{\overline{v_n^2}}{4kT\Delta f} = \frac{S_{iD}}{4kT|Y_{21}|^2} + R_g + n\cdot\frac{S_{iG}}{4kT}R_g^2 \tag{18}$$

$$C_{21} = C_{12}^* = \frac{\overline{v_n^* i_n}}{4kT\Delta f} = \frac{Y_{11}\cdot S_{iD}}{4kT|Y_{21}|^2} + n\cdot\frac{S_{iG}}{4kT}R_g \tag{19}$$

$$C_{22} = \frac{\overline{i_n^2}}{4kT\Delta f} = \frac{|Y_{11}|^2\cdot S_{iD}}{4kT|Y_{21}|^2} + n\cdot\frac{S_{iG}}{4kT}. \tag{20}$$

Here, S_{iG} is the power spectral density of the induced gate noise of MOSFET and is equal to $S_{iG} = 4kT\eta(\omega C_{\rm gs})^2/g_m$, where η is called the induced gate noise coefficient [16], and n is either 0 or 1, corresponding to neglecting or including the induced gate noise, respectively (the correlation between the drain noise and induced gate noise is neglected). It should be noted that in developing (25)–(28), $n = 0$ is chosen to keep the simplicity of the models. However, it will be shown in Section IV of this paper that the error caused by neglecting S_{iG} not significant.

It is also noted that R_g is the effective gate resistance of MOSFET and is extracted based on the equivalent circuit model of Fig. 2 and (21) and (22). Moreover, R_g can be expressed in terms of the sheet resistance and geometry of the device as $R_g = \kappa R_{\rm gsh}W_f/(3L_fN_f)$, where $R_{\rm gsh}, W_f, L_f$, and N_f are the sheet resistance of the gate material, the width of the device, the channel length of the device and the number of fingers, respectively. κ is either 1 or $1/4$ representing the device with one-sided or double-sided gate contacts, respectively, and factor three accounts for the distributed nature of the gate region [16].

B. Analytical Expressions of MOSFETs Noise Parameters

The Y parameters of the noise-free MOSFET can be obtained from the simple compact circuit model, shown in Fig. 2(b), as

$$Y_{11} = \frac{sC_{\rm gg}}{1 + sC_{\rm gg}R_g} \tag{21}$$

$$Y_{12} = \frac{-sC_{\rm gd}}{1 + sC_{\rm gg}R_g} \tag{22}$$

$$Y_{21} = \frac{g_m - sC_{\rm gd}}{1 + sC_{\rm gg}R_g} \tag{23}$$

$$Y_{22} = \frac{1}{r_{\rm ds}} + sC_{\rm gd} + \frac{[g_m - sC_{\rm gg}]sC_{\rm gd}R_g}{1 + sC_{\rm gg}R_g} \tag{24}$$

where $s = j\omega, C_{\rm gg} = C_{\rm gs} + C_{\rm gd}$. Using (14)–(24) and $n = 0$, MOSFETs noise parameters can be expressed as

$$R_n = R_g + \frac{\beta I}{|Y_{21}|^2} \approx R_g + \frac{\beta I}{g_m^2} \tag{25}$$

$$G_{\rm opt} = \frac{|Y_{11}||Y_{21}|\sqrt{\beta IR_g}}{\beta I + R_g|Y_{21}|^2} \approx \left(\frac{f}{f_T}\right)\frac{\sqrt{\beta IR_g}}{R_n} \tag{26}$$

$$B_{\rm opt} = \frac{-\omega C_{\rm gg}\beta I}{\beta I + R_g|Y_{21}|^2} \approx -\left(\frac{f}{f_T}\right)\frac{\beta I}{g_m R_n} \tag{27}$$

$${\rm NF}_{\rm min} \approx 1 + 2\left(\frac{f}{f_T}\right)\sqrt{\beta IR_g}\left(1 + \left(\frac{f}{f_T}\right)\sqrt{\beta IR_g}\right). \tag{28}$$

Here f is the frequency of operation, $f_T = g_m/(2\pi C_{\rm gg})$ the drain current unity gain frequency, and β is defined in (14).

To derive (25)–(28), it is assumed that $(\omega C_{\rm gg}R_g)^2 \ll 1$, which is a reasonable assumption up to frequencies $\sim$10 GHz for MOSFETs in a typical 0.18-μm technology. Equations (25)–(28) explicitly show the relationship between the MOSFETs noise parameters and its biasing conditions, i.e., voltages and current, and they contain no empirical parameter. Moreover, the simplicity of these equations makes them suitable for circuit design purposes, with I, R_g, and g_m as design parameters. It can be found from these expressions that to minimize the noise R_g should be minimized and the drain current I has to be chosen where g_m is maximum. Experimental verification of the channel noise and MOSFETs noise parameters models is presented in the next section.

IV. Experimental Results

In this section, we first verify our channel thermal noise model, i.e., (14), using noise measurement results of MOSFETs with three different channel lengths. Second, MOSFET noise parameters obtained from (25)–(28) will be compared with measured noise parameters as well as calculated noise parameters using (15)–(20) with inclusion of $S_{iG} = 4kT\eta(\omega C_{\rm gs})^2/g_m$, i.e., $n = 1$ in (18)–(20), at different bias points.

Fig. 3 shows the simulated and measured channel noise of MOSFETs with $W = 6 \times 10$ μm, and $L = 0.97, 0.42$, and 0.18 μm, versus gate to source voltage $V_{\rm GS}$. It is found that our

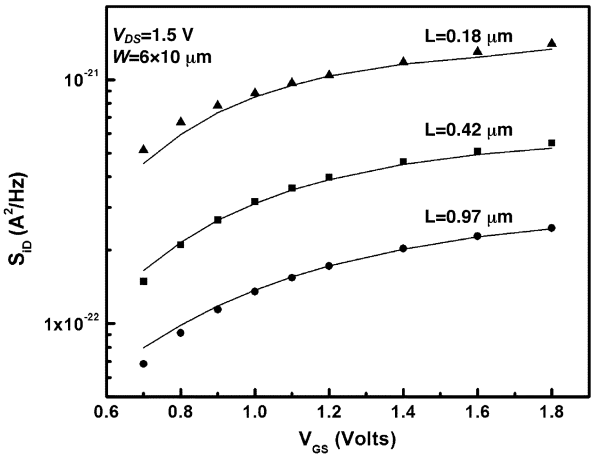

Fig. 3. Channel thermal noise of MOSFETs with different channel lengths versus $V_{\rm GS}$. Symbols and lines are measured and simulated data, respectively.

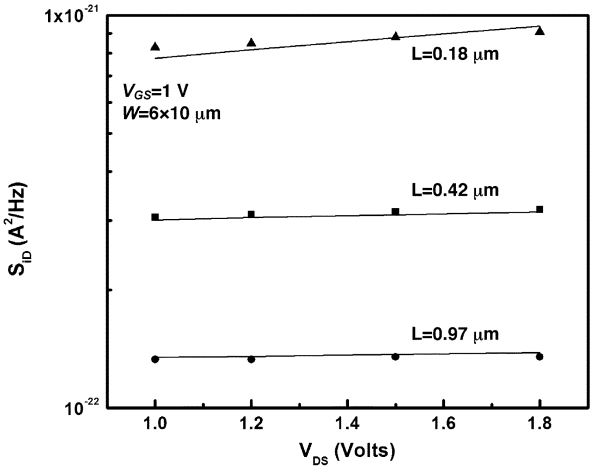

Fig. 4. Channel thermal noise of MOSFETs with different channel lengths versus $V_{\rm DS}$. Symbols and lines are measured and simulated data, respectively.

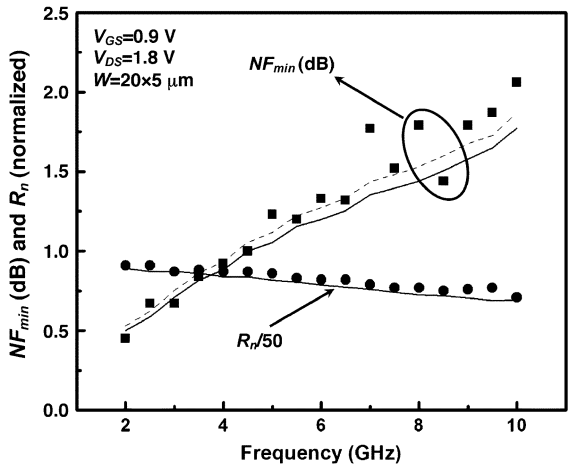

Fig. 5. Minimum noise figure $\rm NF_{min}$ (in decibels) and noise resistance R_n versus frequency at $V_{\rm GS} = 0.9$ V, and $V_{\rm DS} = 1.8$ V. R_n is normalized by 50 Ω.

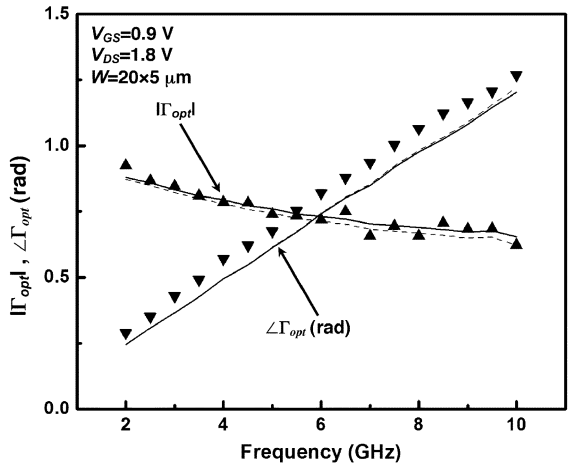

Fig. 6. Magnitude and phase of the optimum source reflection coefficient $\Gamma_{\rm opt}$ versus frequency at $V_{\rm GS} = 0.9$ V, and $V_{\rm DS} = 1.8$ V.

model, i.e., (14), is able to predict the channel thermal noise of these devices with less than ∼10% error. The channel noise dependence on drain to source voltage, $V_{\rm DS}$, is depicted in Fig. 4. Once again our model matches the measured data with ∼10% error.

The comparison between simulated and measured MOSFETs noise parameters at $V_{\rm GS} = 0.9, 1.2$, and 1.5 V, at $V_{\rm DS} = 1.8$ V versus frequency is demonstrated in Figs. 5–10. In this case, the device under test is a MOSFET with $W = 20 \times 5$ μm, and $L = 0.18$ μm. Note that the elements of the compact circuit model of MOSFET, shown in Fig. 2, are extracted using measured Y parameter values and (21)–(24). Also, $\Gamma_{\rm opt} = (Z_{\rm opt} - Z_0)/(Z_{\rm opt} + Z_0)$, where $Z_{\rm opt} = 1/Y_{\rm opt}$, is the optimum source reflection coefficient and $\rm NF_{min}$ is the minimum noise figure given in decibels. In Figs. 5–10, the symbols are measured data, the solid lines are noise parameters from (25)–(28) and the dashed lines are values obtained from (15)–(20) with $n = 1$, respectively. The coefficient η, in S_{iG} expression above, is chosen to be $\eta = 0.1$, to give the best fit between calculated and measured data.

It is observed that (28) can be used to estimate the value of $\rm NF_{min}$ with an average discrepancy of ∼10% at all three $V_{\rm GS}$ points. The increase of $\rm NF_{min}$ and its trend as a function of frequency, which is shown in Figs. 5, 7, and 9, is evident from (28), as the only parameter on the right hand side of this equation that is a function of f is the frequency itself. In addition, as it can be found from the Figs. 5, 7, and 9, higher $V_{\rm GS}$ results in higher $\rm NF_{min}$ at a specific frequency, which is also predicted by (28). The reason is that the effect of any increase in f_T, caused by higher $V_{\rm GS}$, is cancelled by a larger increase in the channel noise, i.e., larger βI [see (28)]. Moreover, it is found that the relative error between modeled and measured values of $|\Gamma_{\rm opt}|$, $\angle\Gamma_{\rm opt}$ and R_n is ∼10%. The slight decrease in noise resistance versus frequency is due to the slight increase in the value of $|Y_{21}|^2$ as the frequency increases, as expected from (23) with $s = j\omega$. It should also be noted that R_g plays a crucial role in MOSFET noise modeling and cannot be neglected, as shown explicitly in (25), (26), and (28) and in (27) through R_n.

Moreover, Figs. 5 to 10 show that taking into account the induced gate noise, S_{iG}, in our modeling procedure has a negligible effect on the accuracy of our models with a maximum improvement of around 5% in estimating $\rm NF_{min}$ at $f = 10$ GHz. The effect of S_{iG} on R_n is so small that it cannot be seen in the

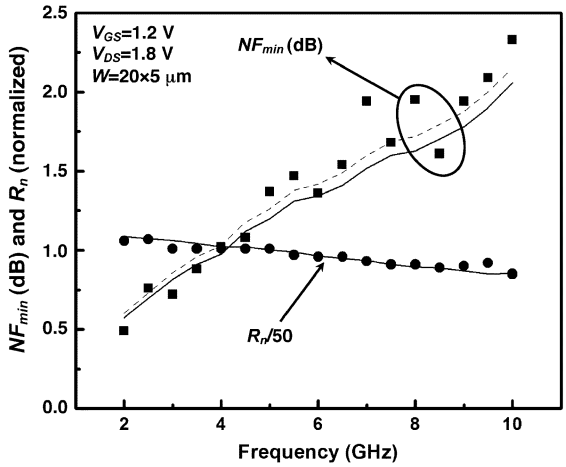

Fig. 7. Minimum noise figure, $\mathrm{NF}_{\min}$ (in decibels), and noise resistance R_n versus frequency at $V_{\mathrm{GS}} = 1.2$ V, and $V_{\mathrm{DS}} = 1.8$ V. R_n is normalized by 50 Ω.

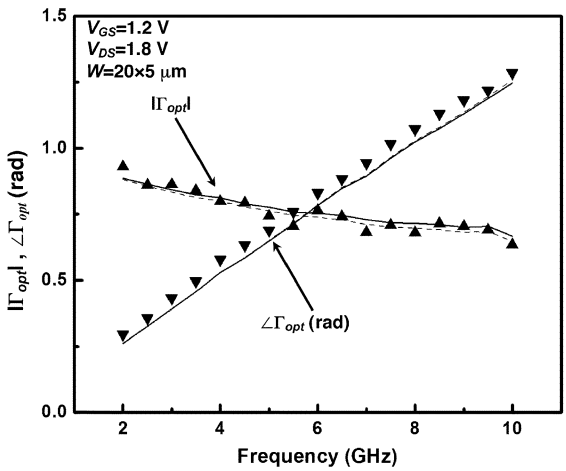

Fig. 8. Magnitude and phase of the optimum source reflection coefficient Γ_{opt} versus frequency at $V_{\mathrm{GS}} = 1.2$ V, and $V_{\mathrm{DS}} = 1.8$ V.

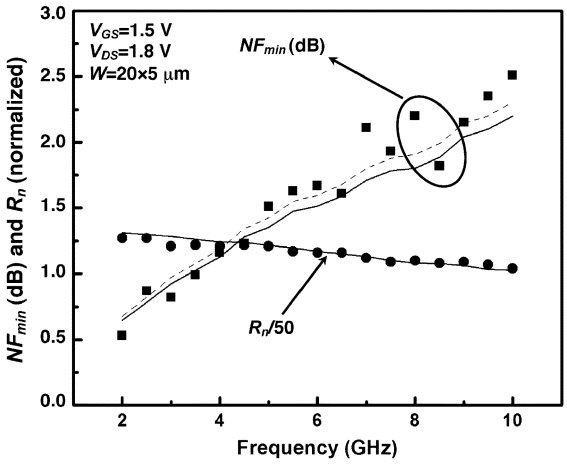

Fig. 9. Minimum noise figure, $\mathrm{NF}_{\min}$ (in decibels), and noise resistance R_n versus frequency at $V_{\mathrm{GS}} = 1.5$ V, and $V_{\mathrm{DS}} = 1.8$ V. R_n is normalized by 50 Ω.

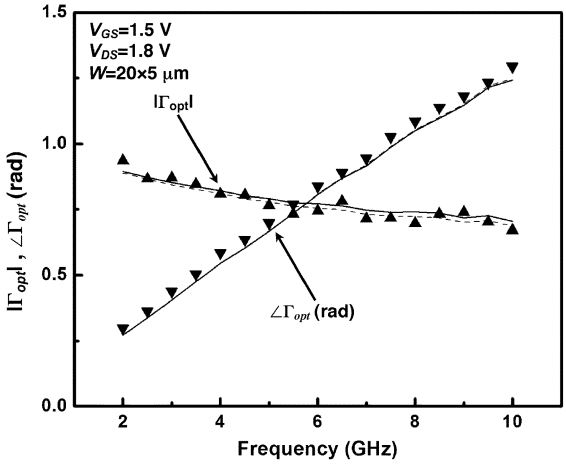

Fig. 10. Magnitude and phase of the optimum source reflection coefficient Γ_{opt} versus frequency at $V_{\mathrm{GS}} = 1.5$ V, and $V_{\mathrm{DS}} = 1.8$ V.

figures. Therefore, it seems reasonable to ignore the slight improvements, caused by including S_{iG} in (18)–(20), to keep the simplicity of (25)–(28).

V. Noise and Scaling

The issue of noise becomes more pronounced when the MOSFETs channel length becomes smaller [5], [6]. One of the advantages of having an analytical noise model, such as (14), is that one can explicitly observe how the reduction in channel length affects the noise performance of MOSFETs. Using $V_0 = V_{\mathrm{GT}} - \alpha V_{D\,\mathrm{Sat}}$, and (8), (14) reduces to

$$S_{iD} = 4kTWv_{\mathrm{sat}}V_{\mathrm{GT}}\left[\frac{1}{E_C L_C} + \frac{\alpha^2}{3}\frac{E_C L_C}{(\alpha E_C L_C + V_{\mathrm{GT}})^2}\right]. \tag{29}$$

It can be shown that for very short-channel devices, (29) can be further simplified to

$$S_{iD} = 4kT\mathrm{WC_{ox}}\mu_{\mathrm{eff}}\frac{V_{\mathrm{GT}}}{2} \times \frac{1}{L_C}. \tag{30}$$

Equation (30) explicitly shows a reciprocal dependence of the channel noise on MOSFETs channel length when it becomes very small. Using (29), the noise parameters of very short-channel MOSFETs are given by (31)–(34) as explicit functions of the channel length.

$$R_n = R_g + \frac{\mathrm{WC_{ox}}\mu_{\mathrm{eff}}}{2g_m^2} \times \frac{1}{L_C} \tag{31}$$

$$G_{\mathrm{opt}} \approx \left(\frac{f}{f_T}\right)\frac{\sqrt{\mathrm{WC_{ox}}\mu_{\mathrm{eff}}V_{\mathrm{GT}}R_g}}{\sqrt{2}R_n} \times \sqrt{\frac{1}{L_C}} \tag{32}$$

$$B_{\mathrm{opt}} \approx -\left(\frac{f}{f_T}\right)\frac{\mathrm{WC_{ox}}\mu_{\mathrm{eff}}V_{\mathrm{GT}}}{2g_m R_n} \times \frac{1}{L_C} \tag{33}$$

$$\mathrm{NF_{min}} \approx 1 + 2\left[\left(\frac{f}{f_T}\right)^2\frac{\mathrm{WC_{ox}}\mu_{\mathrm{eff}}V_{\mathrm{GT}}R_g}{2L_C} + \left(\frac{f}{f_T}\right)\sqrt{\frac{\mathrm{WC_{ox}}\mu_{\mathrm{eff}}V_{\mathrm{GT}}R_g}{2L_C}}\right]. \tag{34}$$

It can be observed that both R_n and $\mathrm{NF_{min}}$ decrease when channel length becomes smaller. However, in the case of extremely short-channel MOSFETs where $g_m \approx \mathrm{WC_{ox}}v_{\mathrm{sat}}$ [10],

R_n and $\mathrm{NF}_{\min}$ are, respectively, reciprocal and linear functions of the channel length.

VI. Conclusion

Analytical modeling of the MOSFET's channel noise was presented. In addition, simple closed form expressions for MOSFETs noise parameters were developed and verified. The expressions were explicit functions of MOSFET geometry and biasing conditions, hence making them useful for circuit design purposes and to be incorporated in simulators such as SPICE. Moreover, it was demonstrated that the effect of induced gate noise on the accuracy of our noise models was negligible.

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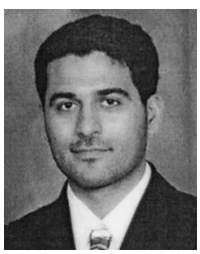

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