

## Lecture #14

### from Chapter 4 in Jaeger, Chapter 2 in Spencer Field Effect Transistors

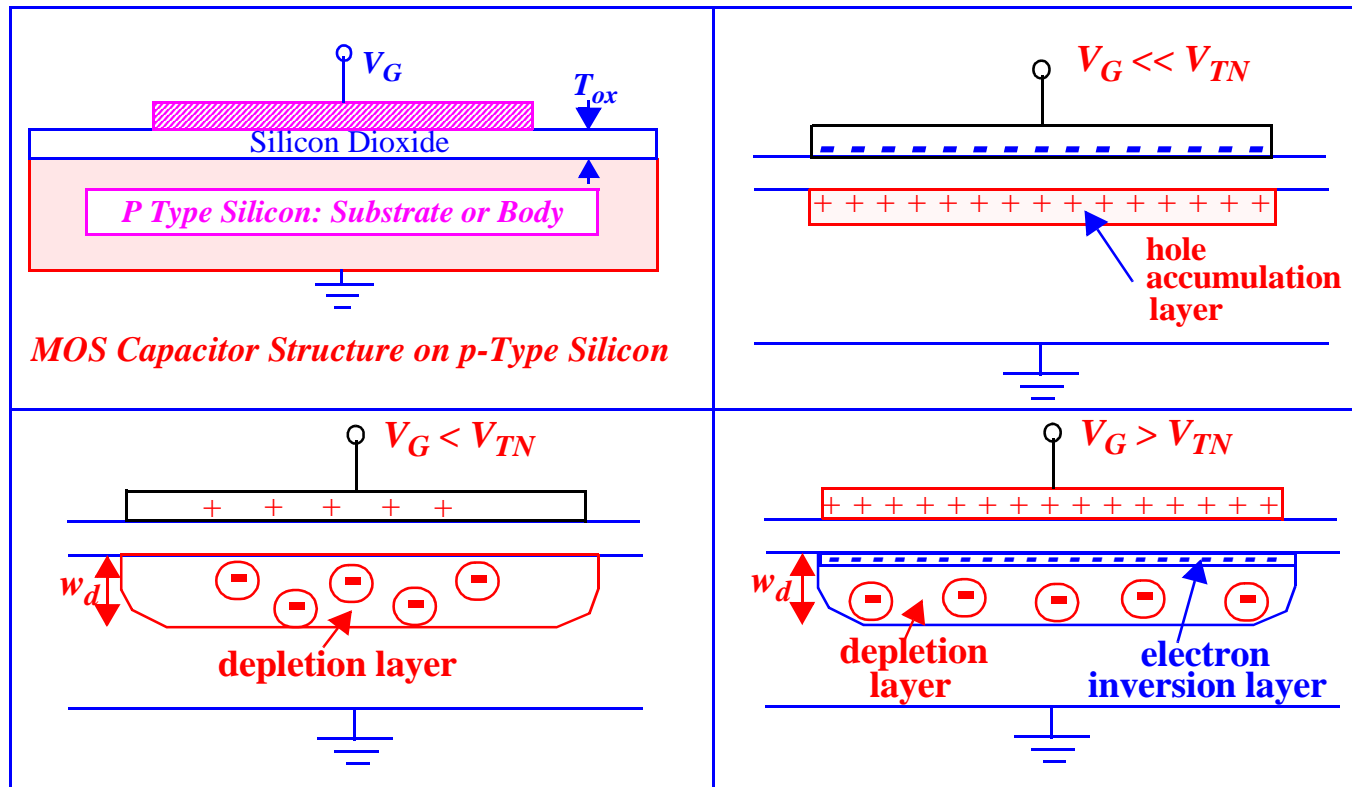
#### **Outline/Learning Objectives:**

- Describe/understand the physical structure of the MOS transistor (MOSFET).
- Identify the NMOS and PMOS transistor circuit diagram symbols.
- Describe qualitatively and quantitatively the physical operating principles of the MOSFET.
- Explain the characteristics (output and transfer) of the MOSFET.
- Determine the operating regions (cutoff, linear & saturation) of the MOSFET.
- Determine the mathematical (square-law) model parameters from given data.
- Solve simple MOSFET dc circuits using the mathematical model.
- Solve simple MOSFET dc circuits using graphical analysis and the load-line concept.
- Solve simple MOSFET dc circuits using iterative numerical methods.
- Analyze and design simple MOSFET dc circuits.
- Define and describe the capacitances in MOS transistors.
- Use the capacitance models to solve simple device problems.
- Use the electronics laboratory to investigate the electrical behavior of simple circuits and devices.

#### **Selected problems:**

**4.9, 4.15, 4.27, 4.35, 4.41, 4.45, 4.51, 4.81, 4.82, 4.86, 4.102, 4.116, 4.118, 4.142**

## Characteristics of the MOS Capacitor



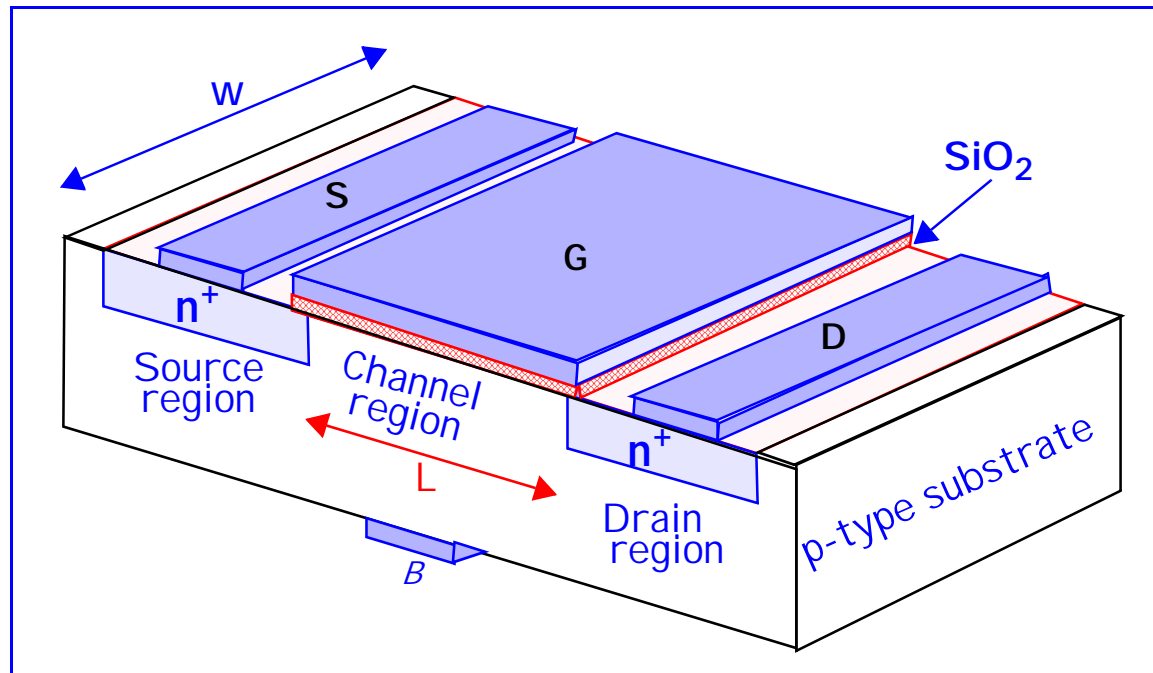
MOS Capacitor -

**Accumulation** - large negative biases on gate results in large number of holes at surface. That is, we have an accumulation of the substrate majority carriers at the surface. Here, the hole density exceeds that in the p-type substrate below. It is a shallow layer.

**Depletion** - gate voltage is made more positive, but less than threshold voltage. Have positive charges on gate which repels holes from the surface. The surface of the substrate becomes depleted. As the gate voltage increases, more holes are repelled to balance the increase of positive charges on gate, so the depletion layer increases.

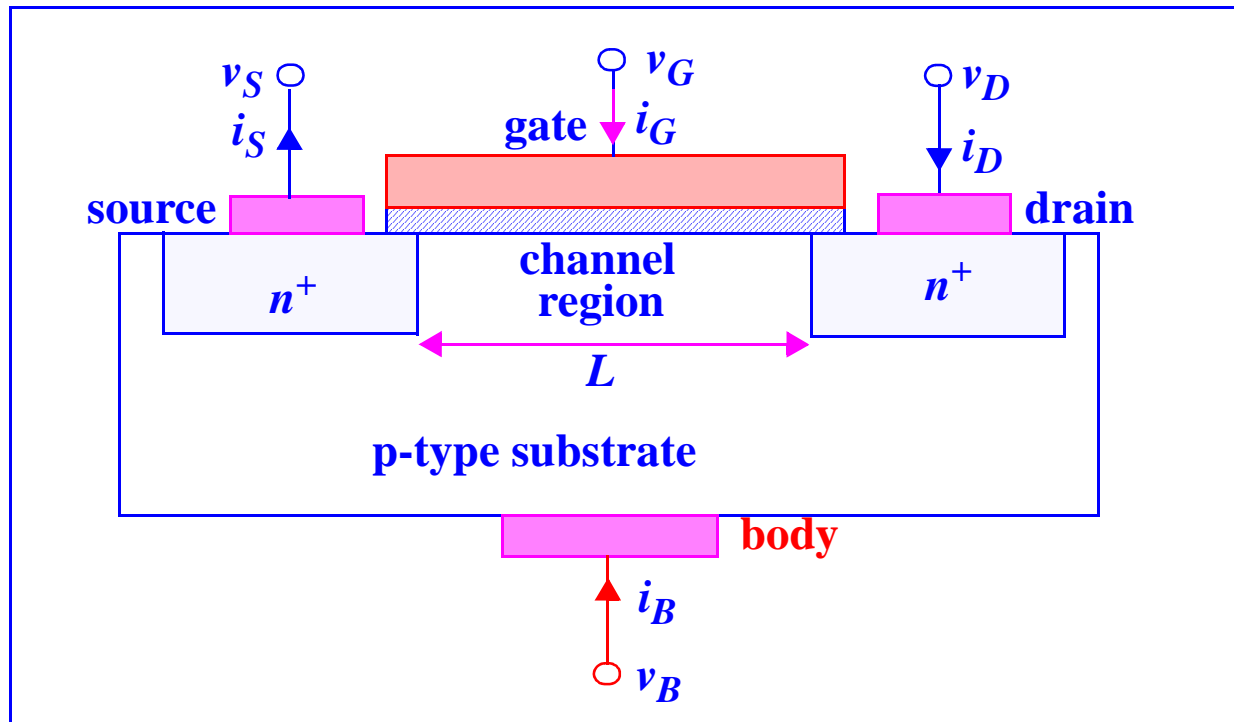
**Inversion** - as gate voltage increases, electrons are now attracted to the surface. When the electron density at surface exceeds the hole density of the substrate, inversion has occurred. Now we have an inversion layer directly at the surface of the substrate below the oxide layer. The voltage at which the inversion layer forms is called the **threshold voltage  $V_{TN}$** .

## Structure of the MOS Transistor

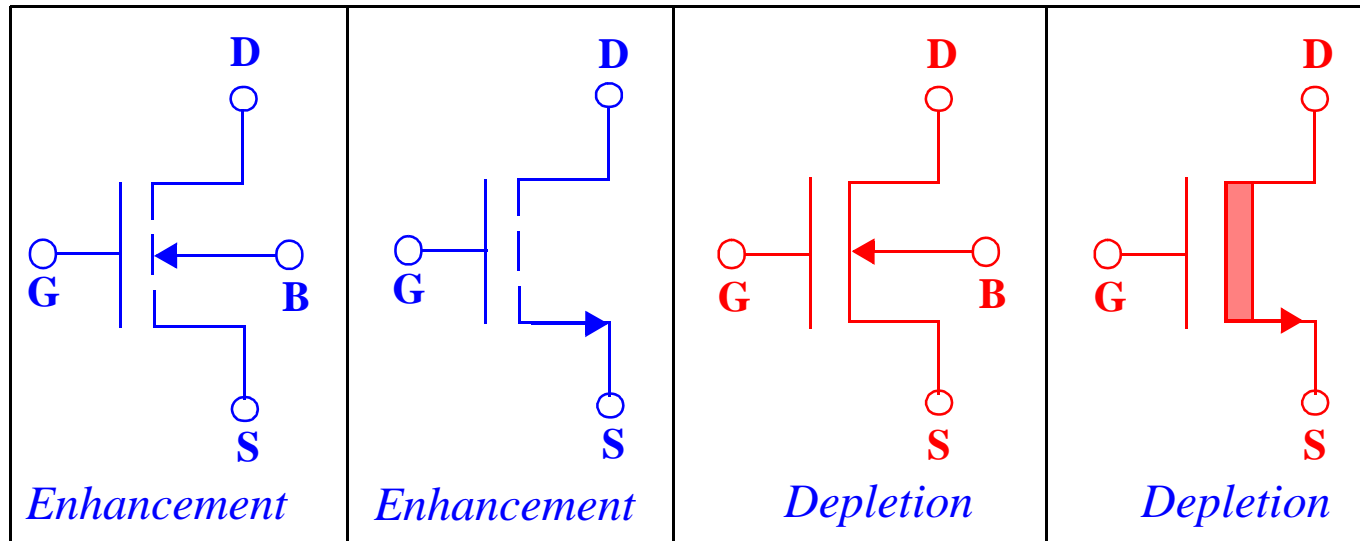


- Explain
- threshold voltage
  - purpose of source and drain
  - function of gate oxide and gate electrode/material
  - aspect ratio ( $W/L$ )
  - 4 terminal structure

# Cross-Section of the MOS Transistor



## Symbol of the n-channel MOS Transistor or NMOSFET



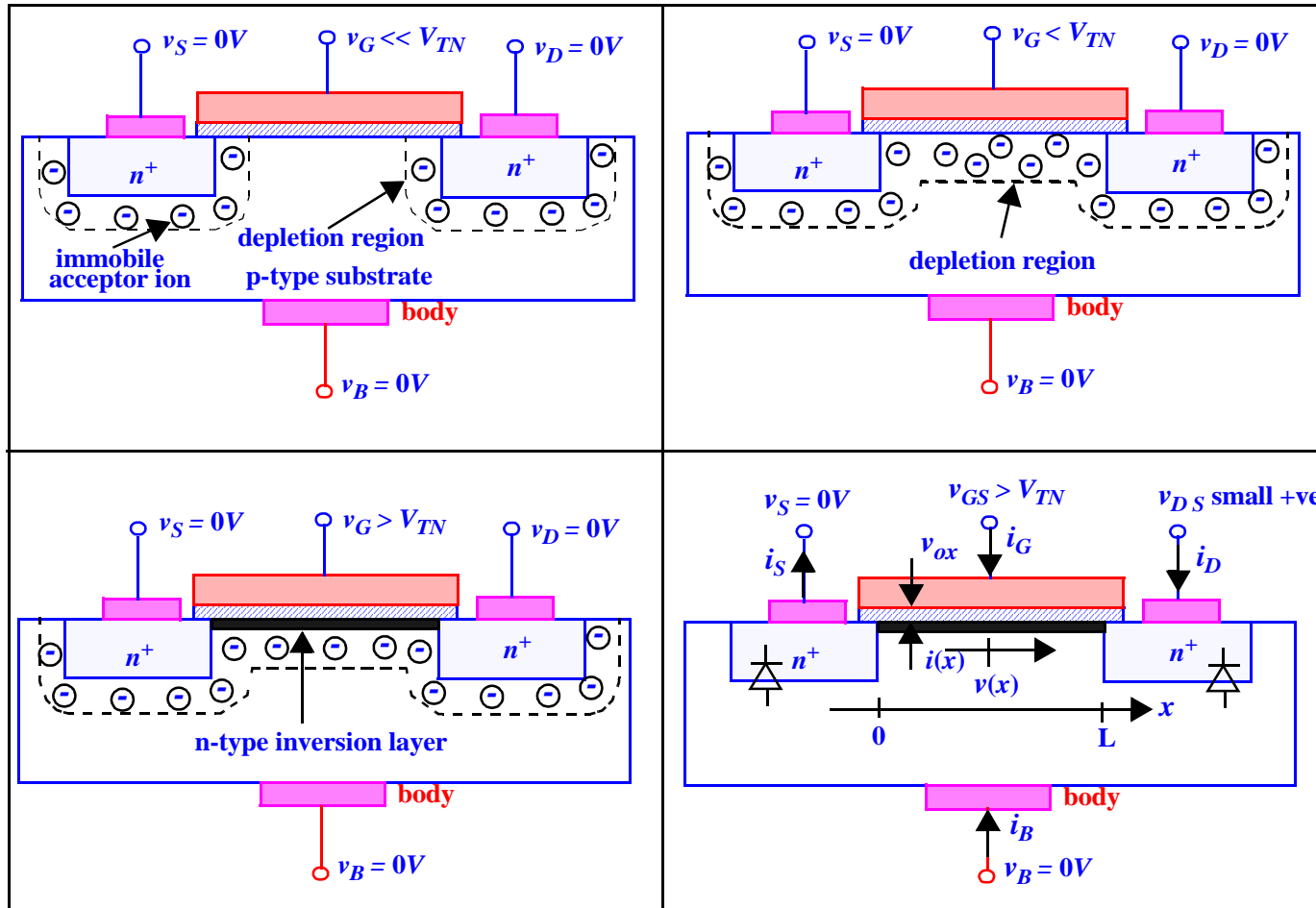
Explain qualitatively how the MOSFET works.

Drain-substrate and source-substrate  $n^+$ -p junctions.

Enhancement mode device.

Depletion mode device.

# Linear Region Characteristics



See appendix for detailed derivations of the following equations.

$$i_{DS} = \mu_n C_{ox} \frac{W}{L} \left( v_{GS} - V_{TN} - \frac{v_{DS}}{2} \right) v_{DS}$$

$$i_{DS} = K_n' \frac{W}{L} \left( v_{GS} - V_{TN} - \frac{v_{DS}}{2} \right) v_{DS} = K_n \left( v_{GS} - V_{TN} - \frac{v_{DS}}{2} \right) v_{DS}$$

$K_n'$  is the process transconductance parameter ( $A/V^2$ ), a **technology variable**.  $K_n$  is the transconductance parameter, a **design variable**.

$$v_{GS} - v(x) > V_{TN} \text{ for } 0 \leq x \leq L$$

For  $v_{GS} - V_{TN} > v_{DS}$  (linear region)

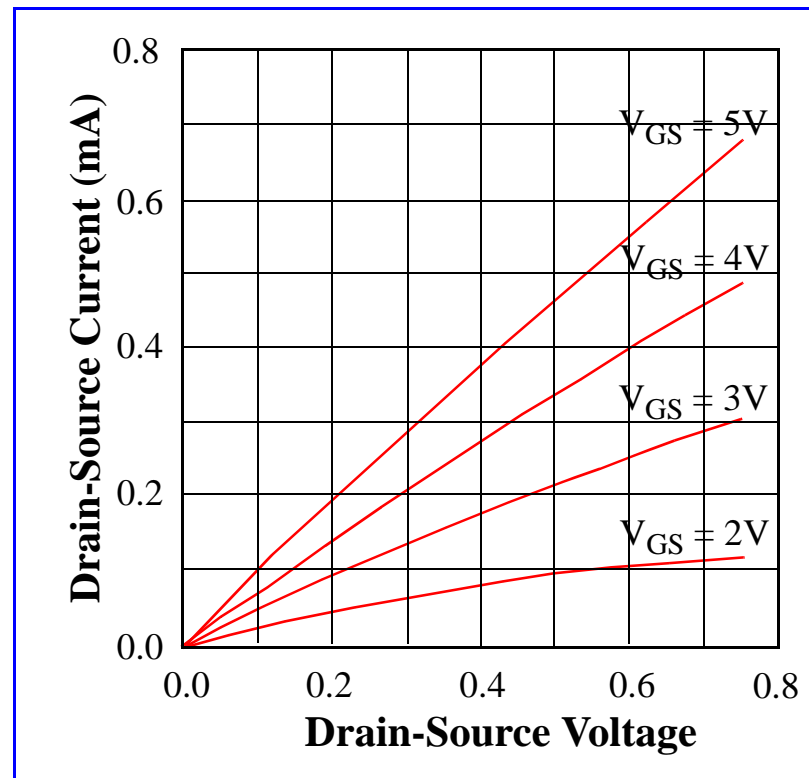
$$i_{DS} = C_{ox} W \left( v_{GS} - V_{TN} - \frac{v_{DS}}{2} \right) \left( \mu_n \frac{v_{DS}}{L} \right)$$

For  $v_{GS} - V_{TN} \gg v_{DS}$ , we have that

$$i_{DS} = \mu_n C_{ox} \frac{W}{L} (v_{GS} - V_{TN}) v_{DS}$$



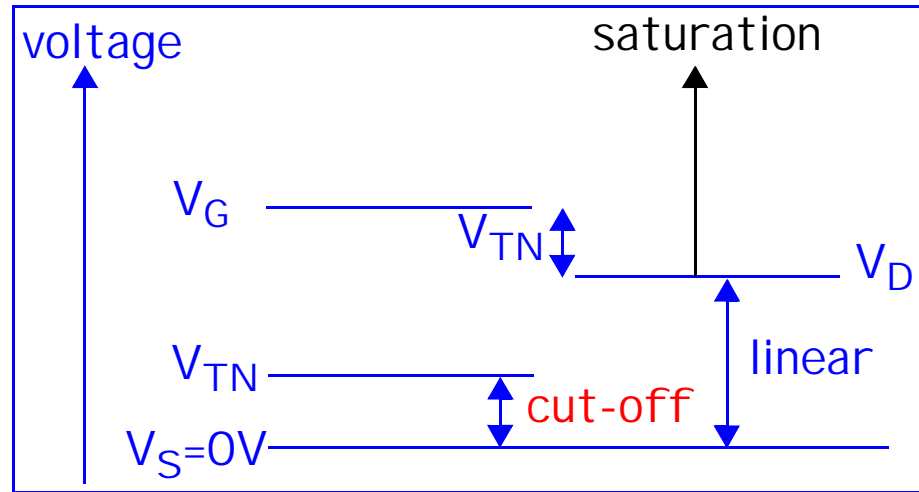
## I-V Characteristics of nMOSFET in Linear Mode



Output/On-resistance  $R_{on} = \left[ \frac{\partial i_{DS}}{\partial v_{DS}} \right]^{-1} \approx \frac{1}{K_n' \frac{W}{L} (v_{GS} - V_{TN})}$  in  $\Omega$

Transconductance  $g_m = \left[ \frac{\partial i_{DS}}{\partial v_{GS}} \right] \approx K_n' \frac{W}{L} v_{DS}$  in S or A/V

Explain in detail the significance of the output resistance and the transconductance.



Example: An NMOS transistor has a channel width  $W = 100\mu\text{m}$ , channel length  $L = 10\mu\text{m}$ ,  $V_{TN} = 1\text{V}$ ,  $K_n' = 20\frac{\mu\text{A}}{\text{V}^2}$  and operates at  $V_{DS} = 2\text{V}$ . If  $V_{GS} = 4\text{V}$ , find  $I_{DS}$ ,  $R_{on}$  and  $g_m$ .

Since  $4 - 1 > 2 \Rightarrow v_{GS} - V_{TN} > v_{DS}$ , operates in linear region.

$$\therefore i_{DS} = K_n' \frac{W}{L} \left( v_{GS} - V_{TN} - \frac{v_{DS}}{2} \right) v_{DS} = (20\mu) \left( \frac{100\mu}{10\mu} \right) \left( 4 - 1 - \frac{2}{2} \right) (2) = 0.8\text{mA}$$

$$R_{on} = \frac{1}{K_n' \frac{W}{L} (v_{GS} - V_{TN})} = \frac{1}{(20\mu) \left( \frac{100\mu}{10\mu} \right) (4 - 1)} = 1.67\text{k}\Omega$$

$$g_m = K_n' \frac{W}{L} v_{DS} = (20\mu) \left( \frac{100\mu}{10\mu} \right) (2) = 0.4\text{mS}$$

## Appendix

### Detailed derivations of the equations for Linear Region Characteristics.

$$i_D = i_S = i_{DS}$$

$$Q' = -WC_{ox}(v_{ox} - V_{TN}) \text{ in C/cm}$$

$$v_{ox} = v_{GS} - v(x) \text{ in V}$$

$$i(x) = Q'(x)v_x(x) \text{ in A}$$

$$i(x) = Q'v_x = -WC_{ox}(v_{ox} - V_{TN})(-\mu_n E_x)$$

$$E_x = -\frac{dv(x)}{dx} \text{ in V/cm}$$

$$i(x) = -\mu_n C_{ox} W (v_{GS} - v(x) - V_{TN}) \frac{dv(x)}{dx}$$

$$i(x)dx = -\mu_n C_{ox} W (v_{GS} - v(x) - V_{TN}) dv(x)$$

$$\int_0^L i(x) dx = -\int_0^{v_{DS}} \{ \mu_n C_{ox} W (v_{GS} - v(x) - V_{TN}) \} dv(x)$$

$$i_{DS} L = \mu_n C_{ox} W \left( v_{GS} - V_{TN} - \frac{v_{DS}}{2} \right) v_{DS}$$

$$i_{DS} = \mu_n C_{ox} \frac{W}{L} \left( v_{GS} - V_{TN} - \frac{v_{DS}}{2} \right) v_{DS}$$

$$i_{DS} = K_n' \frac{W}{L} \left( v_{GS} - V_{TN} - \frac{v_{DS}}{2} \right) v_{DS} = K_n \left( v_{GS} - V_{TN} - \frac{v_{DS}}{2} \right) v_{DS}$$