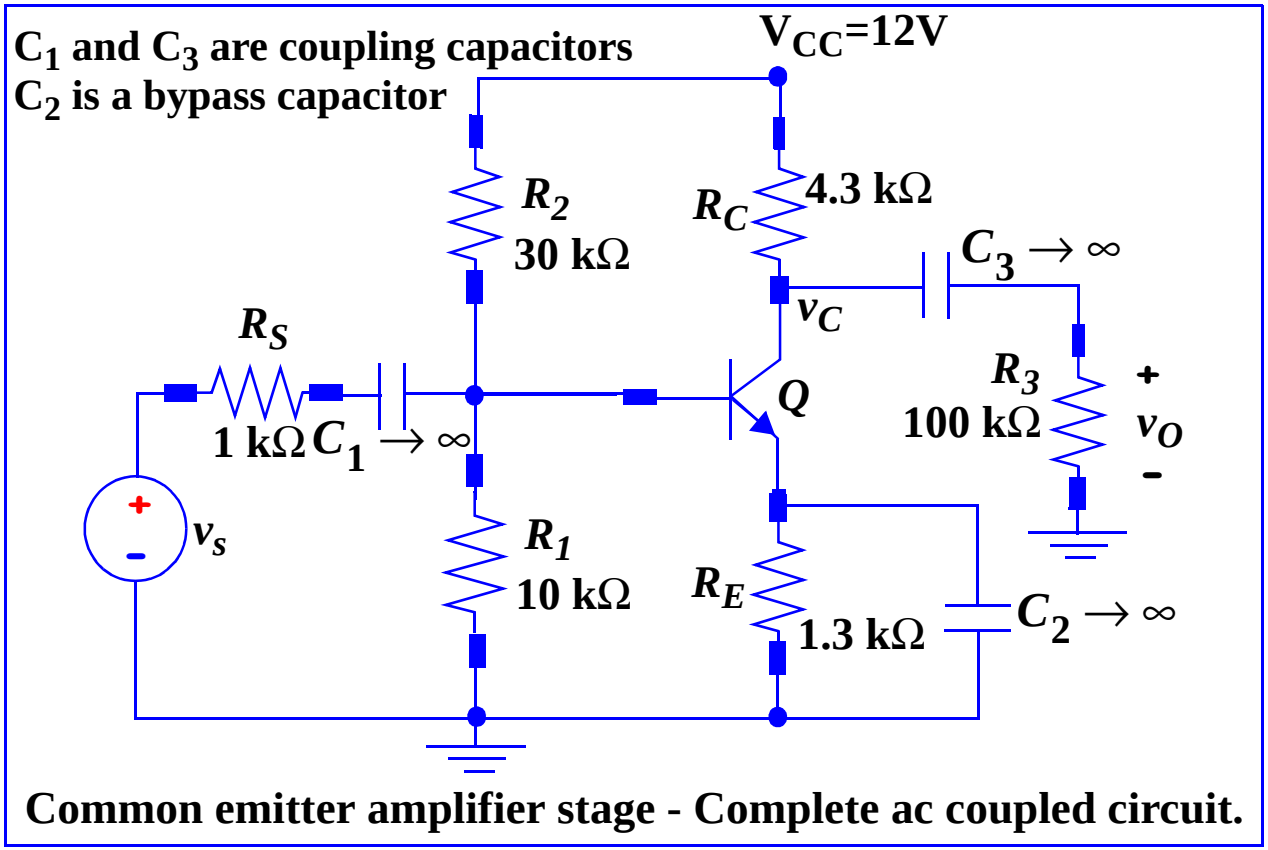
Coupling and Bypass Capacitors

Coupling capacitors (or dc blocking capacitors) are use to decouple ac and dc signals so as not to disturb the quiescent point of the circuit when ac signals are injected at the input.

Bypass capacitors are used to force signal currents around elements by providing a low impedance path at the frequency.



Common emitter amplifier stage - Complete ac coupled circuit.

Circuit Analysis - dc & ac Equivalent Circuits

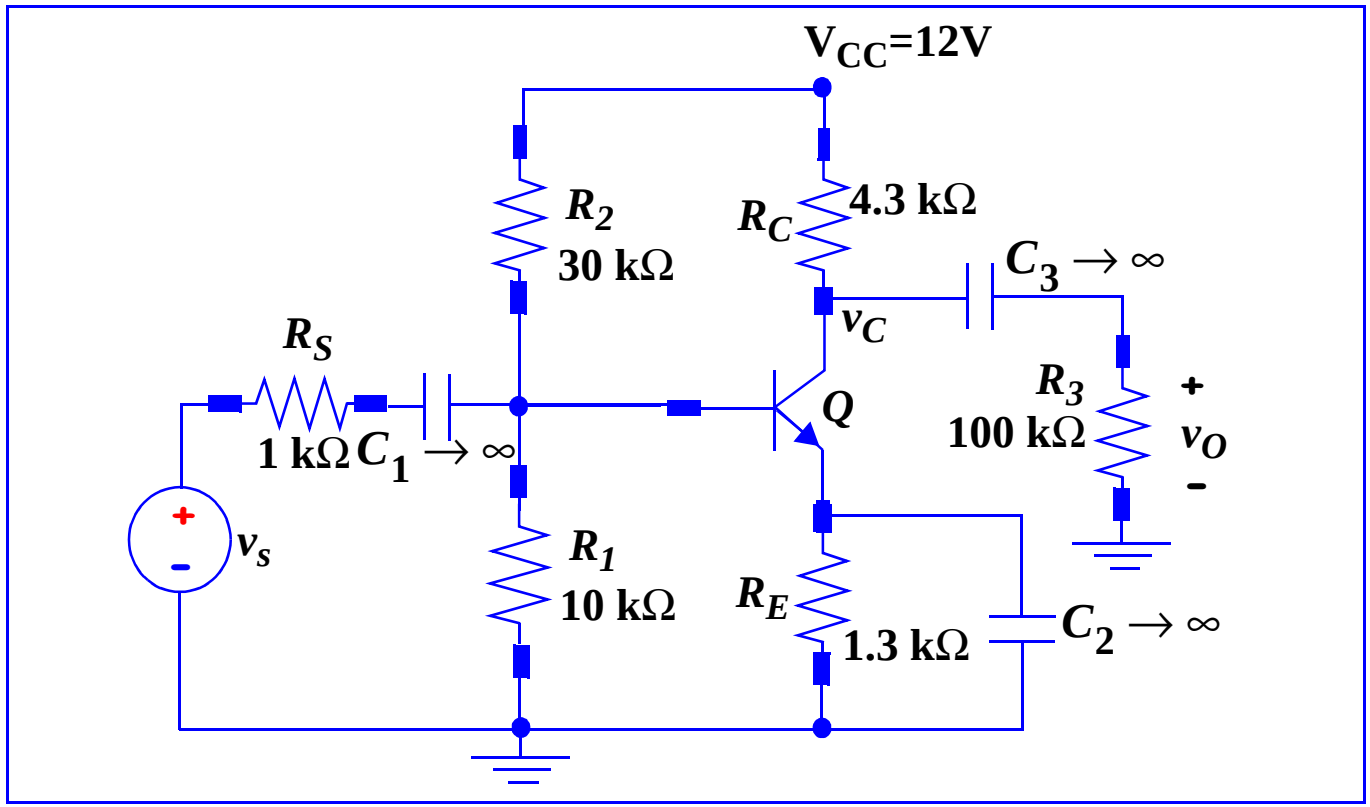
DC Analysis

1. Find dc equivalent circuit. C's replaced by open circuits and L's replaced by short circuits.
2. Find Q-point from dc equivalent circuit using appropriate large-signal model for transistor.

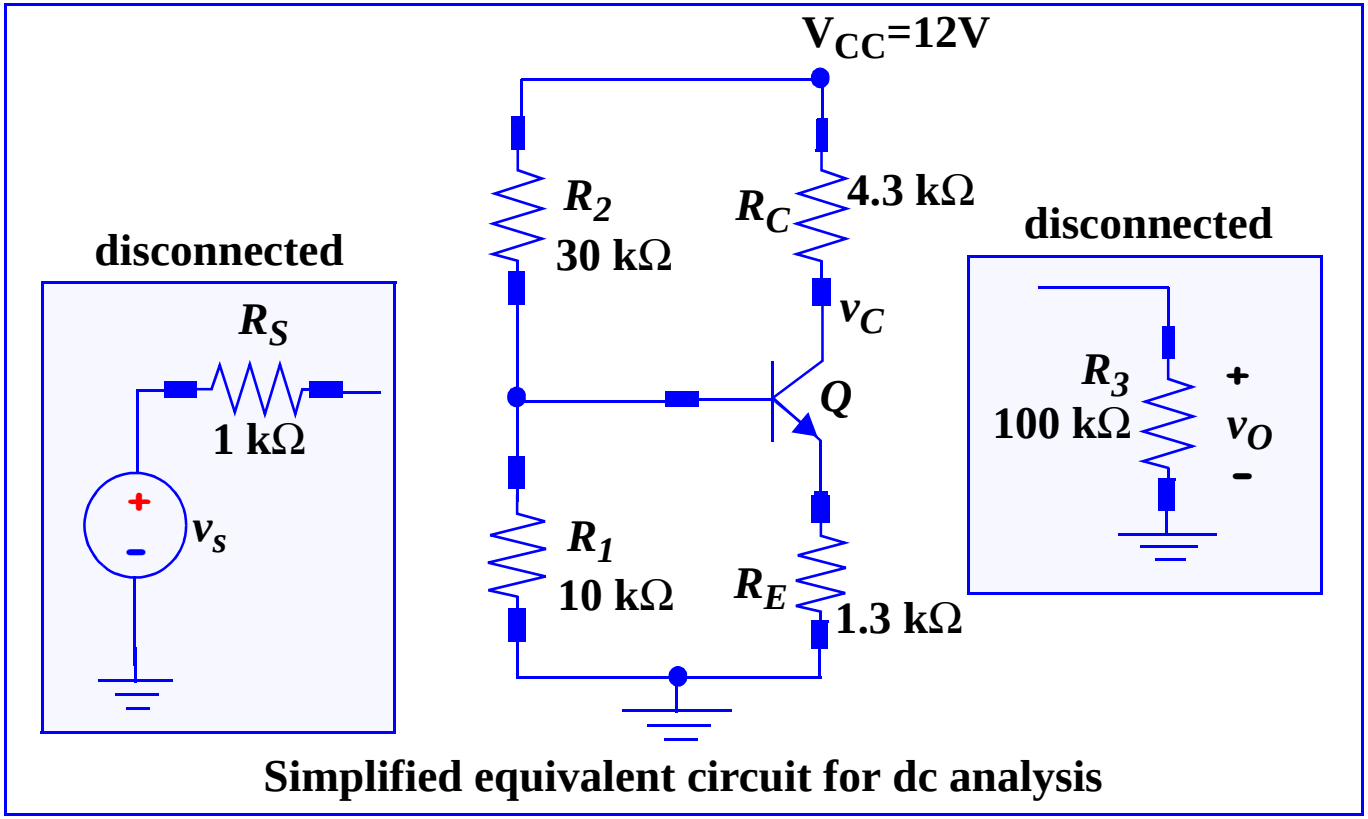
AC Analysis

3. Find ac equivalent circuit. C's replaced by short circuits and L's replaced by open circuits. DC voltage sources are replaced by ground connections and dc current sources by open circuits in ac equivalent circuit.
4. Replace transistor by small-signal model.
5. Analyze ac characteristics from small-signal ac equivalent circuit.
6. Combine results from #2 and #5 to get total voltages and currents in complete network.

BJT Common-Emitter Amplifier

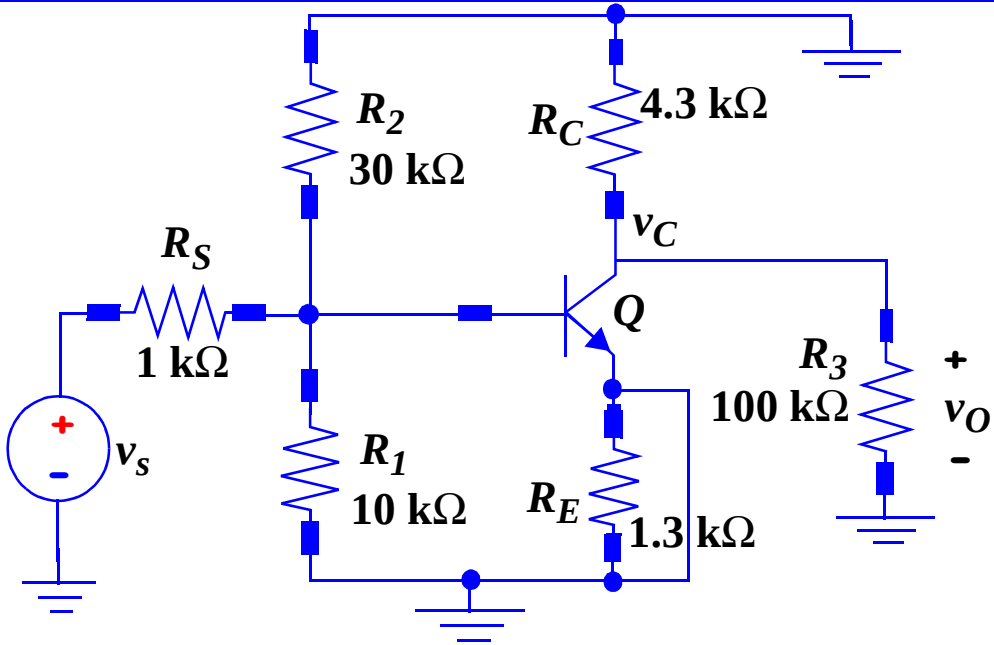


DC Analysis

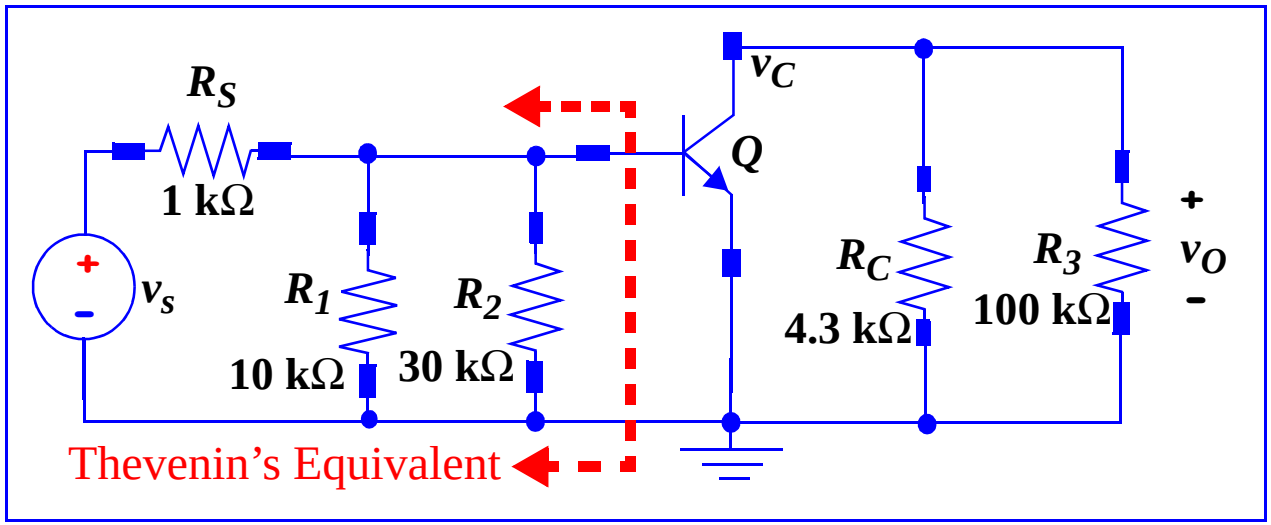


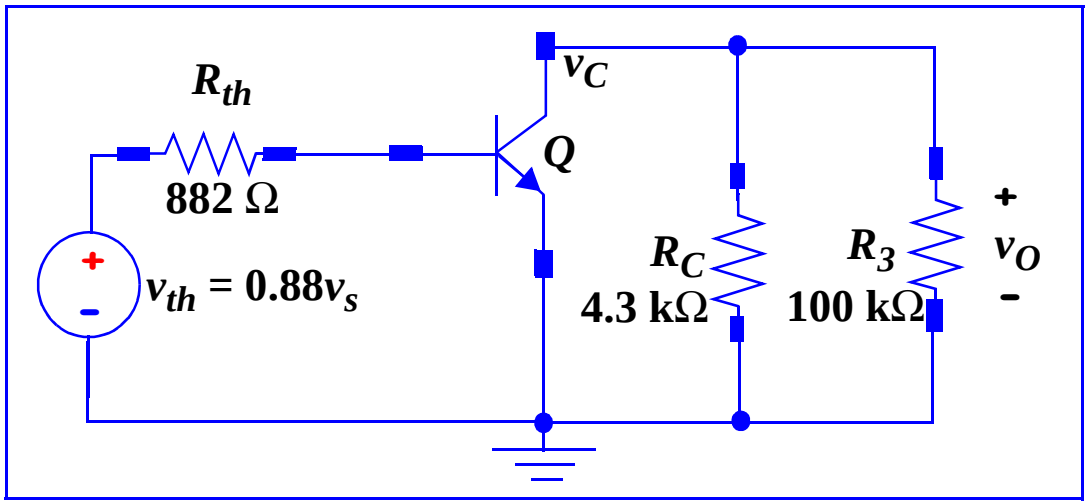
The Q-point is $I_C = 201.5\mu A$, $V_{CE} = 4.30V$.

AC Analysis

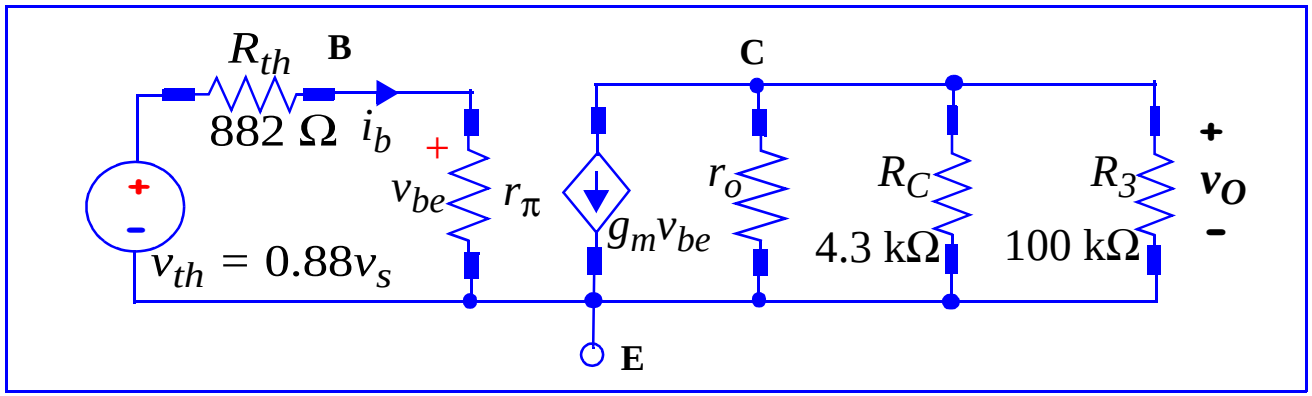


Simplified equivalent circuit for ac analysis



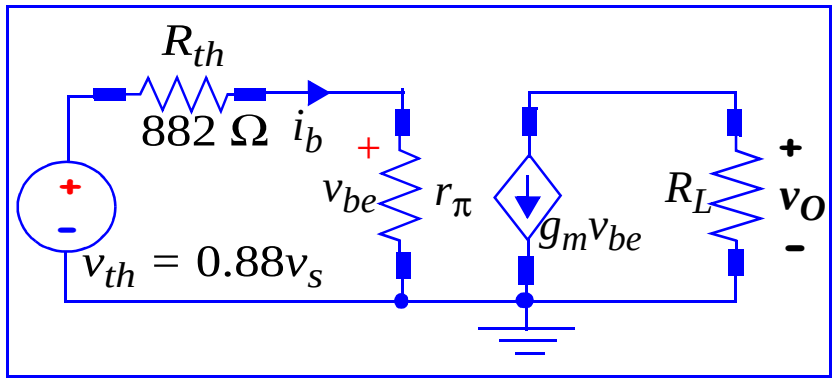


Simplified ac equivalent circuit.



AC Equivalent Circuit with BJT replaced with its SS model.

Final equivalent circuit of common-emitter amplifier.



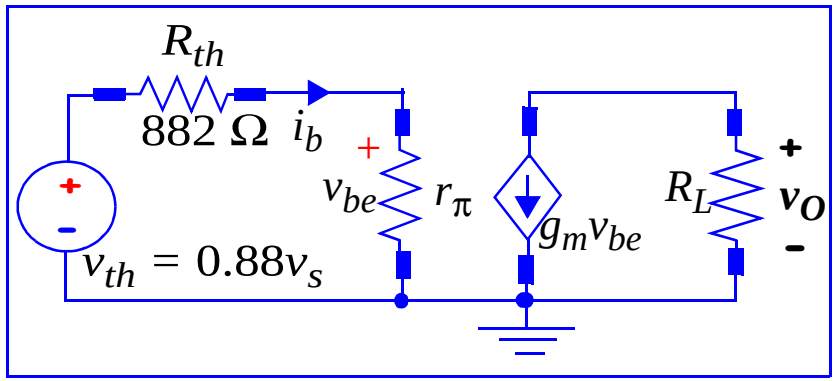
$$R_B = R_1 \| R_2;\ R_{th} = R_S \| R_B;$$

$$v_{th} = \frac{R_B}{R_S + R_B} v_s$$

$$v_{be} = v_{th} \bullet \frac{r_\pi}{r_\pi + R_{th}}$$

The load resistance is $R_L = r_o \| R_C \| R_3$

Final equivalent circuit of common-emitter amplifier.



$$R_B = R_1 \| R_2;\ R_{th} = R_S \| R_B;$$

$$v_{th} = \frac{R_B}{R_S + R_B} v_s$$

$$v_{be} = v_{th} \bullet \frac{r_\pi}{r_\pi + R_{th}}$$

The load resistance is $R_L = r_o \| R_C \| R_3$

Voltage Gain $\boxed{A_{V,\,th} = \frac{v_o}{v_{th}} = -\frac{g_m v_{be} R_L}{v_{th}}}$.

$$\boxed{A_V = \frac{v_o}{v_s} = \frac{-g_m r_\pi R_L}{r_\pi + R_{th}}\left(\frac{R_B}{R_S + R_B}\right) = \frac{-\beta_o R_L}{r_\pi + R_{th}}\left(\frac{R_B}{R_S + R_B}\right)}.$$

$$\boxed{A_V = \frac{v_o}{v_s} = \frac{-g_m R_L}{1 + \frac{R_{th}}{r_\pi}} \bullet \frac{1}{1 + \frac{R_S}{R_B}}}.$$

Model Simplifications

Generally $R_S \ll R_B$ and $R_{th} \ll r_\pi$, so $\boxed{A_V = -g_m R_L = -g_m(r_o \parallel R_C \parallel R_3)}$.

This is the mismatched condition.

Design Guide for CE BJT Amplifier

Typically, $r_o \gg R_3$ and in design, $R_3 \gg R_C$, so $r_o \parallel R_C \parallel R_3 \approx R_C$.

Therefore, $\boxed{A_V = -g_m R_L \approx -g_m R_C = \frac{-I_C R_C}{V_T}}$.

Putting $I_C R_C = \zeta V_{CC}$ with $0 \le \zeta \le 1$, we get $A_V \approx \frac{-\zeta V_{CC}}{V_T} \approx -40\zeta V_{CC}$.

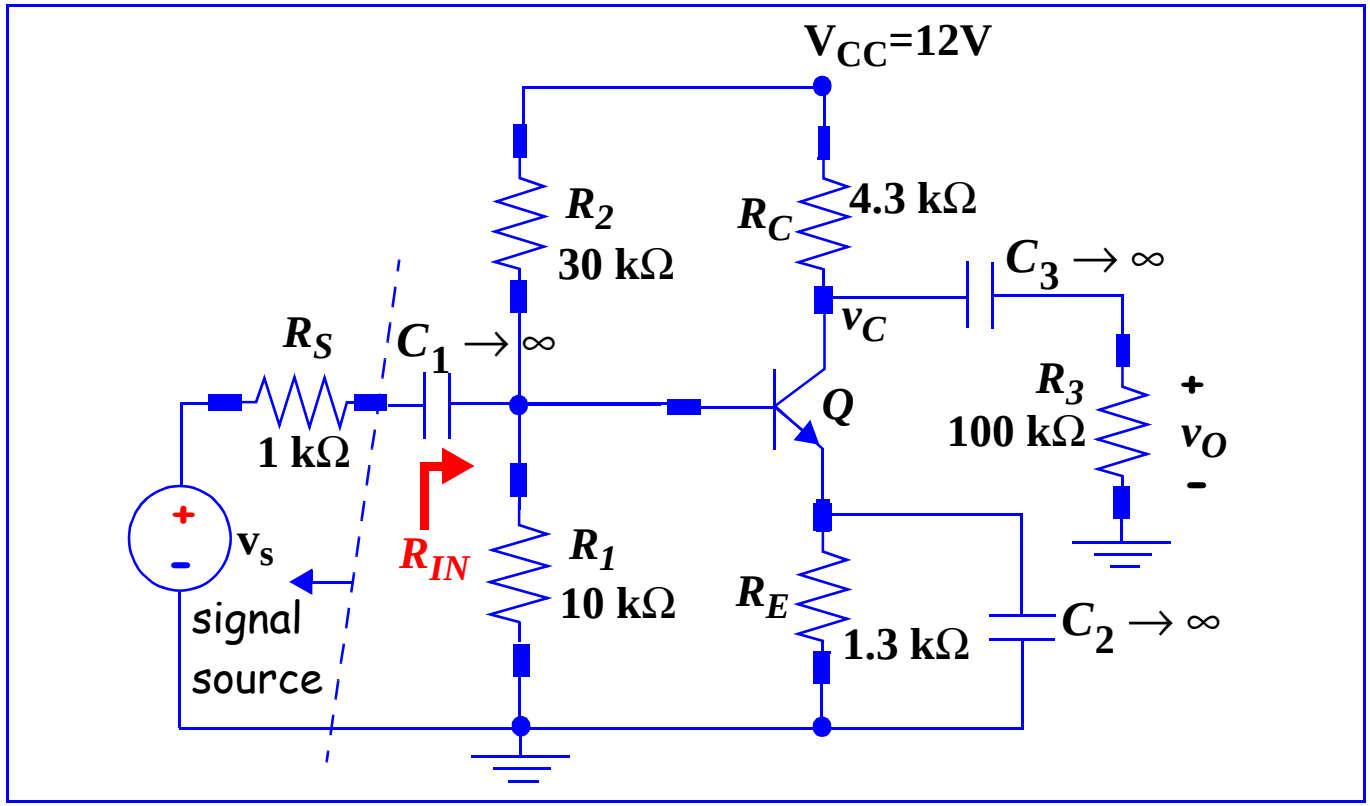
For $\zeta = 0.25$, we get, $\boxed{A_V \approx -10 V_{CC}}$

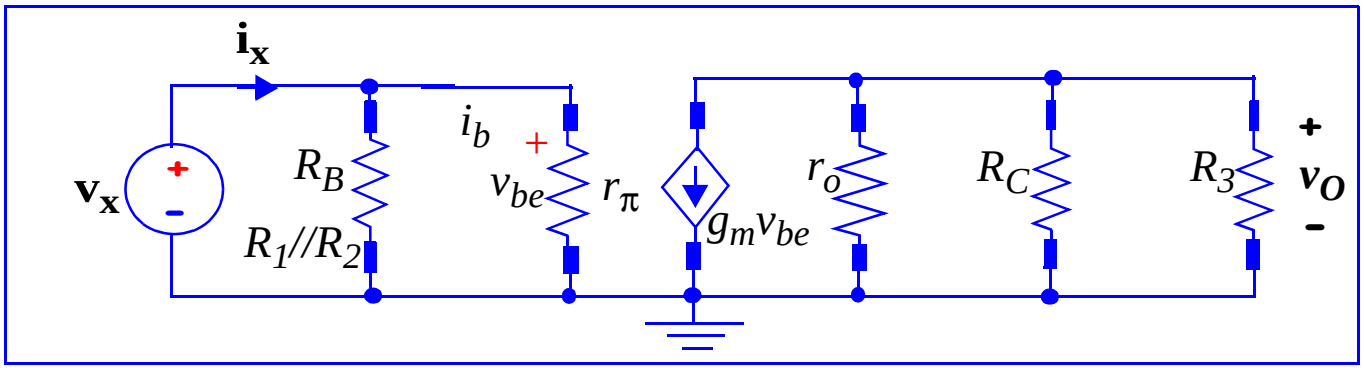
Upper Bound for CE Voltage Gain

Letting $R_L \to r_o$ and in design, $R_3, R_C \to \infty$, we get

$\boxed{A_V = -g_m r_o = -\mu_f}$.

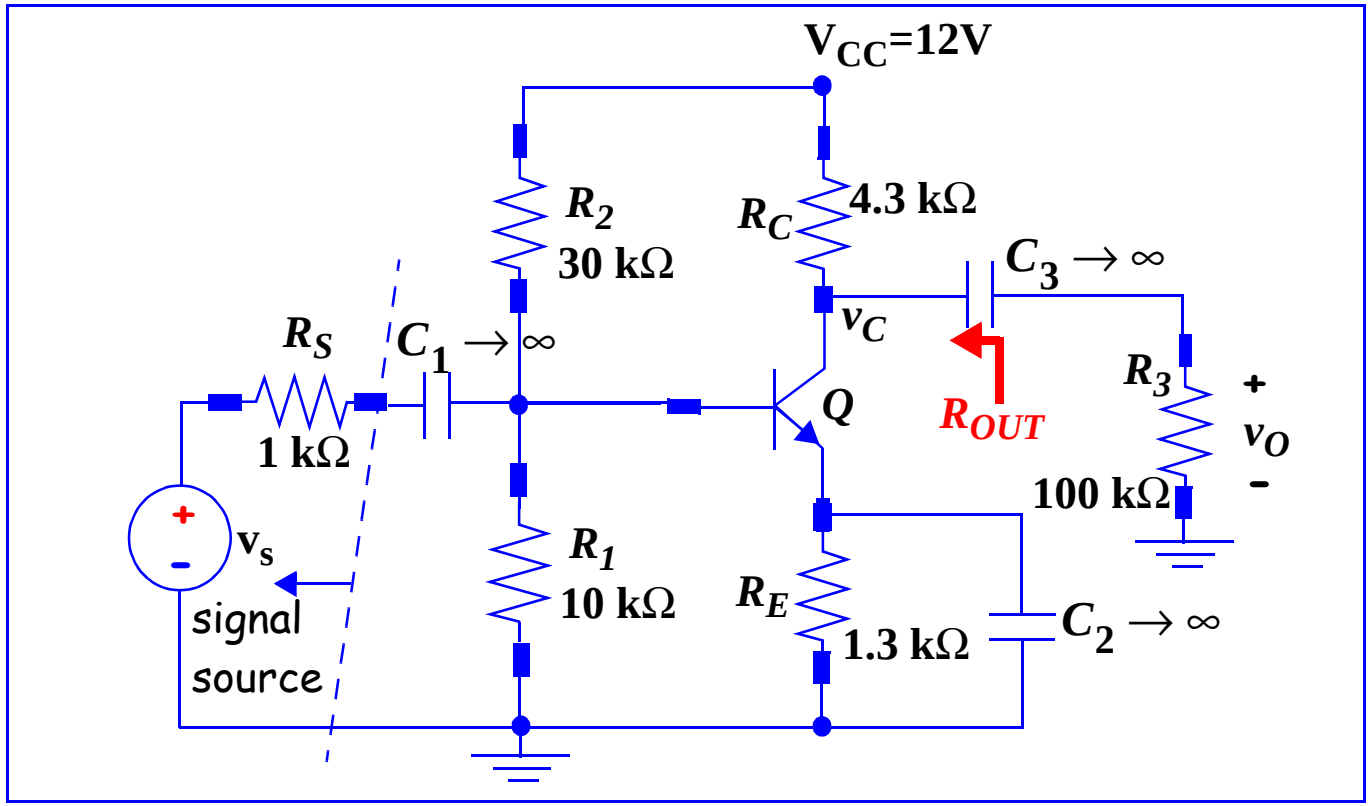
Input Resistance of CE BJT Amplifier

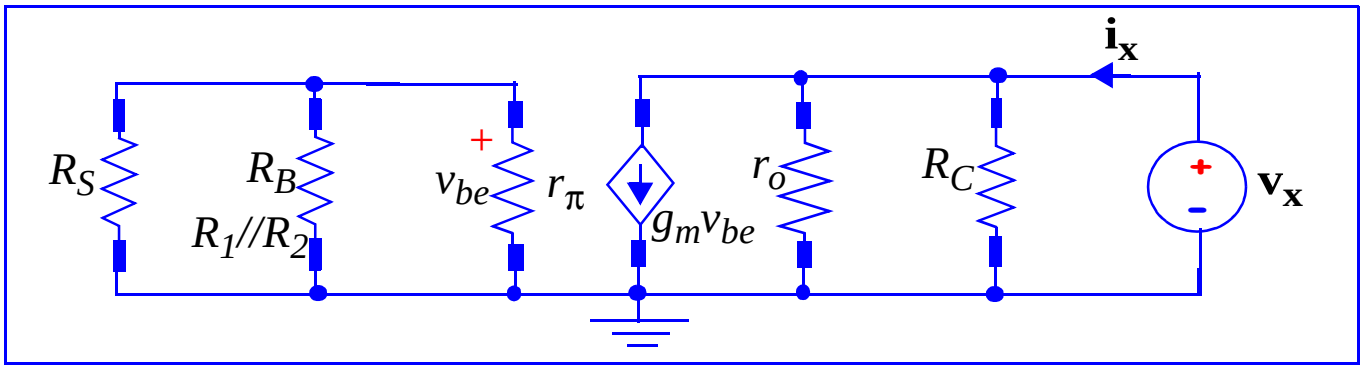




$\mathbf{v_x} = \mathbf{i_x}(R_B \| r_\pi)$ and $\boxed{R_{IN} = \dfrac{\mathbf{v_x}}{\mathbf{i_x}} = R_B \| r_\pi = R_1 \| R_2 \| r_\pi}$

Output Resistance of CE BJT Amplifier

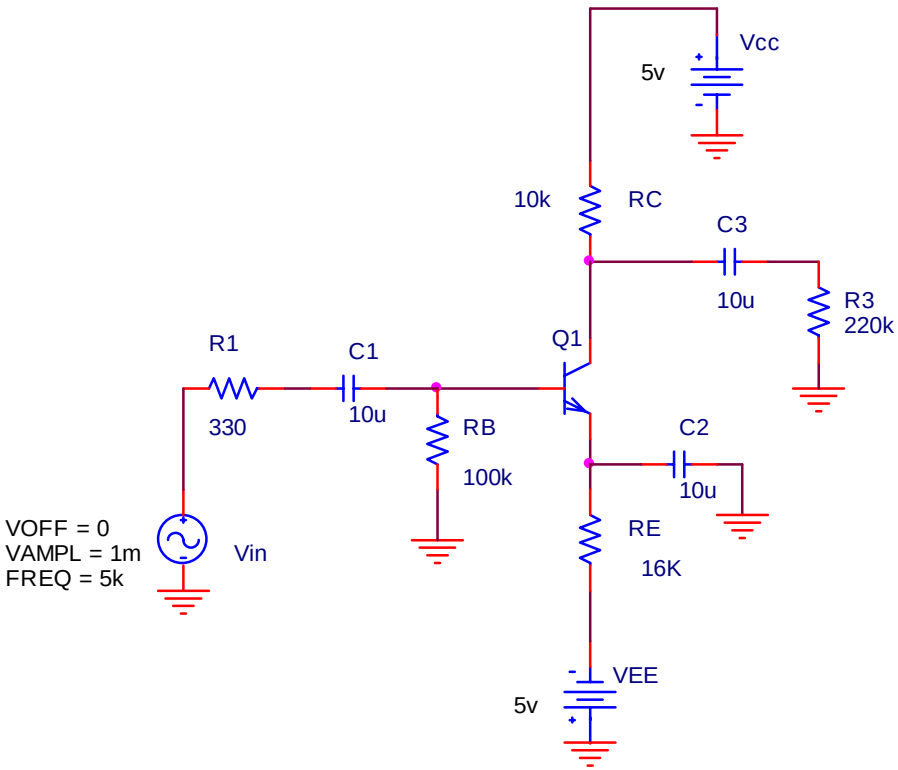




$i_x = \frac{v_x}{R_C} + \frac{v_x}{r_0} + g_m v_{be}$. No excitation at the base node, so $v_{be} = 0$.

$R_{OUT} = \frac{v_x}{i_x} = R_C \| r_0$. $I_C r_0 \approx V_A$ and $I_C R_C \approx \frac{V_{CC}}{2}$.

PSPICE EXAMPLE



***Libraries:**
*** Local Libraries :**
.LIB ".\example12.lib"
*** From [PSPICE NETLIST] section of C:\Program Files\OrcadLite\PSpice\PSpice.ini file:**
.lib "nom.lib"
***Analysis directives:**
.TRAN 0 5ms 0 1u
.PROBE V(*) I(*) W(*) D(*) NOISE(*)
.INC ".\example12-SCHEMATIC1.net"

PSPICE EXAMPLE (Cont'd)

```
**** INCLUDING example12-SCHEMATIC1.net ****
* source EXAMPLE12
R_RC        N00280 N00349  10k
R_RE        N00334 N00307  16K
R_R3        0 N00527  220k
V_Vin        N00822 0
+SIN 0 1m 5k 0 0 0
R_R1        N00726 N00822  330
R_RB        N00656 0  100k
C_C1        N00726 N00656  10u
V_Vcc        N00349 0 5v
C_C3        N00280 N00527  10u
V_VEE         0 N00334 5v
C_C2        N00307 0  10u
Q_Q1        N00280 N00656 N00307 Qbreakn

**** RESUMING example12-SCHEMATIC1-Example12Profile.sim.cir ****
.END
 ****     BJT MODEL PARAMETERS
******************************************************************************
       Qbreakn
        NPN
        IS  100.000000E-18
        BF   65
        NF    1
       VAF    1.000000E+03
        BR    1
        NR    1
        CN    2.42
```

PSPICE EXAMPLE (Cont'd)

```
      D    .87
 ****     INITIAL TRANSIENT SOLUTION       TEMPERATURE =   27.000 DEG C
********************************************************************************

 NODE   VOLTAGE    NODE   VOLTAGE    NODE   VOLTAGE    NODE   VOLTAGE
(N00280)   2.6024 (N00307)  -1.1050 (N00334)  -5.0000 (N00349)   5.0000
(N00527)   0.0000 (N00656)   -.3678 (N00726)   0.0000 (N00822)   0.0000

VOLTAGE SOURCE CURRENTS
 NAME         CURRENT

    V_Vin        0.000E+00
    V_Vcc       -2.398E-04
    V_VEE        -2.434E-04
```