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ECE 2EI4 Quiz 3 (Section 1)

Use the following formulae in your solutions

NMOS Transistor Mathematical Model

Cut off region $i_{DS}=0$ for $v_{GS} < V_{TN}$

Linear region $i_{DS} = K_n(v_{GS} - V_{TN} - 0.5\,v_{DS})\,v_{DS}$ for $v_{GS}\text{-}V_{TN} \geq v_{DS} \geq 0$

Saturation region $i_{DS} = \frac{K_n}{2}(v_{GS} - V_{TN})^2(1+\lambda v_{DS})$ for $v_{DS} \geq v_{GS}\text{-}V_{TN} \geq 0$

PMOS Transistor Mathematical Model

Cut off region $i_{SD}=0$ for $v_{SG} < -V_{TP}$

Linear region $i_{SD} = K_p(v_{SG} + V_{TP} - 0.5v_{SD})v_{SD}$ for $v_{SG}+V_{TP} \geq v_{SD} \geq 0$

Saturation region $i_{SD} = \frac{K_p}{2}(v_{SG}+V_{TP})^2(1+\lambda v_{SD})$ for $v_{SD} \geq v_{SG}+V_{TP} \geq 0$

Small signal Model Parameter of NMOS Transistors

$$g_m = \sqrt{2K_n I_{DS}(1+\lambda V_{DS})}$$

$$r_o = \frac{\frac{1}{\lambda}+V_{DS}}{I_{DS}}$$

Propagation delays for reference CMOS inverter with V_{DD}=5V, V_{TN}=1V and V_{TP}=-1V

$$\tau_{PHL} = 0.322\frac{C}{K_n}$$

$$\tau_{PLH} = 0.322\frac{C}{K_p}$$

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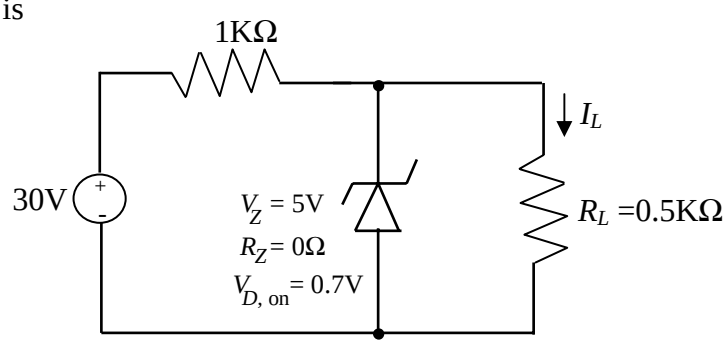
1) For the shown circuit, the load current I_L is

a) -10 mA
b) 1.4 mA
c) 20 mA
d) 10 mA
e) -1.4 mA

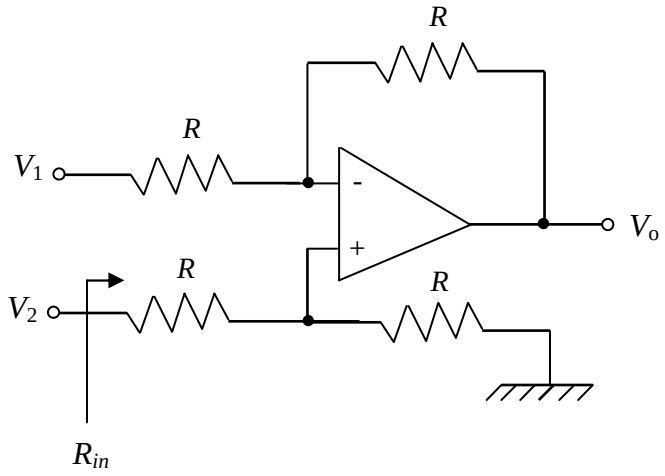


2) In question (1), the smallest allowed value of the load resistance R_L for the Zener diode to work as a regulator is

a) 0.1 KΩ
b) 0.2 KΩ
c) 0.3 KΩ
d) 0.4 KΩ
e) 0.5 KΩ

3) The input resistance R_{in} for the shown ideal OpAmp circuit is

a) ∞ Ω
b) 0 Ω
c) 0.5R Ω
d) R Ω
e) 2R Ω



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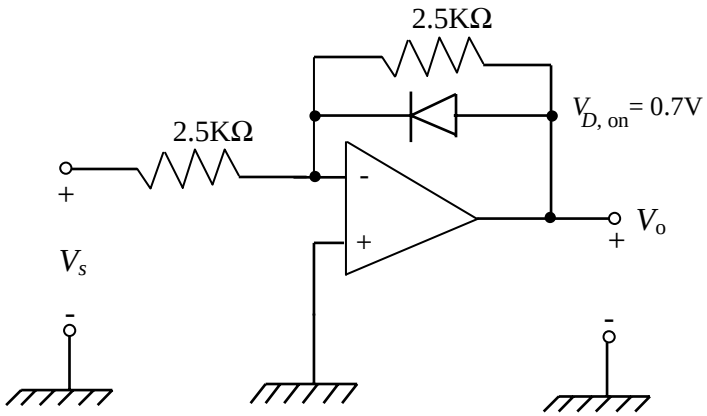
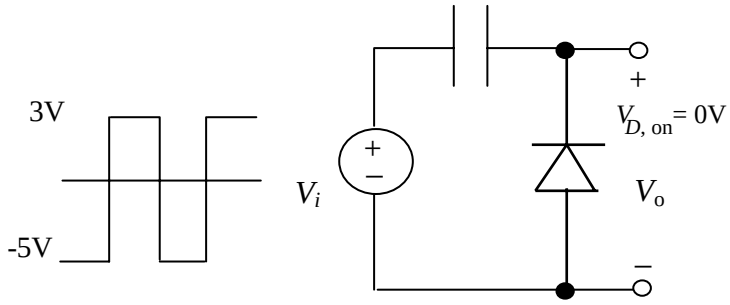
4) For the shown circuit, if V_s= -2.0 V then V_o is

a) -2.0 V
b) -0.7 V
c) 0.7 V
d) 2.0 V
e) -4.0 V



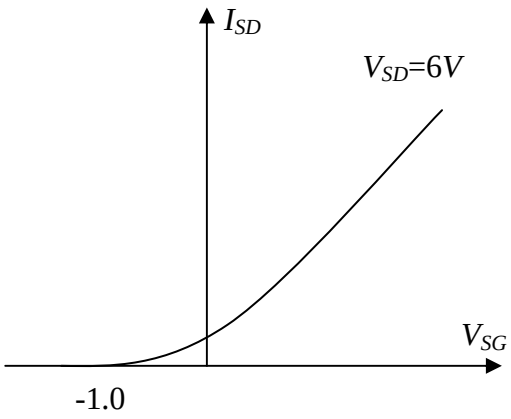
5) The maximum and minimum values of the output voltage V_o for the shown periodic input signal are

a) 8.0 V, 0 V
b) 0 V, -8.0 V
c) 3.0 V, -3.0 V
d) 5.0 V, -5.0 V
e) 3.0 V, 0 V



6) The shown transfer characteristics is for

a) depletion type NMOS
b) depletion type PMOS
c) enhancement type NMOS
d) enhancement type PMOS
e) enhancement type CMOS



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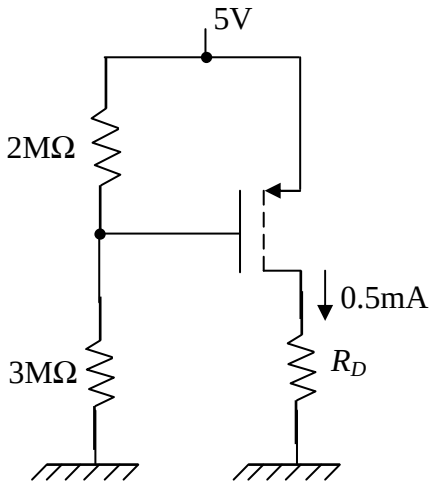
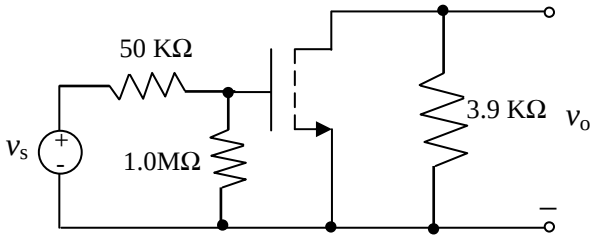
7) The shown enhancement PMOS transistor is operating in the saturation region with I_{SD}=0.5 mA. Given that V_{TP}=-1.0 V, K_p=1.0 mA/V^2 and λ=0 V^{-1}, the largest value of the resistance R_D to maintain saturation operation is

a) 1.0 KΩ
b) 2.0 KΩ
c) 4.0 KΩ
d) 6.0 KΩ
e) 8.0 KΩ



8) The figure to the right shows the ac equivalent circuit of an amplifier circuit with K_n=1.0 mA/V^2, V_{TN}=1.0 V and λ=0 V^{-1}. Given that the operating point is (I_{DS}, V_{DS})=(2.0 mA ,7.5 V), the small signal gain v_o/vs is approximately

a) -3.2
b) 3.2
c) -7.4
d) 7.4
e) -5.3



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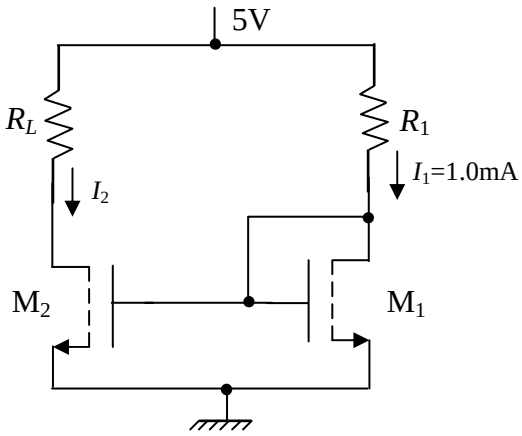
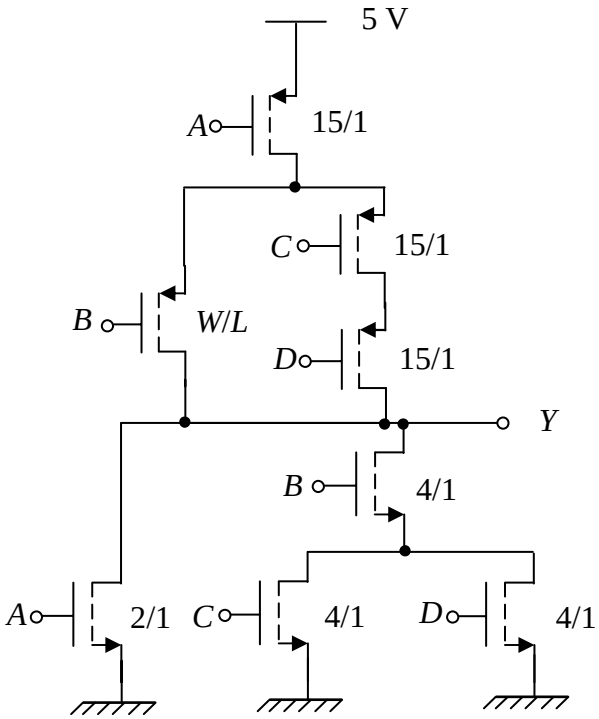
9) Consider the circuit shown to the right. The bias resistor R_1 and the load resistor R_L are selected such that both transistors M_1 and M_2 operate in the saturation region. Given that V_{TN1}= V_{TN2}=1.0 V, $K'_{N1} = K'_{N2} = 1.0\,\text{mA}/V^2$, $(W/L)_1$=2/1 and $(W/L)_2$=6/1, and $\lambda_1 = \lambda_2$=0 V^{-1}, the current I_2 is



a) 3.0 mA
b) 2.0 mA
c) 1.0 mA
d) 0.33 mA
e) None of the above

10) The shown CMOS circuit implements the logic function $\boldsymbol{Y} = \overline{\boldsymbol{A} + \boldsymbol{BC} + \boldsymbol{BD}}$. To obtain worst case delay equal to that of a reference CMOS inverter, the ratio *W*/*L* should be



a) 15/1
b) 5/1
c) 2.5/1
d) 7.5/1
e) 2/1