



SN54LS/74LS192 SN54LS/74LS193

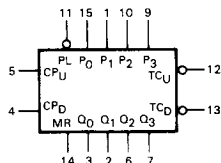
DESCRIPTION — The SN54LS/74LS192 is an UP/DOWN BCD Decode (8421) Counter and the SN54LS/74LS193 is an UP/DOWN MODULO-16 Binary Counter. Separate Count Up and Count Down Clocks are used and in either counting mode the circuits operate synchronously. The outputs change state synchronous with the LOW-to-HIGH transitions on the clock inputs.

Separate Terminal Count Up and Terminal Count Down outputs are provided which are used as the clocks for a subsequent stages without extra logic, thus simplifying multistage counter designs. Individual preset inputs allow the circuits to be used as programmable counters. Both the Parallel Load (PL) and the Master Reset (MR) inputs asynchronously override the clocks.

- **LOW POWER . . . 95 mW TYPICAL DISSIPATION**
- **HIGH SPEED . . . 40 MHz TYPICAL COUNT FREQUENCY**
- **SYNCHRONOUS COUNTING**
- **ASYNCHRONOUS MASTER RESET AND PARALLEL LOAD**
- **INDIVIDUAL PRESET INPUTS**
- **CASCADING CIRCUITRY INTERNALLY PROVIDED**
- **INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS**

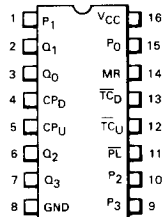
**PRESETTABLE BCD/DECADE
UP/DOWN COUNTER**
**PRESETTABLE 4-BIT BINARY
UP/DOWN COUNTER**
LOW POWER SCHOTTKY

LOGIC SYMBOL



VCC = Pin 16
GND = Pin 8

CONNECTION DIAGRAM DIP (TOP VIEW)



J Suffix — Case 620-08
(Ceramic)
N Suffix — Case 648-05
(Plastic)

NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

PIN NAMES

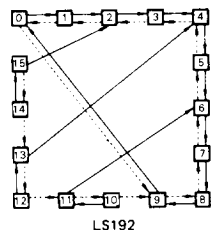
CP _U	Count Up Clock Pulse Input
CP _D	Count Down Clock Pulse Input
MR	Asynchronous Master Reset (Clear) Input
PL	Asynchronous Parallel Load (Active LOW) Input
P _n	Parallel Data Inputs
Q _n	Flip-Flop Outputs (Note b)
TC _D	Terminal Count Down (Borrow) Output (Note b)
TC _U	Terminal Count Up (Carry) Output (Note b)

LOADING (Note a)

	HIGH	LOW
CP _U	0.5 U.L.	0.25 U.L.
CP _D	0.5 U.L.	0.25 U.L.
MR	0.5 U.L.	0.25 U.L.
PL	0.5 U.L.	0.25 U.L.
P _n	0.5 U.L.	0.25 U.L.
Q _n	10 U.L.	5(2.5) U.L.
TC _D	10 U.L.	5(2.5) U.L.
TC _U	10 U.L.	5(2.5) U.L.

- NOTES:**
a. 1 TTL Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW
b. The Output LOW drive factor is 2.5 U.L. for MILITARY (54) and 5 U.L. for COMMERCIAL (74) Temperature Ranges.

STATE DIAGRAMS



LS192 LOGIC EQUATIONS FOR TERMINAL COUNT

$$\overline{TC}_U = Q_0 \cdot Q_3 \cdot \overline{CP}_U$$

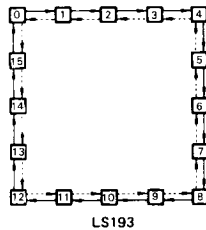
$$\overline{TC}_D = \overline{Q_0} \cdot \overline{Q_1} \cdot \overline{Q_2} \cdot \overline{Q_3} \cdot \overline{CP}_D$$

LS193 LOGIC EQUATIONS FOR TERMINAL COUNT

$$\overline{TC}_U = Q_0 \cdot Q_1 \cdot Q_2 \cdot Q_3 \cdot \overline{CP}_U$$

$$\overline{TC}_D = \overline{Q_0} \cdot \overline{Q_1} \cdot \overline{Q_2} \cdot \overline{Q_3} \cdot \overline{CP}_D$$

COUNT UP —
COUNT DOWN



FUNCTIONAL DESCRIPTION — The LS192 and LS193 are Asynchronously Presettable Decade and 4-Bit Binary Synchronous UP/DOWN (Reversible) Counters. The operating modes of the LS192 decade counter and the LS193 binary counter are identical, with the only difference being the count sequences as noted in the State Diagrams. Each circuit contains four master/slave flip-flops, with internal gating and steering logic to provide master reset, individual preset, count up and count down operations.

Each flip-flop contains JK feedback from slave to master such that a LOW-to-HIGH transition on its T input causes the slave, and thus the Q output to change state. Synchronous switching, as opposed to ripple counting, is achieved by driving the steering gates of all stages from a common Count Up line and a common Count Down line, thereby causing all state changes to be initiated simultaneously. A LOW-to-HIGH transition on the Count Up input will advance the count by one; a similar transition on the Count Down input will decrease the count by one. While counting with one clock input, the other should be held HIGH. Otherwise, the circuit will either count by twos or not at all, depending on the state of the first flip-flop, which cannot toggle as long as either Clock input is LOW.

The Terminal Count Up (\overline{TC}_U) and Terminal Count Down (\overline{TC}_D) outputs are normally HIGH. When a circuit has reached the maximum count state (9 for the LS192, 15 for the LS193), the next HIGH-to-LOW transition of the Count Up Clock will cause \overline{TC}_U to go LOW. \overline{TC}_U will stay LOW until CP_U goes HIGH again, thus effectively repeating the Count Up Clock, but delayed by two gate delays. Similarly, the \overline{TC}_D output will go LOW when the circuit is in the zero state and the Count Down Clock goes LOW. Since the TC outputs repeat the clock waveforms, they can be used as the clock input signals to the next higher order circuit in a multistage counter.

Each circuit has an asynchronous parallel load capability permitting the counter to be preset. When the Parallel Load ($\overline{P_L}$) and the Master Reset (MR) inputs are LOW, information present on the Parallel Data inputs (P_0, P_3) is loaded into the counter and appears on the outputs regardless of the conditions of the clock inputs. A HIGH signal on the Master Reset input will disable the preset gates, override both Clock inputs, and latch each Q output in the LOW state. If one of the Clock inputs is LOW during and after a reset or load operation, the next LOW-to-HIGH transition of that Clock will be interpreted as a legitimate signal and will be counted.

MODE SELECT TABLE

MR	$\overline{P_L}$	CP_U	CP_D	MODE
H	X	X	X	Reset (Asyn.)
L	L	X	X	Preset (Asyn.)
L	H	H	H	No Change
L	H	J	H	Count Up
L	H	H	J	Count Down

L = LOW Voltage Level
H = HIGH Voltage Level
X = Don't Care
J = LOW-to-HIGH Clock Transition