# MOTOROLA

**DESCRIPTION** — The LSTTL/MSI SN54LS/74LS253 is a Dual 4-Input Multiplexer with 3-state outputs. It can select two bits of data from four sources using common select inputs. The outputs may be individually switched to a high impedance state with a HIGH on the respective Output Enable ($\overline{E}_O$) inputs, allowing the outputs to interface directly with bus oriented systems. It is fabricated with the Schottky barrier diode process for high speed and is completely compatible with all Motorola TTL families.

- SCHOTTKY PROCESS FOR HIGH SPEED
- MULTIFUNCTION CAPABILITY
- NON-INVERTING 3-STATE OUTPUTS
- INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS

## SN54LS253
## SN74LS253

### DUAL 4-INPUT MULTIPLEXER WITH 3-STATE OUTPUTS

LOW POWER SCHOTTKY

### PIN NAMES

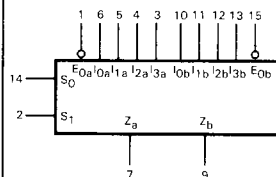| | | LOADING (Note a) | |
|---|---|---|---|
| | | HIGH | LOW |
| $S_0$, $S_1$ | Common Select Inputs | 0.5 U.L. | 0.25 U.L. |
| **Multiplexer A** | | | |
| $\overline{E}_{0a}$ | Output Enable (Active LOW) Input | 0.5 U.L. | 0.25 U.L. |
| $I_{0a} - I_{3a}$ | Multiplexer Inputs | 0.5 U.L. | 0.25 U.L. |
| $Z_a$ | Multiplexer Output (Note b) | 65(25) U.L. | 15(7.5) U.L. |
| **Multiplexer B** | | | |
| $\overline{E}_{0b}$ | Output Enable (Active LOW) Input | 0.5 U.L. | 0.25 U.L. |
| $I_{0b} - I_{3b}$ | Multiplexer Inputs | 0.5 U.L. | 0.25 U.L. |
| $Z_b$ | Mutiplexer Output (Note b) | 65(25) U.L. | 15(7.5) U.L. |

NOTES:
a. 1 TTL Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW.
b. The Output LOW drive factor is 7.5 U.L. for Military (54) and 15 U.L. for Commercial (74) Temperature Ranges. The Output HIGH drive factor is 25 U.L. for Military (54) and 65 U.L. for Commercial (74) Temperature Ranges.

### LOGIC SYMBOL

$V_{CC}$ = Pin 16
GND = Pin 8

### LOGIC DIAGRAM

$V_{CC}$ = Pin 16
GND = Pin 8
○ = Pin Numbers

### CONNECTION DIAGRAM
### DIP (TOP VIEW)

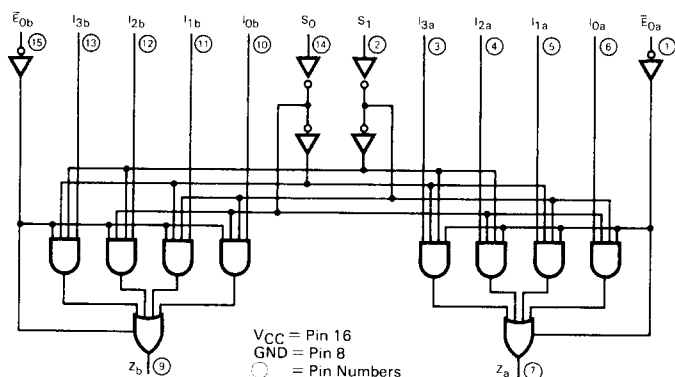| | | |
|---|---|---|
| 1 | $\overline{E}_{0a}$ | $V_{CC}$ 16 |
| 2 | $S_1$ | $\overline{E}_{0b}$ 15 |
| 3 | $I_{3a}$ | $S_0$ 14 |
| 4 | $I_{2a}$ | $I_{3b}$ 13 |
| 5 | $I_{1a}$ | $I_{2b}$ 12 |
| 6 | $I_{0a}$ | $I_{1b}$ 11 |
| 7 | $Z_a$ | $I_{0b}$ 10 |
| 8 | GND | $Z_b$ 9 |
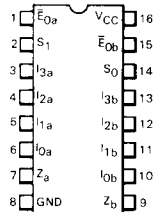
J Suffix — Case 620-08 (Ceramic)
N Suffix — Case 648-05 (Plastic)

NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

**FUNCTIONAL DESCRIPTION** — The LS253 contains two identical 4-Input Multiplexers with 3-state outputs. They select two bits from four sources selected by common select inputs ($S_0$, $S_1$). The 4-input multiplexers have individual Output Enable ($\overline{E}_{0a}$, $\overline{E}_{0b}$) inputs which when HIGH, forces the outputs to a high impedance (high Z) state.

The LS253 is the logic implementation of a 2-pole, 4-position switch, where the position of the switch is determined by the logic levels supplied to the two select inputs. The logic equations for the outputs are shown below:

$$Z_a = \overline{E}_{0a} \cdot (I_{0a} \cdot \overline{S}_1 \cdot \overline{S}_0 + I_{1a} \cdot \overline{S}_1 \cdot S_0 + I_{2a} \cdot S_1 \cdot \overline{S}_0 + I_{3a} \cdot S_1 \cdot S_0)$$
$$Z_b = \overline{E}_{0b} \cdot (I_{0b} \cdot \overline{S}_1 \cdot \overline{S}_0 + I_{1b} \cdot \overline{S}_1 \cdot S_0 + I_{2b} \cdot S_1 \cdot \overline{S}_0 + I_{3b} \cdot S_1 \cdot S_0)$$

If the outputs of 3-state devices are tied together, all but one device must be in the high impedance state to avoid high currents that would exceed the maximum ratings. Designers should ensure that Output Enable signals to 3-state devices whose outputs are tied together are designed so that there is no overlap.

## TRUTH TABLE

| SELECT INPUTS | | DATA INPUTS | | | | OUTPUT ENABLE | OUTPUT |
|---|---|---|---|---|---|---|---|
| $S_0$ | $S_1$ | $I_0$ | $I_1$ | $I_2$ | $I_3$ | $\overline{E}_0$ | Z |
| X | X | X | X | X | X | H | (Z) |
| L | L | L | X | X | X | L | L |
| L | L | H | X | X | X | L | H |
| H | L | X | L | X | X | L | L |
| H | L | X | H | X | X | L | H |
| L | H | X | X | L | X | L | L |
| L | H | X | X | H | X | L | H |
| H | H | X | X | X | L | L | L |
| H | H | X | X | X | H | L | H |

H = HIGH Level
L = LOW Level
X = Irrelevant
(Z) = High Impedance (off)
Address inputs $S_0$ and $S_1$ are common to both sections.

## GUARANTEED OPERATING RANGES

| SYMBOL | PARAMETER | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{CC}$ | Supply Voltage | 54 | 4.5 | 5.0 | 5.5 | V |
| | | 74 | 4.75 | 5.0 | 5.25 | |
| $T_A$ | Operating Ambient Temperature Range | 54 | −55 | 25 | 125 | °C |
| | | 74 | 0 | 25 | 70 | |
| $I_{OH}$ | Output Current — High | 54 | | | −1.0 | mA |
| | | 74 | | | −2.6 | |
| $I_{OL}$ | Output Current — Low | 54 | | | 12 | mA |
| | | 74 | | | 24 | |