MOTOROLA

SN54LS/74LS75
SN54LS/74LS77

4-BIT D LATCH

LOW POWER SCHOTTKY

DESCRIPTION — The TTL/MSI SN54LS/74LS75 and SN54LS/74LS77 are latches used as temporary storage for binary information between processing units and input/output or indicator units. Information present at a data (D) input is transferred to the Q output when the Enable is HIGH and the Q output will follow the data input as long as the Enable remains HIGH. When the Enable goes LOW, the information (that was present at the data input at the time the transition occurred) is retained at the Q output until the Enable is permitted to go HIGH.

The SN54LS/74LS75 features complementary Q and $\overline{Q}$ output from a 4-bit latch and is available in the 16-pin packages. For higher component density applications the SN54LS/74LS77 4-bit latch is available in the 14-pin package with $\overline{Q}$ outputs omitted.

PIN NAMES		LOADING (Note a) HIGH	LOW
D_1–D_4	Data Inputs	0.5 U.L.	0.25 U.L.
E_{0-1}	Enable Input Latches 0, 1	2.0 U.L.	1.0 U.L.
E_{2-3}	Enable Input Latches 2, 3	2.0 U.L.	1.0 U.L.
Q_1–Q_4	Latch Outputs (Note b)	10 U.L.	5(2.5) U.L.
$\overline{Q_1}$–$\overline{Q_4}$	Complimentary Latch Outputs (Note b)	10 U.L.	5(2.5) U.L.

Notes:
a. 1 Unit Load (U.L.) = 40 μA HIGH
b. The Output LOW drive factor is 2.5 U.L. for Military (54) and 5 U.L. for Commercial (74) Temperature Ranges.

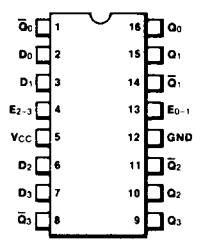
TRUTH TABLE
(Each latch)

t_n	t_{n+1}
D	Q
H	H
L	L

NOTES:
t_n = bit time before enable negative-going transition
t_{n+1} = bit time after enable negative-going transition

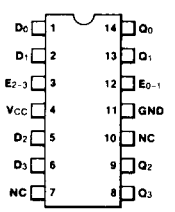
CONNECTION DIAGRAMS
DIP (TOP VIEW)

SN54LS/74LS75



J Suffix — Case 620-08 (Ceramic)
N Suffix — Case 648-05 (Plastic)

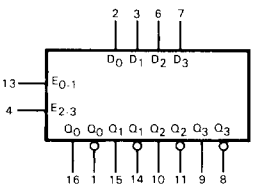
SN54LS/74LS77



J Suffix — Case 632-07 (Ceramic)
N Suffix — Case 646-05 (Plastic)

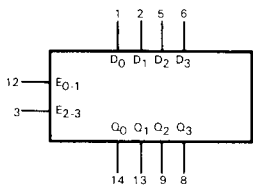
LOGIC SYMBOLS

SN54LS/74LS75



V_{CC} = Pin 5
GND = Pin 12

SN54LS/74LS77



V_{CC} = Pin 4
GND = Pin 11
NC = Pin 7,10