Dr. X. Wu **COE2DI4 Midterm Test #2** Nov. 04 *2013*

Instructions: This examination paper includes 7 pages and 18 multiple-choice questions starting on page 2. You are responsible for ensuring that your copy of the paper is complete. Bring any discrepancy to the attention of your invigilator. Each question is worth one mark. The answers for all the questions must be indicated by filling the corresponding circle on the optical scanning (OMR) examination sheet. Answer all questions. There is no penalty for guessing. This is a closed book exam. No reference material of any kind is permitted. No calculators of any kind are permitted. **Time allowed is 50 minutes**.

Note: A’ and $\overline{A}$ are used interchangeably.

Multiple choice questions (numbered 1 to 18) – indicate your answer by filling the corresponding circle on the OMR answer sheet

1. The decimal equivalent of $(11111010)_2$ represented in sign 1's complement format is:

1. $(-6)_{10}$
2. $(-5)_{10}$
3. $(-122)_{10}$
4. $(-250)_{10}$
5. $(250)_{10}$

2. What is the decimal equivalent of $N = \underbrace{11...1}_{n}.\underbrace{11...1}_{n}$

1. $N = 2^n + 2^{-n} + 1$
2. $N = 2^n - 1 + 2^{-n}$
3. $N = 2^n - 2^{-n}$
4. $N = 2^{n-1} - 2^{-n}$
5. $N = 2^n - 2^{-(n-1)}$

3. Convert the decimal numbers 73 , -91 into 2's complement of 12-bit numbers:

1. $(000001001000)_2$, $(111110100100)_2$
2. $(000001001001)_2$, $(111110100100)_2$
3. $(000001001001)_2$, $(111110100101)_2$
4. $(000001001001)_2$, $(100010100101)_2$
5. none of the above

4. What is the output for the circuit shown in Figure 1?

1. $w = \bar{b}c$
2. $w = b \oplus c$
3. $w = \overline{b \oplus c}$
4. $w = \bar{b} + \bar{c}$
5. $w = bc$

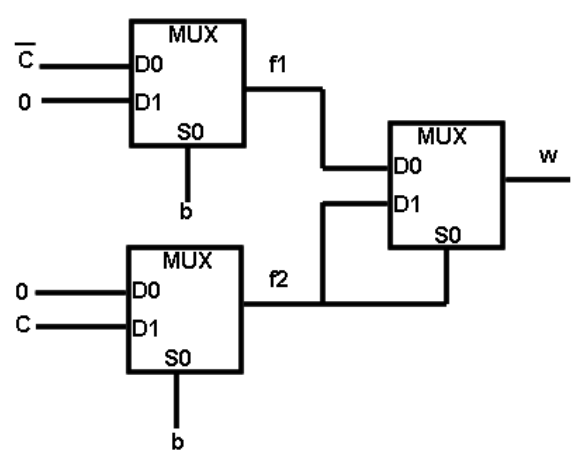
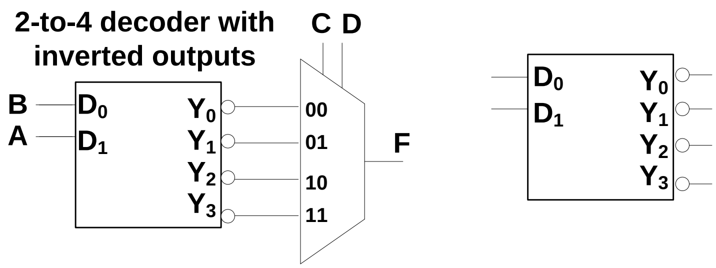


Figure 1 – Circuit for question 4.

5. The circuit shown in Figure 2 is:

1. **F(A,B,C,D)** = ∏ **M**(0,2,13,15)
2. **F(A,B,C,D)** = ∏ **M**(0,4,11,15)
3. **F(A,B,C,D)** = ∏ **M** (0,5,10,15)
4. **F(A,B,C,D)** = ∏ **M** (0,7,8,15)
5. none of the above



D_1 D_0	Y_0 Y_1 Y_2 Y_3
0 0	0 1 1 1
0 1	1 0 1 1
1 0	1 1 0 1
1 1	1 1 1 0

(a) **(b)**

Figure 2 – (a) Circuit for question 5. (b) Truth table of the decoder with inverted outputs

6. How many minterms does function f (X_1, X_2, X_3, X_4) = $X_1 \oplus X_2 \oplus X_3 \oplus X_4$ include:

1. 2
2. 4
3. 8
4. 12
5. 16

7. In Figure 3, if $A_3A_2A_1A_0$ = 1001, $B_3B_2B_1B_0$ = 1101 and S = 1 then the output is:

1. Sum = 0110 and C_4 = 0
2. Sum = 0110 and C_4 = 1
3. Sum = 1100 and C_4 = 0
4. Sum = 1100 and C_4 = 1
5. none of the above

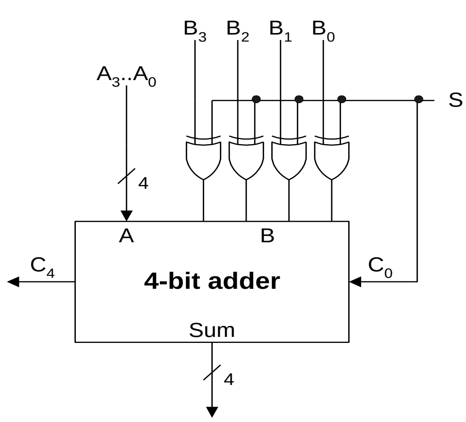


Figure 3 – Circuit for questions 7 to 11. Note, c_0 is carry in and c_4 is carry out for the 4-bit adder.

8. In Figure 3, both A and B are 2's compliment number inputs, and Sum is 2's compliment number output. If $A_3A_2A_1A_0$=0000, S = B_3, then Sum is:

1. Sum = B
2. Sum = -B
3. Sum = |B| (absolute value of B)
4. Sum = 1111
5. none of the above

9. In Figure 3, overflow occurs for:

1. $A_3A_2A_1A_0$=0100, $B_3B_2B_1B_0$=1010 and S=0
2. $A_3A_2A_1A_0$=0100, $B_3B_2B_1B_0$=0110 and S=1
3. $A_3A_2A_1A_0$=1100, $B_3B_2B_1B_0$=0110 and S=0
4. $A_3A_2A_1A_0$=1100, $B_3B_2B_1B_0$=1010 and S=1
5. none of the above

10. In Figure 3, detecting a zero result can be achieved by connecting the output Sum to a:

1. 4-input AND gate
2. 4-input NAND gate
3. 4-input XOR gate
4. 4-input XNOR gate
5. 4-input NOR gate

11. Compared with an n-bit ripple-carry adder, an n-bit carry-lookahead adder:

1. reduces delay while increasing complexity (of the circuit)
2. reduces delay and reduces complexity
3. increases delay and increases complexity
4. increases delay but reduces complexity
5. none of the above

12. A four-variable logic function F(A,B,C,D) equals to 1 if input A is different from input B and if input C is identical to input D. Function F(A,B,C,D) can be written as:

1. F(A,B,C,D) = Σ m (4,7)
2. F(A,B,C,D) = Σ m (8,11)
3. F(A,B,C,D) = $\prod$ M(0,1,2,3,5,6,9,10,12,13,14,15)
4. F(A,B,C,D) = $\prod$ M(0,1,2,3,5,8,9,10,12,13,14,15)
5. none of the above

13. What is the minimum number of logic gates required if we convert the circuit in Figure 4 to a circuit with NAND gates ONLY?

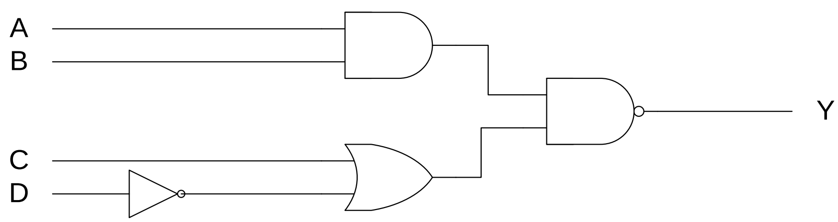


Figure 4

1. 4
2. 5
3. 6
4. 7
5. none of the above

14. Determine the minimum-cost SOP expression for the function F$(x1, x2, x3, x4) = \sum m(4,6,8,10,11,12,15) + D(3,5,7,9)$

1. $\mathbf{f} = \overline{x_1}x_2 + x_1\overline{x_2} + x_3x_4 + x_1\overline{x_3}\ \overline{x_4}$
2. $\mathbf{f} = \overline{x_1}x_2x_3 + x_1\overline{x_2} + x_3x_4 + \overline{x_1}x_3x_4$
3. $\mathbf{f} = \overline{x_1}x_2 + x_1\overline{x_2} + x_3x_4 + \overline{x_3}x_4$
4. $\mathbf{f} = \overline{x_1}x_2 + x_1\overline{x_2} + \overline{x_3}x_4 + x_3\overline{x_4}$
5. none of the above

15. The number of prime implicants of F(A, B, C, D) shown in Figure 5 is:

1. 3
2. 4
3. 5
4. 6
5. none of the above

CD \ AB	00	01	11	10
00	1	1	0	0
01	0	1	1	0
11	0	1	1	0
10	0	0	1	1

Figure 5 - Karnaugh map for a logic function F(A,B,C,D) for questions 16, 17.

16. The number of essential prime implicants of F(A, B, C, D) shown in Figure 5 is:

1. 1
2. 3
3. 4
4. 5
5. none of the above

17. If input z=1 then the output $\mathbf{T_6}$ in Figure 6 is:

1. 0
2. x'y
3. xy'
4. 1
5. none of the above

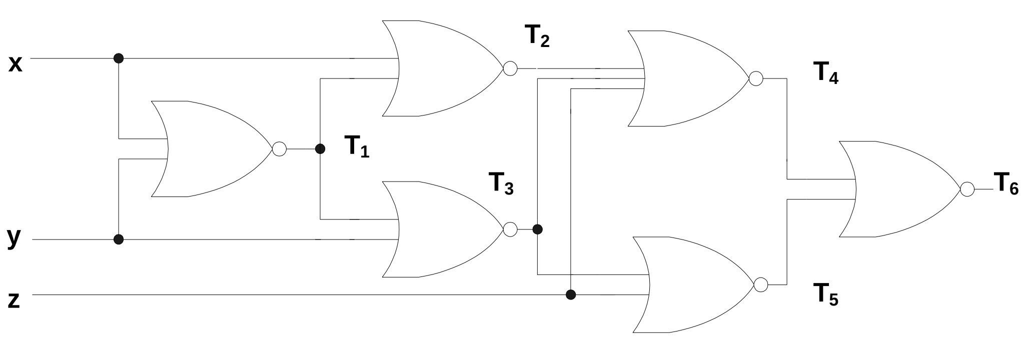


Figure 6

18. You are asked to implement the following four functions with half-adders:

$f_1=A\oplus B\oplus C$
$f_2=A'BC+AB'C$
$f_3=ABC'+(A'+B')C$
$f_4=ABC$

What is the minimum number of half-adders required to implement all four functions simultaneously? (you are not allowed to use any other logic element). Hint: the circuit of a half-adder is shown in Fig. 7.

1. 2
2. 3
3. 4
4. 5
5. 6

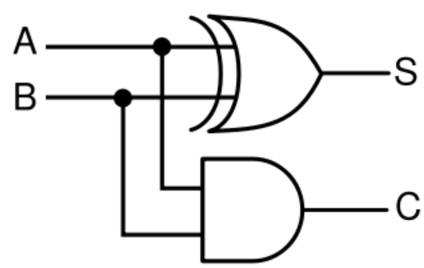


Figure 7 – Half-adder

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